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CONTROL DATA CORPORATION

CDC® MICROCIRCUITS

GENERAL THEORY
LOGIC SYMBOLOGY
DATA SHEETS

NORMANDALE CIRCUITS MANUAL

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REVISION RECORD

REVISION	DESCRIPTION
A	Manual released. This manual replaces and updates the information previously
(1-10-77)	contained in the Logic Symbology subsection and the Integrated Circuit Package
	Configurations section of Hardware Reference manuals produced at CDC's
	Normandale facility.
B	Add 24 microcircuit descriptions. Revise several descriptions for consistent
(2-21-77)	symbology. Make various editorial changes.
C	Add seven microcircuit descriptions. Make various editorial and technical
(5-1-77)	changes.
D	Add six microcircuit descriptions. Revise certain Op Amp data sheets to view
(8-8-77)	metal-can configurations from the bottom of the IC. Make various editorial
	and technical changes.
E	Correct 26 data sheets for technical and minor textual errors.
(12-22-77)	
F	Add 544 (CDC) and 75461 (Vendor) microcircuit descriptions and make various
(5-5-78)	technical corrections.
G	Make technical corrections to elements 176, 195, 500, 949, 10141, 50255700
(7-20-78)	
H	5600/7500 is now a 950A; 75461 is now 951;50255700 is now 5700. Assign
(10-20-78)	correct part numbers to 5100, 5200, 5300, 5400 elements. Make various
	technical/editorial additions and corrections to pages 1-6, 1-11, 147, 189,
	306, 327, 521.
J	Add the following microcircuit descriptions: 227,228,240,243,247,344,352/
(7-1-79)	352A,363,394,934,4052,4053,10115,10136,10192,10198,3BA,2114L,2716,3423,6821,
	79180,82S131. Add Vendor Type/CDC Element ID cross-reference list and
	necessary usage information.
K	Add the following microcircuit descriptions: 2222, 2369, 2732, 2907, 4021,4040,
(11-15-79)	6802, 6840, 9368, 10178; make various technical corrections; rectify paging
	errors for 363 and 368 data sheets.
L	Correct logic symbols for 529, 4016, 4052, 10107, 2716, 2732, 9368.
(2-7-80)	Correct pin configuration for 4052. Make miscellaneous editorial
	corrections.
M	Add 16 new microcircuits: 10113,10195, 14411, 2903, 2910, 6402, 6800, 6810,
(6-5-80)	6875, 74163, 745225, 745288, 75115, 825100/101, TIL 311, and element 370.
	Add clarifications to 300-series pin configurations and make miscellaneous
	editorial additions.

KØR 0639

REVISION LETTERS I,O,Q AND X ARE NOT USED

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or use Comment Sheet in the back of this manual.

PREFACE

This manual provides the customer engineer with a functional understanding of the microcircuits used in equipment manufactured by the Normandale facility. It is not intended to be a logic designer's handbook and does not include design ground rules for using the microcircuits.

Section 1 discusses the characteristics, operational theory, and physical packaging of TTL (transistor-transistor logic), ECL (emitter-coupled logic), and CMOS (complementary metal oxide semiconductor) microcircuit families. It concludes with some general information on operational amplifiers.

Section 2 describes the symbology used on the individual data sheets in section 3, including the meanings of the various modifiers and qualifiers found within each logic symbol.

Section 3 contains the data sheets.

Appendix A is a glossary of microcircuit terminology used in this manual.

NOTE

The data sheets in section 3 incorporate the latest CDC-approved symbology. As such, some of the symbols may be at variance with those found in the logic diagrams sections of less-recent product support manuals. This in no way lessens the validity of the data sheets with respect to those earlier manuals.

SPECIAL NOTE TO READER

Despite every reasonable effort by us, a manual of this scope may contain errors, omissions, or ambiguities. To a very large extent, we depend upon feedback from the field to correct those situations. We urge you, therefore, to let us know about what you consider to be deficiencies in this manual. And the surest way to do that is to use the postage-paid comment sheet just inside the back cover.

CONTENTS

APPENDIXES

FIGURES

SECTION 1

GENERAL THEORY

GENERAL THEORY

INTRODUCTION

A microcircuit is an electronic circuit in a miniature package that performs a specific binary or linear function. Microcircuit complexity varies from a few logic gates to more than 100 gates on a single silicon chip. The term small-scale integration (SSI) is sometimes used to refer to a level of complexity of up to 12 logic gates. Medium scale integration (MSI) refers to circuits containing from 13 to 100 gates. Large scale integration (LSI) generally indicates circuits containing 100 or more gates. These gates may be interconnected within a microcircuit to form flip-flops, multivibrators, etc., which in turn are further interconnected, again within an individual microcircuit, to form registers, counters, coders/decoders, multiplexers/demultiplexers, etc. Thus it is possible for a microcircuit to provide simple gating functions (AND, OR, NAND, NOR) as in SSI, or to provide complex functions (registers, counters, arithmetic logic units, memories, etc.) as in LSI.

TRANSISTOR-TRANSISTOR-LOGIC (TTL)

TTL microcircuits provide small physical size and high performance-to-cost ratio. Reliability also improves because relatively few interconnections are necessary. Most TTL microcircuits are of the monolithic type. That is, a complete circuit or group of circuits is fabricated on a single silicon chip. Another type of microcircuit is the hybrid. Hybrid circuits consist of small discrete components mounted on a ceramic substrate. A metallization pattern on the substrate forms the interconnections. Hybrid circuits usually appear in relatively small quantities. Ordinarily, microcircuits cannot be opened for repair or trouble-shooting.

STANDARD TTL CHARACTERISTICS

There are five series of TTL circuits: Standard, Low-Power, High-Speed, Schottky-Clamped and Low-Power Schottky TTL circuits. These series are functionally identical except for propagation time and power consumption. All five series are compatible; circuits from any series can interface with any other series. These series are described under their individual headings further in this section. A circuit of a series normally drives 10 circuits of the same series. However, combining circuits of different series varies the output drive capability (fan-out) from 1 to over 50. Typical values of the essential characteristics for all series are:

	Min	Nom	Max
Supply voltage	+4.75	+5.0	+5.25
High output voltage	+2.4	+3.3	
Low output voltage		+0.2	+0.4
High input voltage	+2.0	+3.3	
Low input voltage		+0.2	+0.8

The logic levels may be observed as indicated below, depending on the circuit load:

HIGH - from +2.0 to +3.3 volts.

LOW - from +0.2 to +0.8 volts.

TRI-LEVEL CIRCUITS

Tri-Level (tristate) circuits are similar to conventional TTL circuits. In addition to the normal high or low, tri-level circuits have a special control input that places the output of the circuit into an "off" (high impedance) state. In the off state, the circuit effectively disconnects from the output line. This characteristic is useful in a bus or party-line application where a number of driving circuits connect to a common transmission line, but only one circuit is active at any given time. A tri-level circuit draws significantly less input current when it is in the "off" state.

OPEN COLLECTOR CIRCUITS AND WIRED LOGIC

Some TTL microcircuits have an open-collector output. That is, the collector load or active pull-up portion of the ouput is not present. The output pin of the package connects only to the collector of an npn transistor. An open-collector output can go low only. It cannot drive the input of a following circuit high. To operate properly, an open-collector output must connect to an external pull-up resistor tied to Vcc.

More than one open-collector output may connect to the same pull-up resistor to form wired logic. This is sometimes called "collector dotting". Figure 1-1 illustrates open-collector circuits and a wired - AND gate. Each gate accomplishes the NAND operation for active-high inputs, and the NOR operation for active-low inputs. The expression for the function performed at the wired output is $Y = \overline{AB+CD}$ or $\overline{Y} = AB+CD$. Although sometimes referred to as "wired - OR" or "dot - OR", "wired - AND" is the correct description of the logic performed by this circuit.

UNUSED INPUTS

Generally unused inputs of TTL microcircuits are terminated in one of the following methods:

- Unused inputs are connected to used inputs if this does not exceed the fan-out of the driving output,
- unused inputs are connected to Vcc through a 1 kΩ resistor. The resistor protects the input from transients. Up to 25 inputs may be connected to one 1 kΩ resistor,
- unused inputs are connected to the output of an unused gate. This output must always be high.
- Unused inputs are connected to a separate supply voltage between 2.4 V and 3 V.

Leaving unused inputs open degrades the switching and noise characteristics of TTL microcircuits.

DUALITY OF FUNCTION

Figure 1-2 shows the four basic TTL gates (NAND, NOR, AND, OR). As implied by the logic symbols and truth tables, each of the two inverting gates may be considered as performing either the NAND function or the NOR function, depending upon which of the input states (high-or low-level) is regarded as being more significant-- that is, "active". Likewise, the two non-inverting gates can perform either the AND or the OR function, depending upon the polarity of the active inputs.

This principal of duality applies to all of the microcircuit families, not just to TTL. Later in this manual, these symbols are used in either representation to illustrate the logical construction of more complex circuits. When each of these composite circuits is constructed a new symbol is generated. These symbols are then used to construct yet a more complex circuit, such as flip-flops being used to construct registers, counters, etc.

BASIC TTL CIRCUITS

Generally, all TTL microcircuits are derived by using combinations of the four basic (or "standard") gates shown on figure 1-2. These standard gates may be modified in various ways to meet the requirements for faster switching speed or lower power consumption. The several "series" thus produced are differentiated as follows:

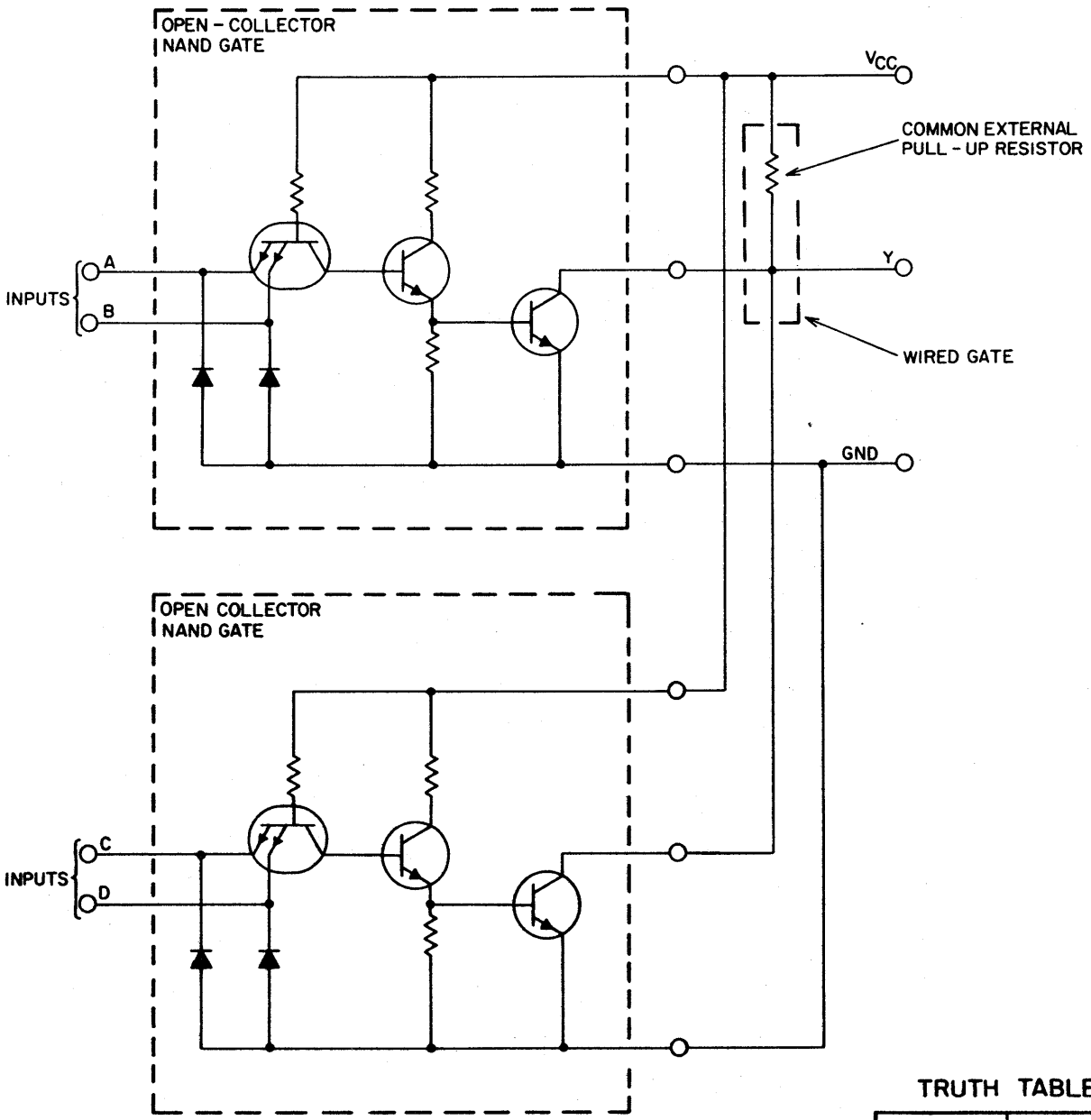
- XXX = Standard series
- XXXL = Low-Power series
- XXXH = High-Speed series
- XXXS = Schottky Clamped series
- XXXLS = Low-Power Schottky series

The following paragraphs describe the characteristics of each series. Electrical schematic diagrams are included to show how the standard NAND gate (depicted at the top of figure 1-2) is modified for each series. The other basic gate types would, of course, undergo similar alterations.

Standard Series

Because of the effect of capacity, decreasing the impedance of a circuit tends to make the circuit switch faster. However, decreasing the circuit impedance also tends to increase power consumption. The Standard Series TTL attempts to compromise speed and power requirements. Typical switching speed is 10 ns. Power consumption is 10 mW per gate. The standard-series NAND gate, shown it the top of figure 1-2, operates as follows: If one or both inputs are low, Q1 conducts, bringing the base voltage of Q2 close to ground. Q2 turns off, causing Q3 to be off and Q4 to be on. Thus, the output is high. If both inputs are high, the base-collector junction of Q1 is forward biased. This allows current to flow through R1 into the base of Q2 turning Q2 on. When Q2 is on, base current flows into Q3, and it turns on, causing the output to be low.

The multiple-emitter input transistor, Q1, replaces combinations of resistors, diodes, and transistors found in other types of logic. This configuration results in smaller size, which reduces stray capacity. Low stray capacity and low circuit impedances help to increase switching speed. At the output, Q3 and Q4 form an active pull-up or totem pole drive circuit. When the output is low, Q3 is saturated, providing a low source impedance. If the output is



TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H

X = IRRELEVANT

9K I A

Figure 1-1. Open-Collector Circuits and a Wired AND

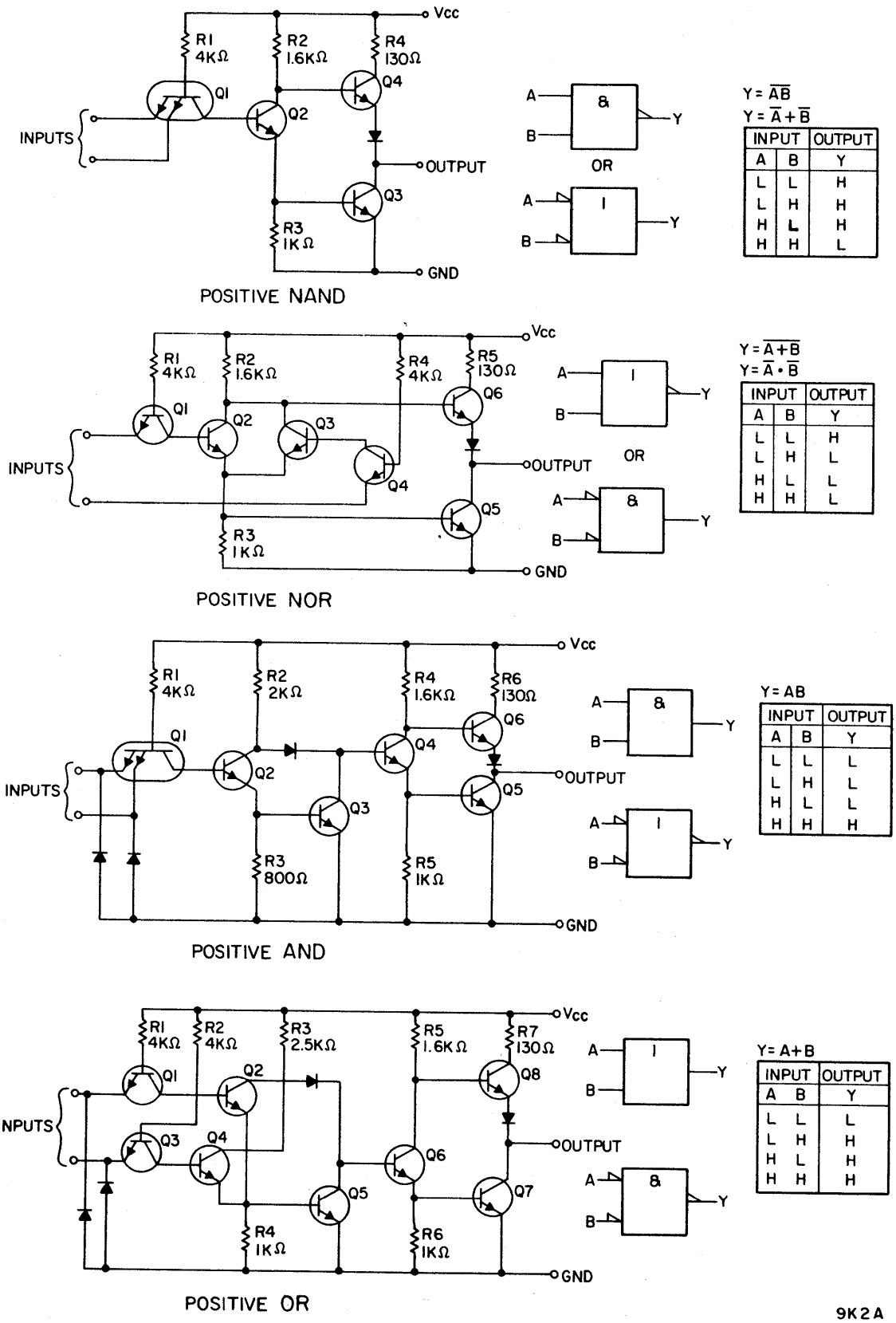


Figure 1-2. Basic TTL Gates

high, Q4 acts as an emitter-follower that also provides a low source impedance. This arrangement permits driving several loads and reduces the effect of capacity on switching time.

Low-Power Series

The low-power gate circuit is shown in figure 1-3. Typical switching speed is 33 ns, and power consumption is 1 mW per gate. Generally, an L suffix on the element identifier number indicates the low-power series.

High-Speed Series

Figure 1-4 shows the basic high-speed gate. Typical switching speed is 6 ns. Power consumption is 22 mW per gate. Usually, an H suffix on the element identifier indicates the high-speed series.

Schottky Clamped Series

Figure 1-5 shows the basic Schottky series gate. This series uses Schottky-barrier diodes as base-collector clamps. Clamping the collector prevents a transistor from saturating and thereby improves switching time. Switching time is 3 ns and power dissipation is 20 mW per gate. An S suffix on the element identifier indicates the Schottky series.

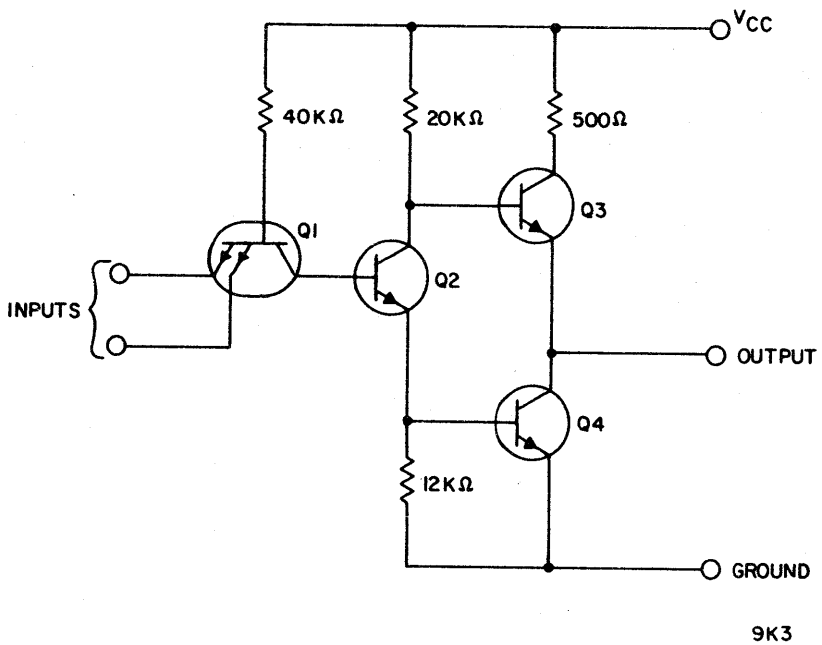


Figure 1-3. TTL NAND Circuit, Low-Power Series

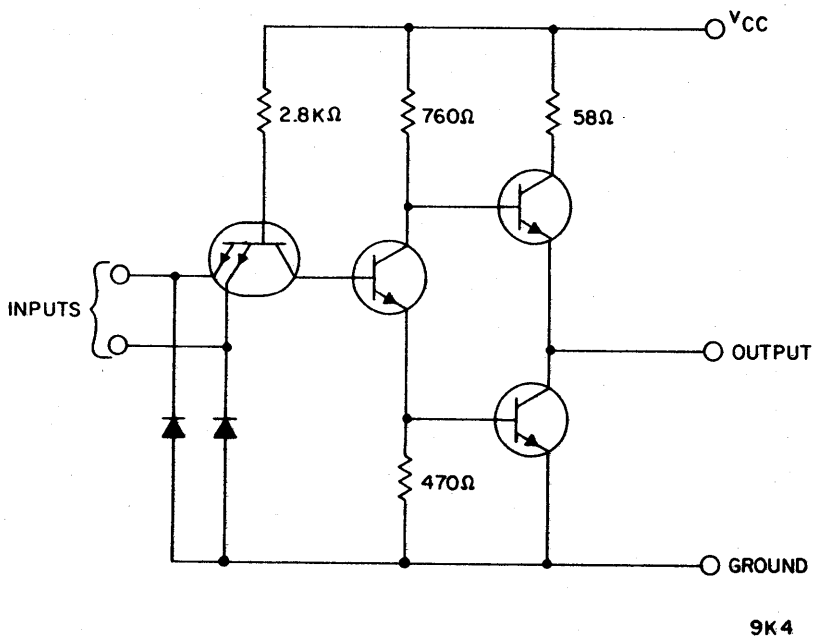
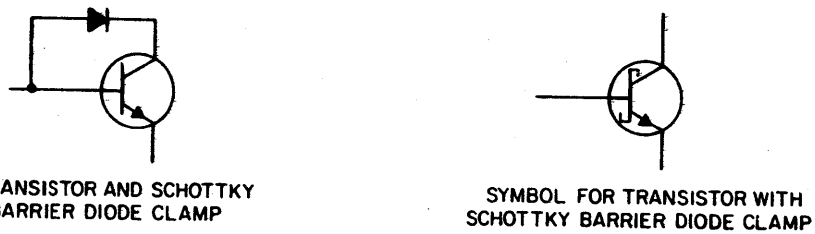


Figure 1-4. TTL NAND Circuit, High-Speed Series



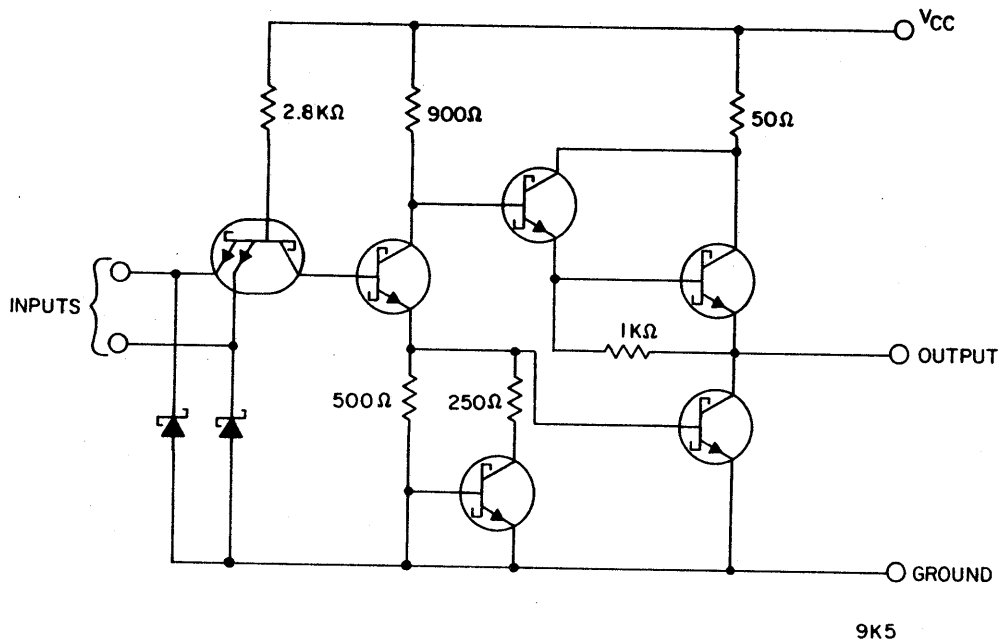


Figure 1-5. TTL NAND Circuit, Schottky Series

Low-Power Schottky Series

The low-power Schottky gate is shown in figure 1-6. The suffix letters LS on the element identifier denote this series of microcircuit. The LS series offers a happy substitute for the standard TTL microcircuits, and in fact enjoys the best speed-power product of any of the five TTL series. Switching time is typically 9.5 ns per gate (as against 10 ns for the standard series), while power dissipation is 2 mW per gate as opposed to 10 mW for the standard TTL gate.

LOGIC INTERFACE CIRCUITS

Special microcircuits are used to interface different families of microcircuits. In the case of interfacing TTL (logic levels of HIGH = +3.3 volts, LOW = +0.2 volt) to ECL (logic levels of HIGH = -0.5 volt, LOW = 1.75 volts), circuits such as illustrated in figure 1-7 are used.

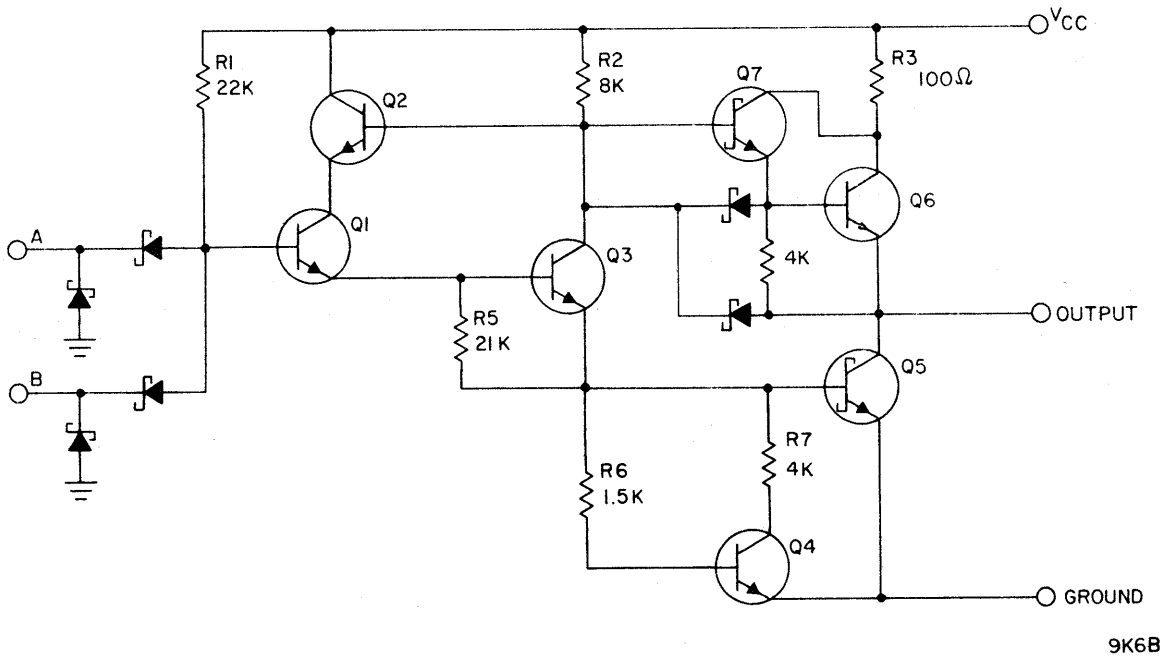


Figure 1-6. TTL NAND Circuit, Low-Power Schottky Series

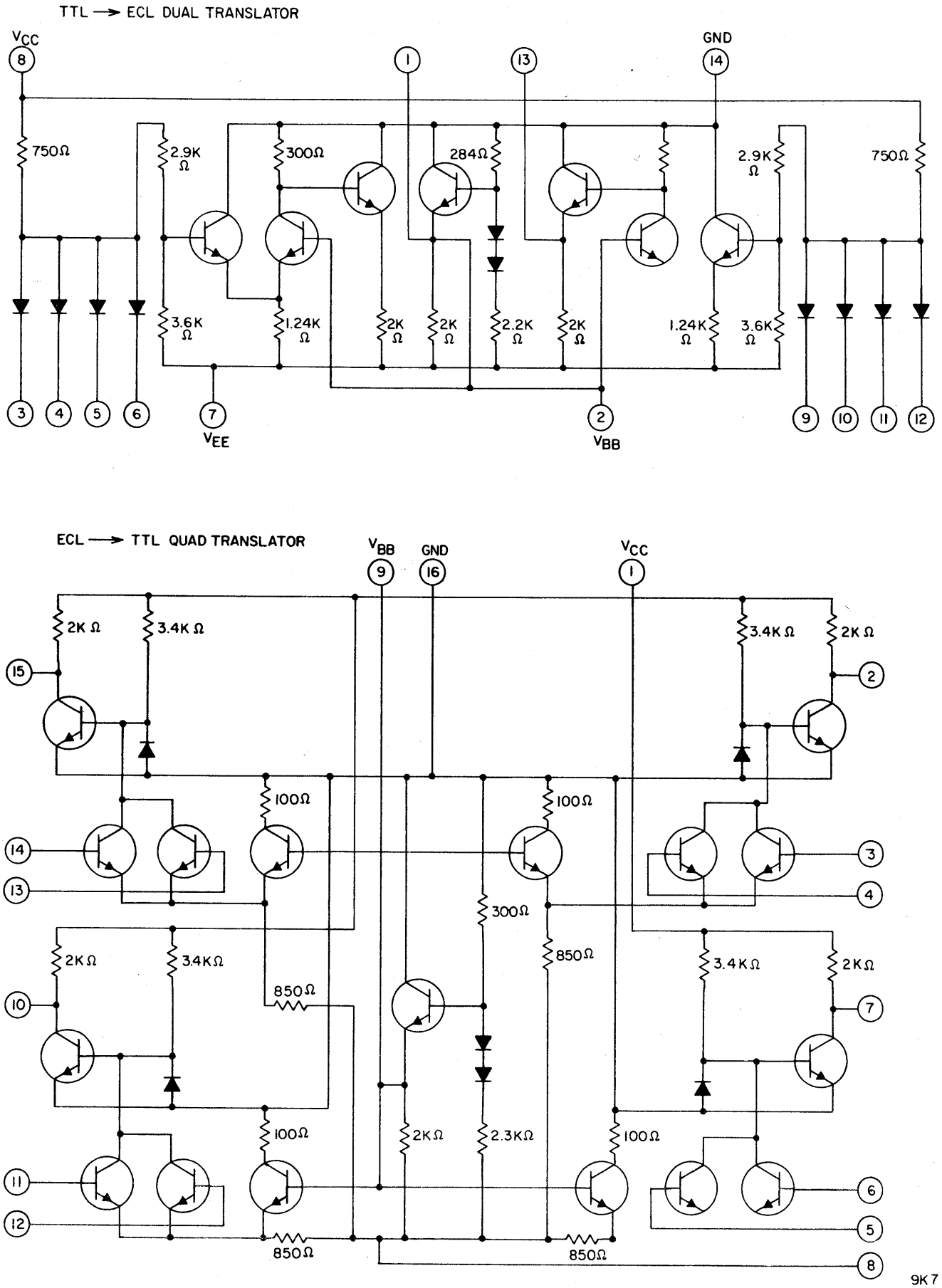


Figure 1-7. TTL/ECL Interface

TTL PACKAGING

TTL microcircuits are manufactured in several physical configurations. Three common ones are the dual-in-line packages, flat packages, and plug-in packages. These units are hermetically sealed and have from 8 to 40 pins. Flat packages and plug-in packages are available with various numbers of leads. Figure 1-8 shows an example of each package.

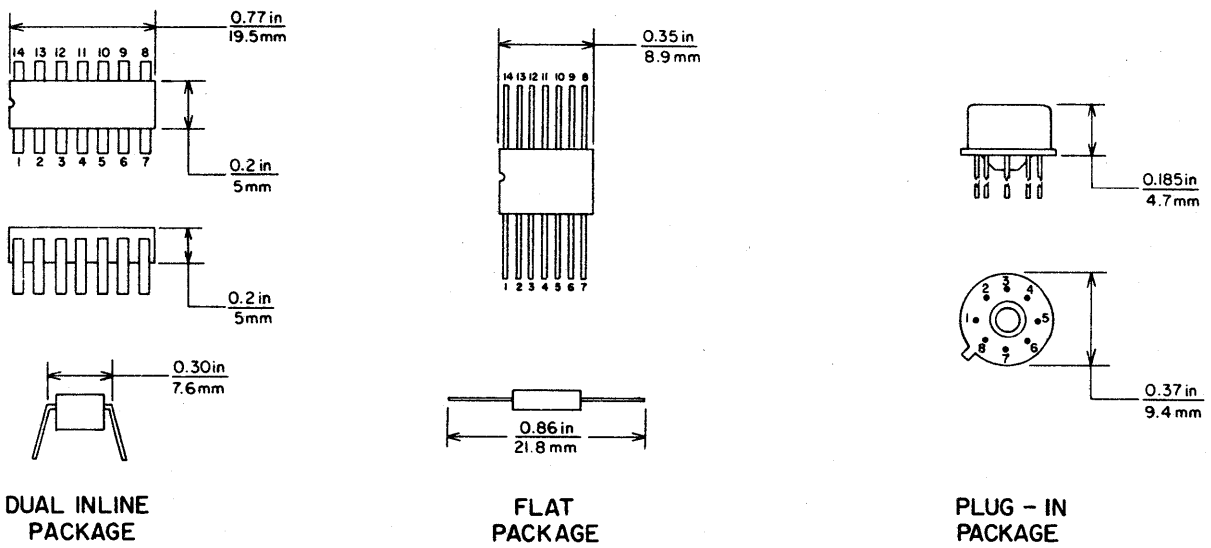


Figure 1-8. Typical TTL Packaging

EMITTER-COUPLED-LOGIC (ECL)

The emitter-coupled-logic (ECL) microcircuit is, by design, nonsaturating, and therefore avoids transistor storage time and its attendant speed limitation, characteristic of transistor-transistor logic (TTL). The high speed of ECL microcircuits has either or both of two characteristics; switching rates of over 50 megahertz and/or gate propagation delays of less than 6 nanoseconds. In general, the gate propagation delays of ECL logic are approximately 2 nanoseconds.

Some of the salient features of ECL microcircuits are as follows:

- High input impedance/low output impedance properties enable large fanout and versatile drive characteristics.
- Minimal power supply noise generation due to differential amplifier design.
- Nearly constant power supply current drain.
- Minimal crosstalk due to low-current switching on signal path.
- Low on-chip power consumption (e.g., less than 8 milliwatts in some complex function chips)
- No line drivers needed due to open emitter outputs of ECL
- Capability of driving twisted pair transmission lines of up to 1000 feet in length.
- Simultaneous complementary outputs available at logic element output without using external inverters.

LOGIC AND POWER LEVELS

	Nom	Min	Max
Supply voltage (V_{EE})	-5.2		
Noise immunity	*	*	*
High output voltage	-0.924	-0.96	-0.81
Low output voltage	-1.75	-1.65	-1.85
High input voltage		-1.105	
Low input voltage		-1.85	-1.475

*Noise immunity of a system involves line impedances, circuit output impedances, propagation delays, and noise margin specifications. Noise margin is a dc parameter calculated from specified points tabulated on an ECL data sheet for the particular microcircuit in question.

CIRCUIT THEORY

A typical ECL gate circuit is shown in figure 1-9 and consists of a differential amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower buffering transistors for transmission line driving. To explain operation of the gate, each of the major sections is discussed in the following paragraphs.

The differential amplifier is an emitter-coupled current switch consisting of transistors Q1 through Q5. The multiple gate inputs provide an OR function (Q1 through Q4) which is amplified by current switch Q5. To understand the gate's operation, assume that all gate inputs are low (-1.75 V and Q1 through Q4 therefore cutoff). Under this condition, Q5 is forward biased, the base being held at -1.29 volts by the bias supply voltage (V_{BB}), and its emitter is at one diode voltage drop (0.8 V) more negative than its base (-2.09 volts total). The base-to-emitter differential then becomes the difference between the low logic level (-1.75 V) and V_{BB} (-1.29 V), or 0.34 volt. Since this voltage is less than the threshold voltage to turn Q1 through Q4 on, they remain in the cutoff state. The current through Q5 will be about 4 milliamperes with a voltage of -2.09 volts at the emitter nodes of Q1 through Q4 using an emitter resistor R_E of about 780 ohms.

The emitter-follower outputs buffer the current switch from loading and restore output voltages to proper ECL levels. The OR output is obtained through Q8 producing the low-level logic signal of -1.75 volts. Similarly, the NOR output is obtained through Q7 producing the high-level logic signal of -0.924 volt.

When any or all of the logic inputs is switched to the high logic level, the appropriate input transistor turns on, a current flows through resistor RC1 in the differential amplifier, and transistor Q5 cannot sustain conduction due to forward biasing, so is cut off. After translating through the emitter followers, the NOR output is a nominal -1.75 volts and the OR output a nominal -0.924 volt.

The differential action of the switching transistors (one section off when the other is on) produces simultaneous complementary signals at the output.

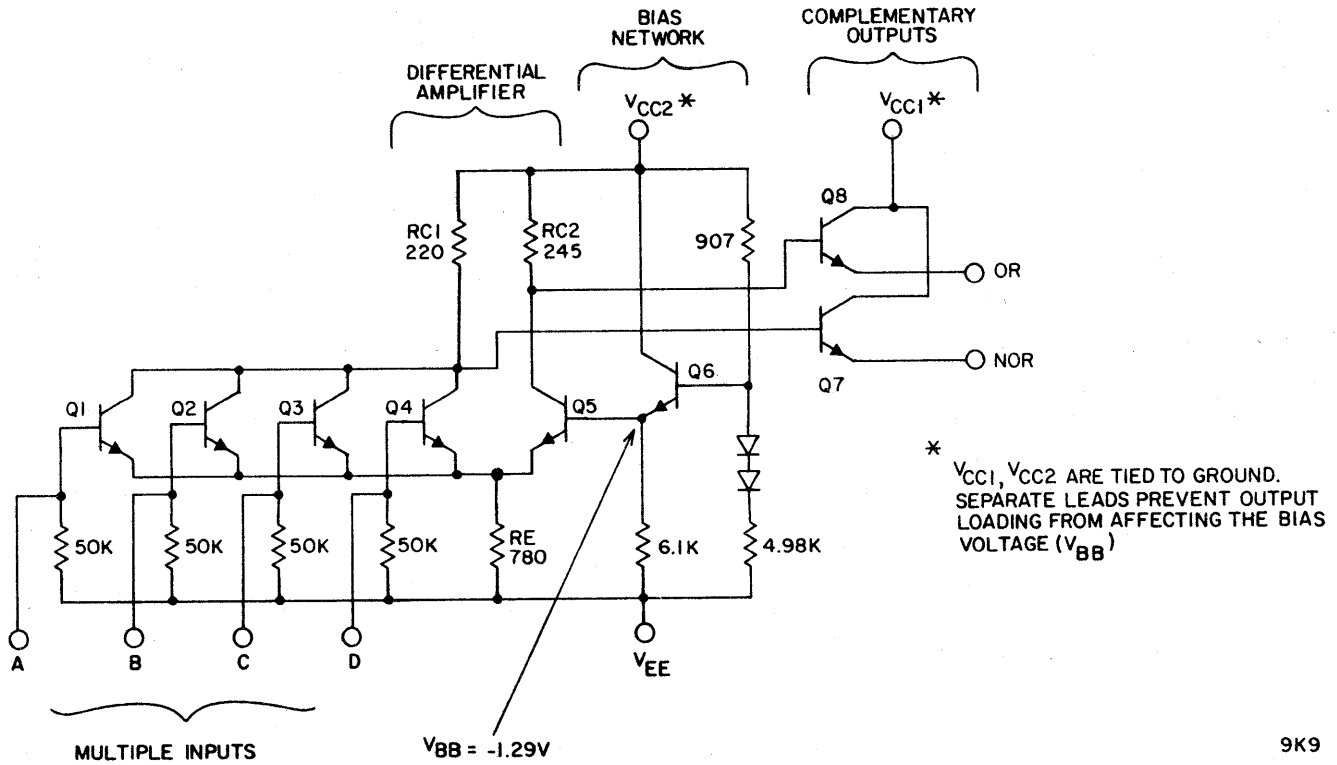


Figure 1-9. Typical ECL Gate

The bias network provides a reference voltage (V_{BB}) of -1.29 volts. This network compensates for variations in power supply voltage and temperature changes to ensure that the bias voltage threshold point remains in the proper operating region.

LOADING CHARACTERISTICS

The differential input to ECL circuits offers several advantages. Its common mode rejection feature offers immunity against power supply noise, and its relatively high input impedance enables any circuit to drive a large number of gate inputs without deterioration of noise margins. The dc loading factor (the number of gate inputs of the same family that can be driven by a circuit output) for ECL circuits is 90. While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit, and therefore affects circuit speed. For ECL circuits, best performance at fanouts of greater than 10 will occur with the use of transmission lines. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance (Z_o) of the transmission line itself are affected by the distributed capacitance and loading due to stubs off the line. Maximum allowable stub lengths for loading of an ECL transmission line vary with line impedance. For example, a transmission line with a Z_o of 50 ohms will accept stubs 4.5 inches (114.3 mm) long. When the Z_o of the line is changed to 100 ohms, stubs may be only 2.8 inches (71.1 mm) long.

The input loading capacitance of an ECL 10109 is 2.9 picofarads. Therefore, fanouts in a non-transmission line environment should be limited to a maximum of 10 loads due to line delay increases which in turn limit speed.

UNUSED INPUTS

The input impedance of the differential amplifier used in the typical ECL circuit is high when the applied signal level is low. Under low signal conditions, any leakage to the input capacitance of the gate may cause a gradual buildup of voltage on the input lead, thereby adversely affecting switching characteristics at low repetition rates. All but a few of the ECL circuits contain input pull-down resistors between the input transistor bases and the -5.2 volt power supply (V_{EE}). Therefore, unused inputs may be left unconnected because leakage current is dissipated by the resistor, keeping inputs sufficiently negative so that circuits will not trigger due to noise coupled into those inputs.

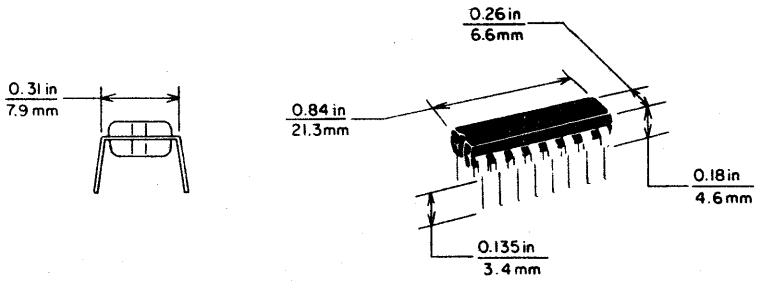
Input pull-down resistors must not be used as pull-down resistors for preceding open-emitter outputs. If an ECL circuit (such as the 10116) does not contain input pull-down resistors, one input of a circuit must be connected to the reference bias supply voltage (V_{BB}) and the other input to V_{EE}.

WIRED LOGIC

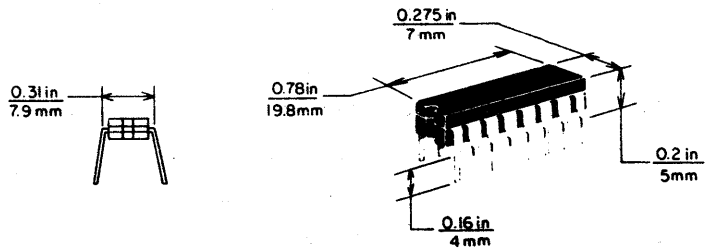
Wired-OR gates can be produced in ECL microcircuits by wiring output emitters together (to a maximum of 10) outside their respective packages. Wired-OR gates can be connected directly to a bus, also. Propagation delay is increased by approximately 50 picoseconds per wired-OR gate. To economize on power dissipation, a single output pull-down resistor is used per wired-OR gate. Normally, wired-OR gates are connected between gates on the same logic board.

ECL PACKAGING

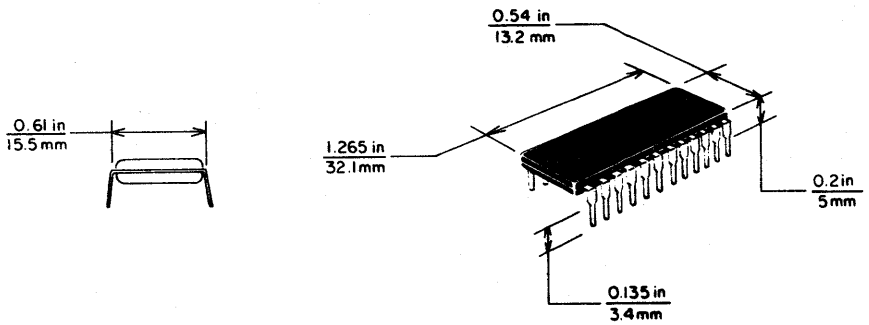
ECL microcircuits are manufactured in a variety of physical configurations. Two of the more common ones used for the ECL microcircuits described in this manual are the ceramic dual in-line and the plastic dual in-line cases having both 16 and 24 pins, depending upon the size of the package. Figure 1-10 illustrates these packages.



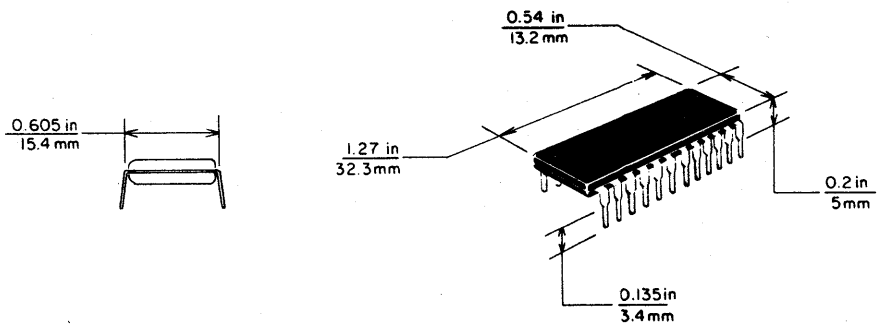
16-PIN DUAL INLINE PLASTIC (CASE 648)



16-PIN DUAL INLINE CERAMIC (CASE 620)



24-PIN DUAL INLINE PLASTIC (CASE 649)



24-PIN DUAL INLINE CERAMIC (CASE 623)

9K 10

Figure 1-10. Typical ECL Packaging

COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (CMOS)

CMOS microcircuits use four-terminal, enhancement-type field effect transistors (FETs), the symbol for which is given in figure 1-11, to form the basic inverter.

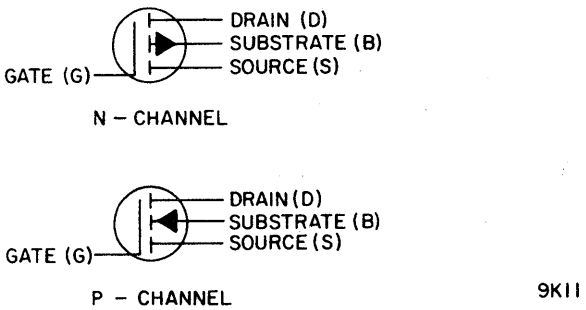


Figure 1-11. FET Symbol

As shown in figure 1-12, a complementary inverter may be formed by applying the input signal to the gates of two opposite-polarity FETs.

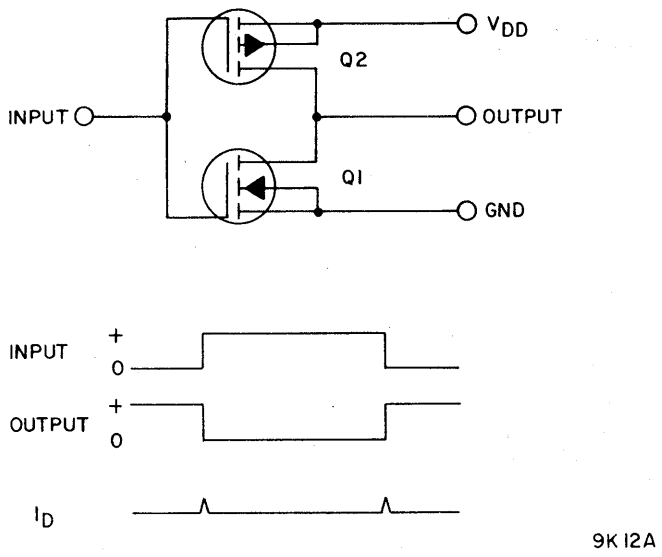


Figure 1-12. Typical CMOS Inverter

In this circuit, a low input signal turns the N-channel transistor Q1 off, and turns the P-channel transistor (Q2) on. The output is shorted to the positive supply, but virtually no load current is drawn if the load is assumed to be another CMOS device with high-impedance input. When the input signal goes high, Q1 is turned on and Q2 is turned on. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the circuit is thus limited to the crossover points as the device changes state, and with proper design is typically 2 nanowatts per gate.

ADVANTAGES/DISADVANTAGES

Advantages

- High circuit density
- High noise immunity
- Lower power dissipation (2.5 nW per gate, typical)
- High fan-out to other CMOS elements (>50)
- Logic swing independent of fanout
- Input threshold is constant over wide temperature range (5% variation, typical)

Disadvantages

- Fabrication complex and more costly than TTL or ECL
- Buffering required when driving several TTL loads
- Level translation required when driving ECL loads
- Characteristic complementary output configuration precludes use of "wired OR" schemes.
- Inputs extremely electrostatic sensitive -- require special precautions when handling.

OPERATING VOLTAGES

An additional advantage of the CMOS family is its wide range of operation voltage (V_{DD}), which may vary from 3 V dc to 16 V dc although, as is shown later, operating

speed suffers for the lower supply voltages. Noise immunity is typically 45% of the supply voltage. The range of input and output voltages is shown below for a Vcc of +5 V.

	Min	Nom	Max
High output voltage	4.99	5.0	-
Low output voltage	-	0	0.01
High input voltage	3.5	5.0	-
Low input voltage	-	0	1.5

INPUT PROTECTION NETWORK

CMOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide region. Any potential over about 100 V between the gate and the substrate breaks down the oxide, resulting in permanent damage. The input protection network shown in figure 1-13 protects the CMOS against voltages in the hundreds region, which is normally sufficient for ICs mounted on a circuit card that is already plugged into a logic-chassis connector. When removing, replacing, shipping, or otherwise handling these electrostatic-sensitive cards, special precautions should be observed to prevent static buildup between the handler and the card. These precautions are outlined in the maintenance manual for any equipment using such cards. The CE is strongly advised against attempting to remove and replace CMOS ICs on these cards; adequate measures to avoid harmful electrostatic discharges during such repair procedures are simply not realizable in the field.

The diode-resistor input protection network shown in figure 1-13 is built into every external input lead as part of the fabrication process. The circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and ground, respectively. (The protection network is not usually shown in CMOS electrical schematic diagrams.)

The series isolation resistor, RS, is typically 1500 ohms. Diodes D1 and D2 clamp the input voltages between Vcc and ground. Diode D3 is a useful parasitic structure resulting from the diffusion fabrication of RS. The 6 to 7 ns delay of RS allows excess energy present at the input pin to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) over-voltage protection, with respect to ground when V_{DD} is open, is provided by D1.

Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) protection with respect to V_{DD} when ground is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric. The avalanche characteristic of D3 and D4 is typically 120 V.

REPRESENTATIVE CMOS GATES

Figure 1-14 contrasts a 2-input NAND with a 2-input NOR. The dashed-line boxes enclose the output buffer that is usually a part of the gate. Buffering achieves high performance, standardized output drive, highest noise immunity, and decreased sensitivity to output loading.

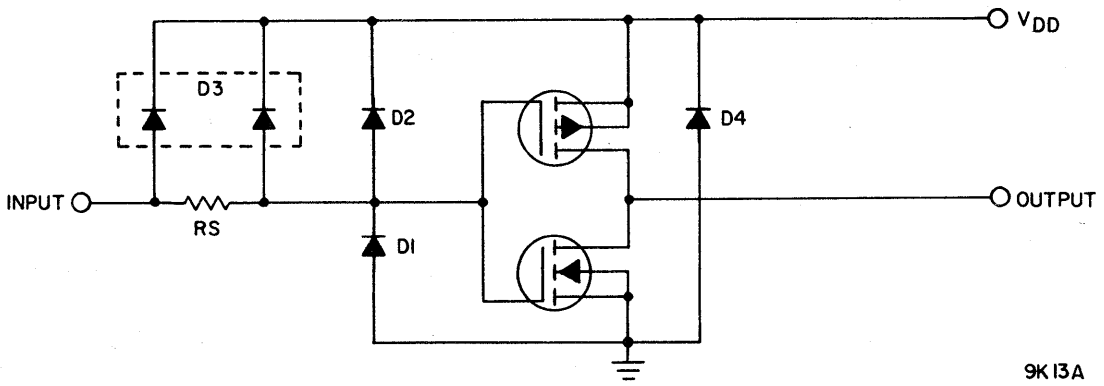


Figure 1-13. Diode-Resistor Input Protection

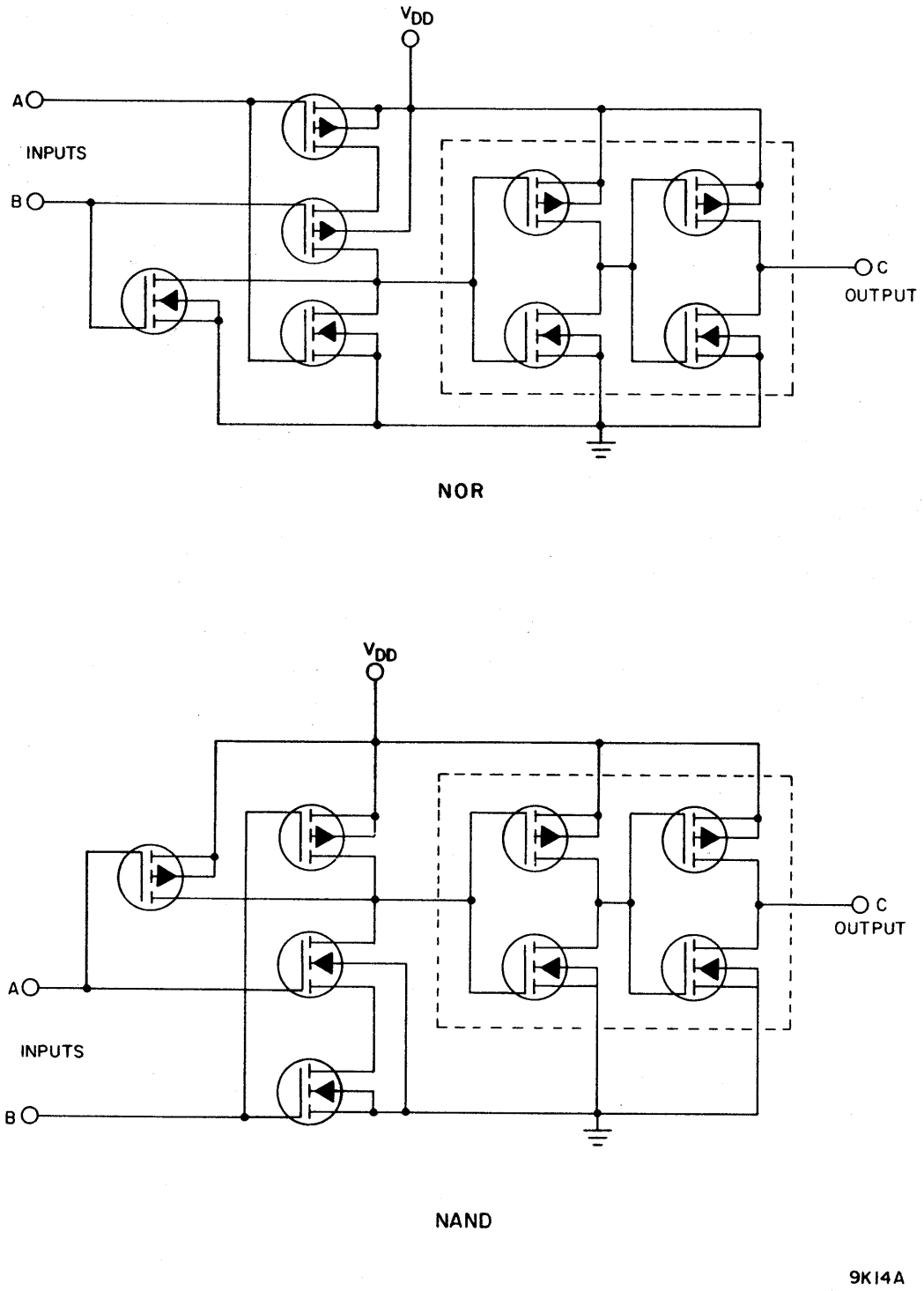


Figure 1-14. Typical CMOS Gates

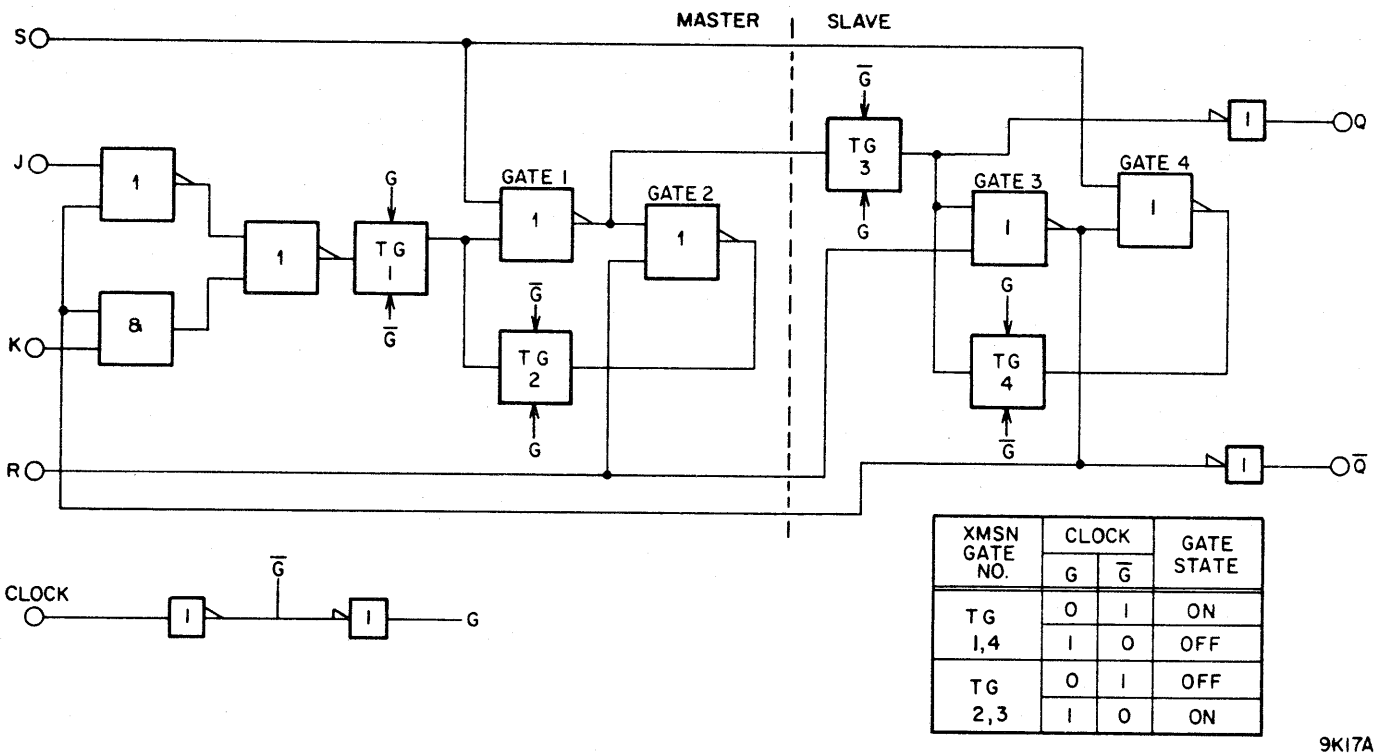
TRANSMISSION GATE

The transmission gate (TG) is a valuable tool in CMOS design. Two representations of the gate, as found in vendor literature, are shown below. The symbol on the left is used in functional diagrams in this manual.

The two control inputs, one on the top and the other on the bottom of the symbol, are most usually fed complementary signals. A high on the top control input turns the gate off; a high on the bottom control input turns the gate on.

A typical use of the transmission gate is shown in figure 1-15, which depicts a positive-edge-triggered J-K master-slave FF (circuit 4027). Here, four transmission gates are controlled by complementary clock signals (G, $\overline{G}$). When the clock is low, TG1 and TG4 are on, while TG2 and TG3 are off. This logically disconnects the Master from the Slave. Gates 3 and 4, however, are cross-coupled through TG4 (which is on), and the output state remains stable. Assuming that the S and R inputs are inactive, TG1 transmits the state of the J and K inputs to Gates 1 and 2.

When the clock goes high, TG2 and TG3 turn on, while TG1 and TG4 turn off. Now gates 1 and 2 are cross-coupled through TG2, and latch into the state they held when the low-to-high clock transition took place. With TG3 on, the logic state of the Master section (output of Gate 1) is fed through an inverter to the Q output. Simultaneously, the $\overline{Q}$ output receives the double inverted output of Gate 1.



XMSN GATE NO.	CLOCK G	CLOCK $\overline{G}$	GATE STATE
TG 1,4	0	1	ON
	1	0	OFF
TG 2,3	0	1	OFF
	1	0	ON

Figure 1-15. Use of Transmission Gates in J-K Flip-Flop Circuit

OPERATING SPEED

Propagation delay and rise/fall times are functions of the device temperature, operating voltage, and output load capacitance. Delay and transition times increase approximately 1/4 of one percent for each degree Celsius above +25°C, and decrease approximately as the inverse of the operating voltage. For a given V_{DD}, the rise, fall, turn-on and turn-off times are about equal for a load capacitance of 15 picofarads and increase at different rates above that point. The table below gives representative figures.

DELAY/TRANSITION TIMES FOR VARIOUS OPERATING VOLTAGES

Time Measured	V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V			Units
	Load Capacitance									
	15	50	100	15	50	100	15	50	100	pF
Turn off/on	60	120	200	20	40	65	10	25	40	ns
Fall	60	130	220	30	60	110	20	40	70	ns
Rise	60	220	≈320	30	90	170	20	60	120	ns

UNUSED INPUTS

Unused CMOS inputs should be connected to an appropriate logic voltage, depending upon the function of the logic device. Unused NAND inputs should be connected to the +5 V bus, unused NOR inputs to ground. This prevents the input protection structure from floating to some undesired voltage level that prevents the device from functioning properly. In addition, "floating" inputs may be subjected to electrostatic potentials that will permanently damage the device.

CMOS/TTL INTERFACE

The majority of CMOS devices will not sink the 1.6 mA required for the logical zero input (+0.4 V) to a TTL device. The sinking capability is usually increased by using a 2- or 4-input NOR gate (CMOS) to drive the TTL input. For multiple TTL inputs, special CMOS buffers are used. Sourcing the µA-range needed for a TTL logical one is no problem for the CMOS device.

When converting from TTL to CMOS, it is important that the TTL output device does not source other TTL circuits, but only the CMOS input. (Sourcing 400 µA for a TTL logical one drops the TTL output to about 2.4 V, considerably below the 3.5 V CMOS threshold required for a logical one.) Sourcing the 10 pA for a CMOS logical one results in a TTL output of around 3.6 V. This is adequate, but provides little noise margin. For this reason, a 2000-ohm pull-up resistor is usually inserted between the TTL output and Vcc.

CMOS/ECL INTERFACE

The -5.2 V typical for an ECL supply is easily handled by a CMOS device. If higher negative voltages are advisable because of required CMOS speed, a diode clamp on each ECL input is required to prevent the input from going below the -5.2 V ECL supply.

Level translation is required when going from ECL to CMOS. The 800-mV output swing of an ECL device is not sufficient to drive a CMOS input, so a pnp transistor is used (figure 1-16). A diode in series with the transistor's emitter provides a reverse bias of about 900 mV, which is beyond the output voltage typical of an ECL logical one (-0.924 V). The transistor switches from about -0.9 V to -5.2 V, which is well within the -1.7 V typical for an ECL logical zero output.

CMOS PACKAGING

CMOS microcircuits are manufactured in dual-inline ceramic (DIC) and dual-inline plastic (DIP) packages with 14, 16, or 24 pins. Figure 1-17 shows the various packaging dimensions.

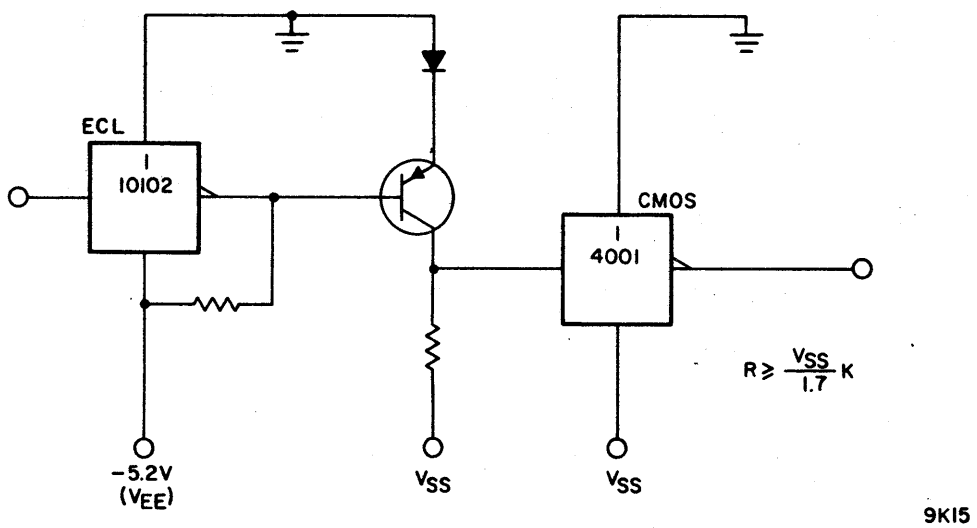
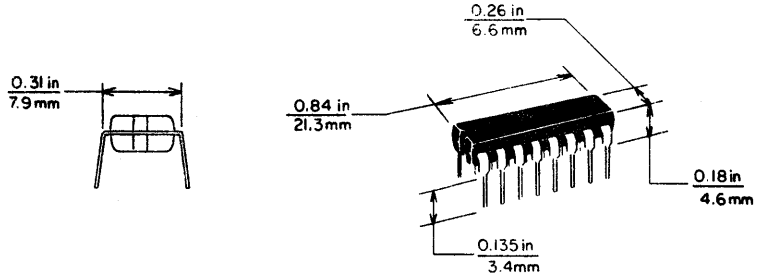
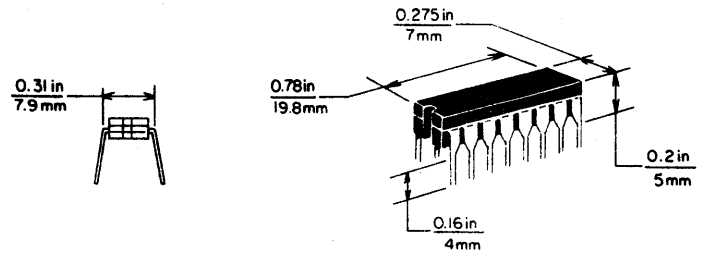


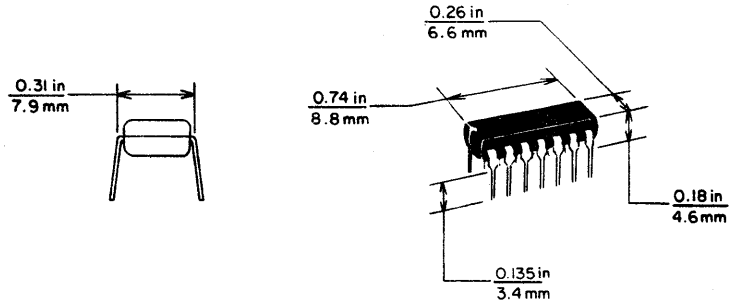
Figure 1-16. ECL-To-CMOS Interface



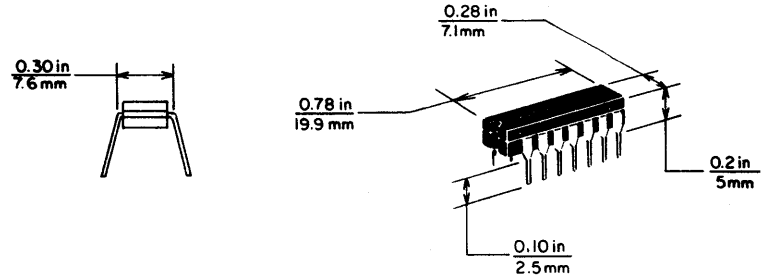
16-PIN DUAL INLINE PLASTIC (DIP) (CASE 648)



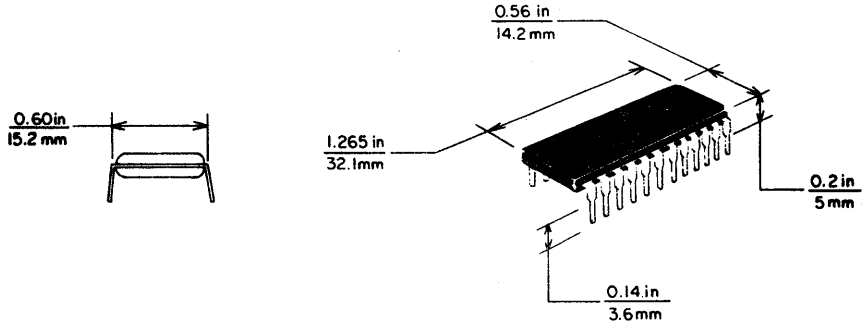
16-PIN DUAL INLINE CERAMIC (DIC) (CASE 620)



14-PIN DUAL INLINE PLASTIC (DIP) (CASE 646)

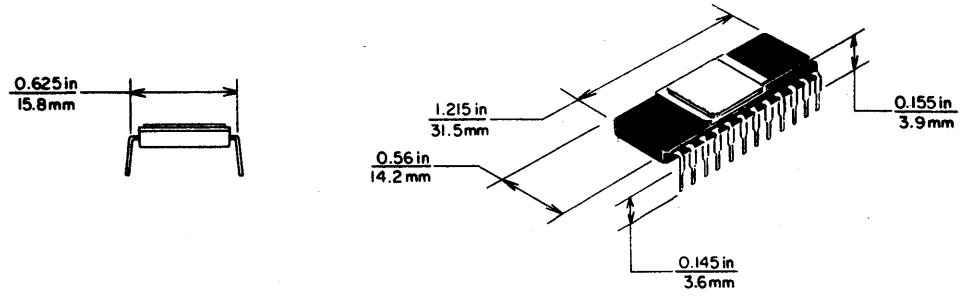


14-PIN DUAL INLINE CERAMIC (DIC) (CASE 632)



24-PIN DUAL INLINE PLASTIC (DIP) (CASE 709)

9K16-1



24-PIN DUAL INLINE CERAMIC (DIC) (CASE 684)

9K16-2

Figure 1-17. Typical CMOS Packaging

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can apply signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used frequently in a disk drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Zero offset: output is zero when input is zero
5. High bandwidth frequency response

BASIC CIRCUIT ELEMENTS

Figure 1-18 is a simplfied schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FETs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 mV are applied to the non-inverting input while 9 mV are applied to the inverting input, the 1 mV difference is amplified. The amplification, which may be a voltage gain of up to 100000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the common-mode input signal. In the preceding example, 9 mV is the common-mode input, while 1 mV is the differential input. In the ideal op amp, the output is zero with identical inputs; only the difference (1 mV in this case) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.

BASIC CIRCUIT FUNCTIONS

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; therefore it is assumed to be zero.
2. The differential voltage (V3) is insignificant and therefore is assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current (I1) entering the summing point must leave it (I2). These currents are:

$$I1 = V1/R1$$

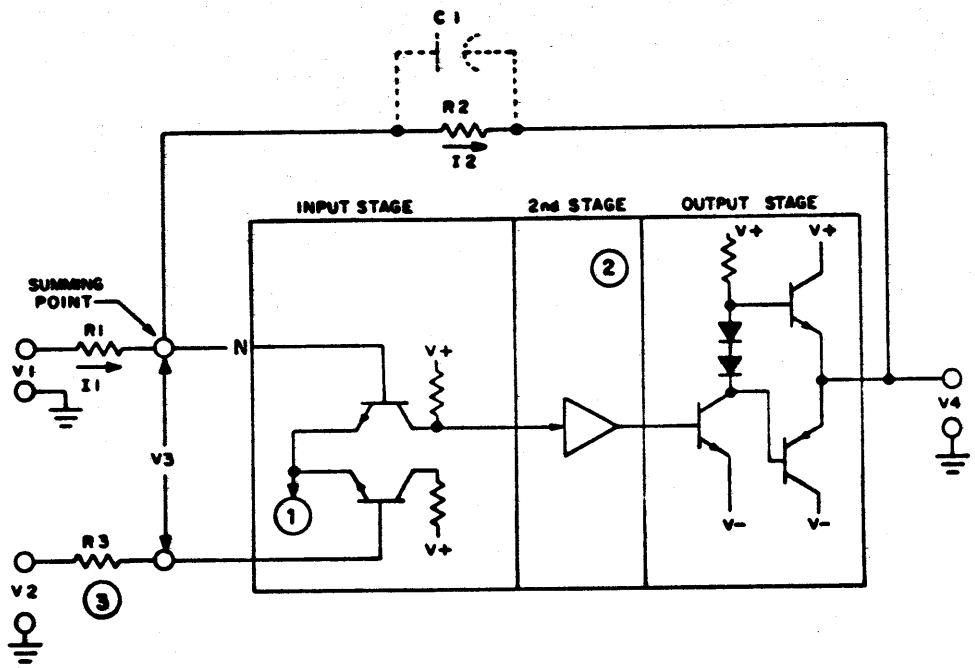
$$I2 = -V4/R2$$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohm's Law:

$$V4/V1 = -R2/R1 \text{ or } V4 = -V1\ (R2/R1)$$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, as frequency increases, the effective impedance of R2/C1 decreases to reduce overall gain.



NOTES;

1. TO COMMON CONSTANT-CURRENT SOURCE.
2. NOT APPLICABLE TO ALL TYPES. REFER TO MANUFACTURER'S DATA SHEET.
3. FOR BALANCED INPUT IMPEDANCE, $R3 = \frac{R1\ R2}{R1+R2}$

7J133A

Figure 1-18. Simplified Op Amp Schematic

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset; that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made equal, that is, the same input impedance is presented to both, they are therefore common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule 2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a virtual ground; that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

Typical op amp circuit functions are illustrated in figure 1-19.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (figure 1-20). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open-loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

Consider A376 of figure 1-20. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28 V. Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

As the input A goes more positive, the output does not change until A equals B (+1.28 V). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14 V available at Y, the voltage at B is reduced to +1.10 V. The input must now swing to less than +1.10 V for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

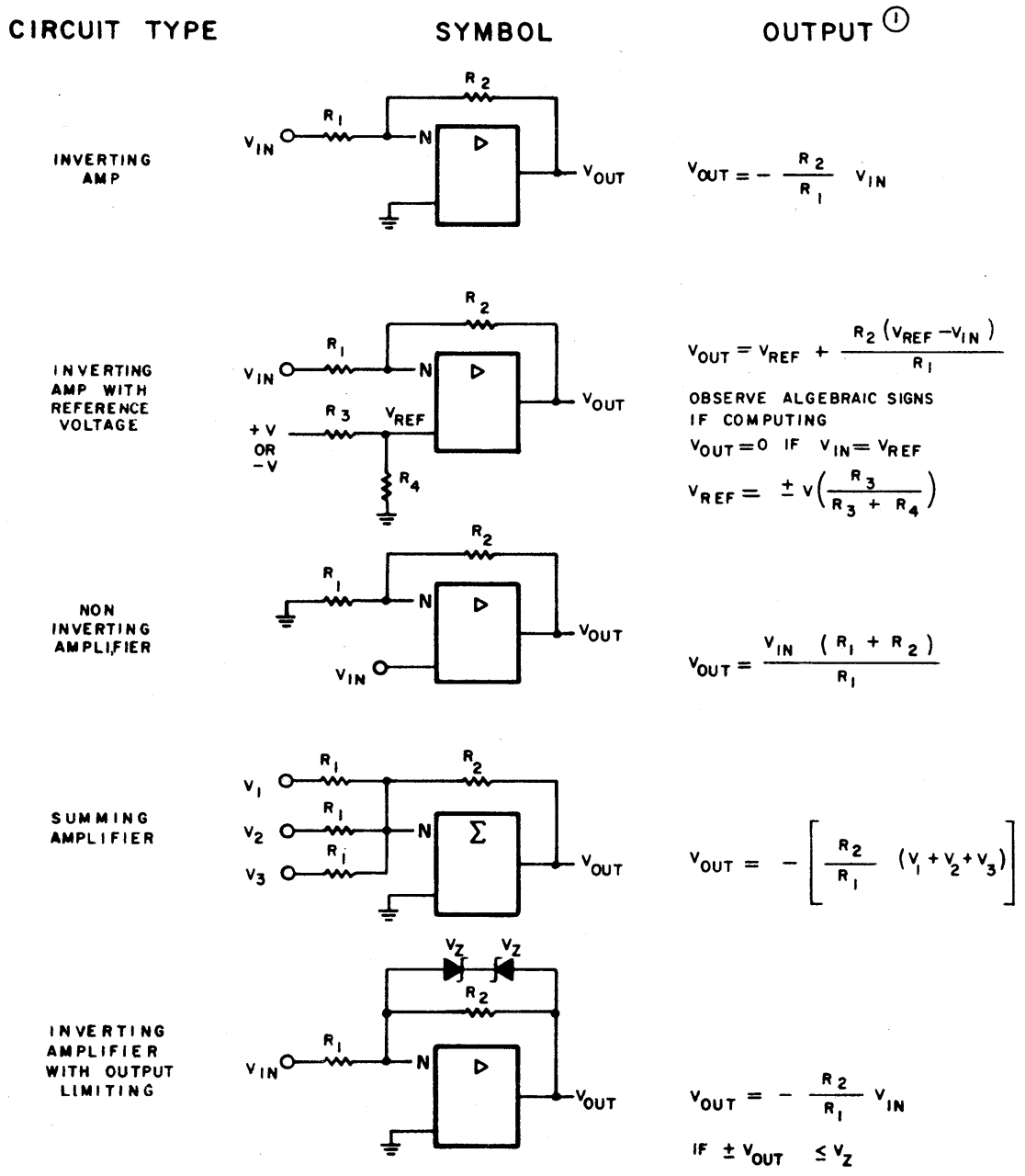


Figure 1-19. Op Amp Circuit Functions (Sheet 1 of 3)

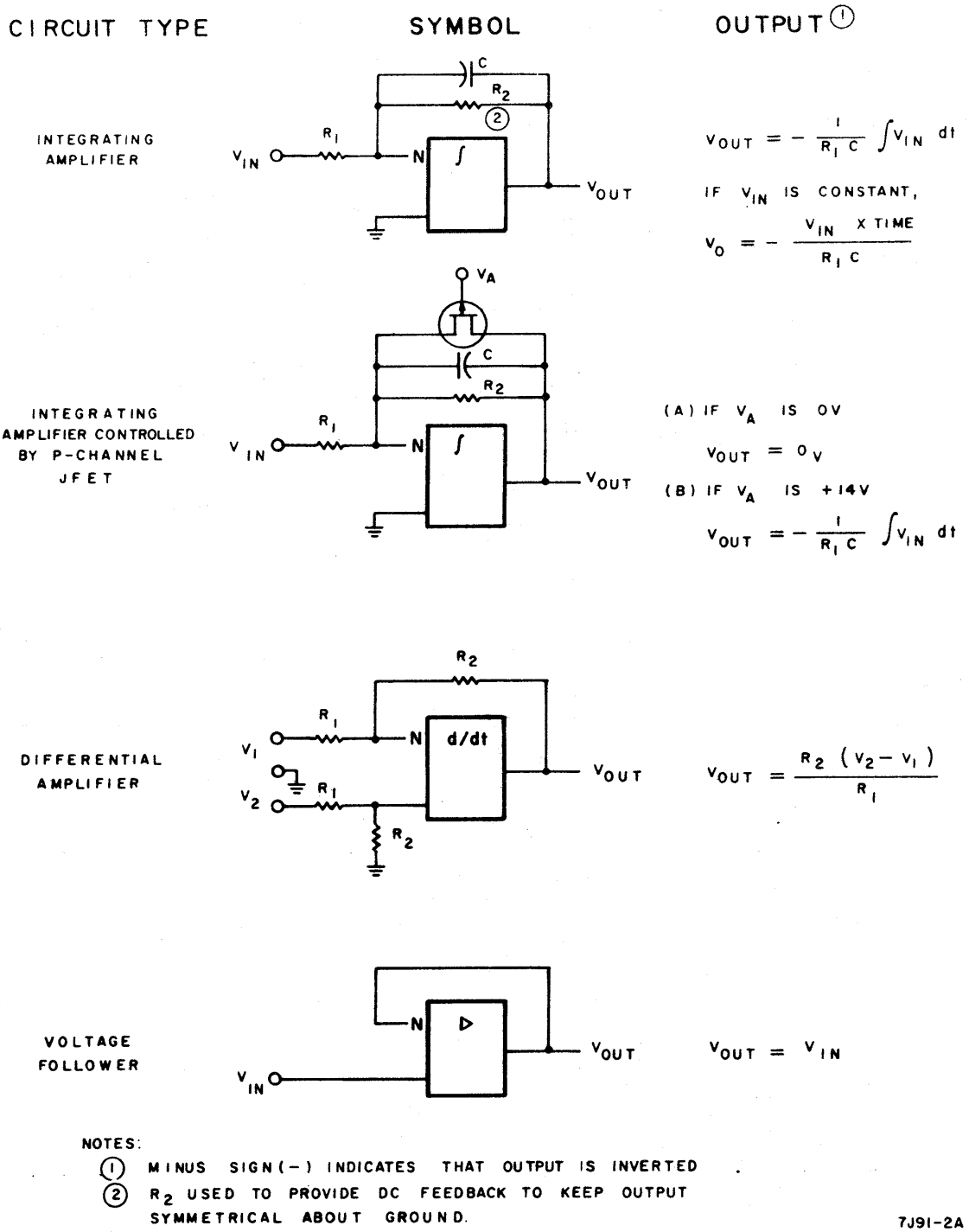
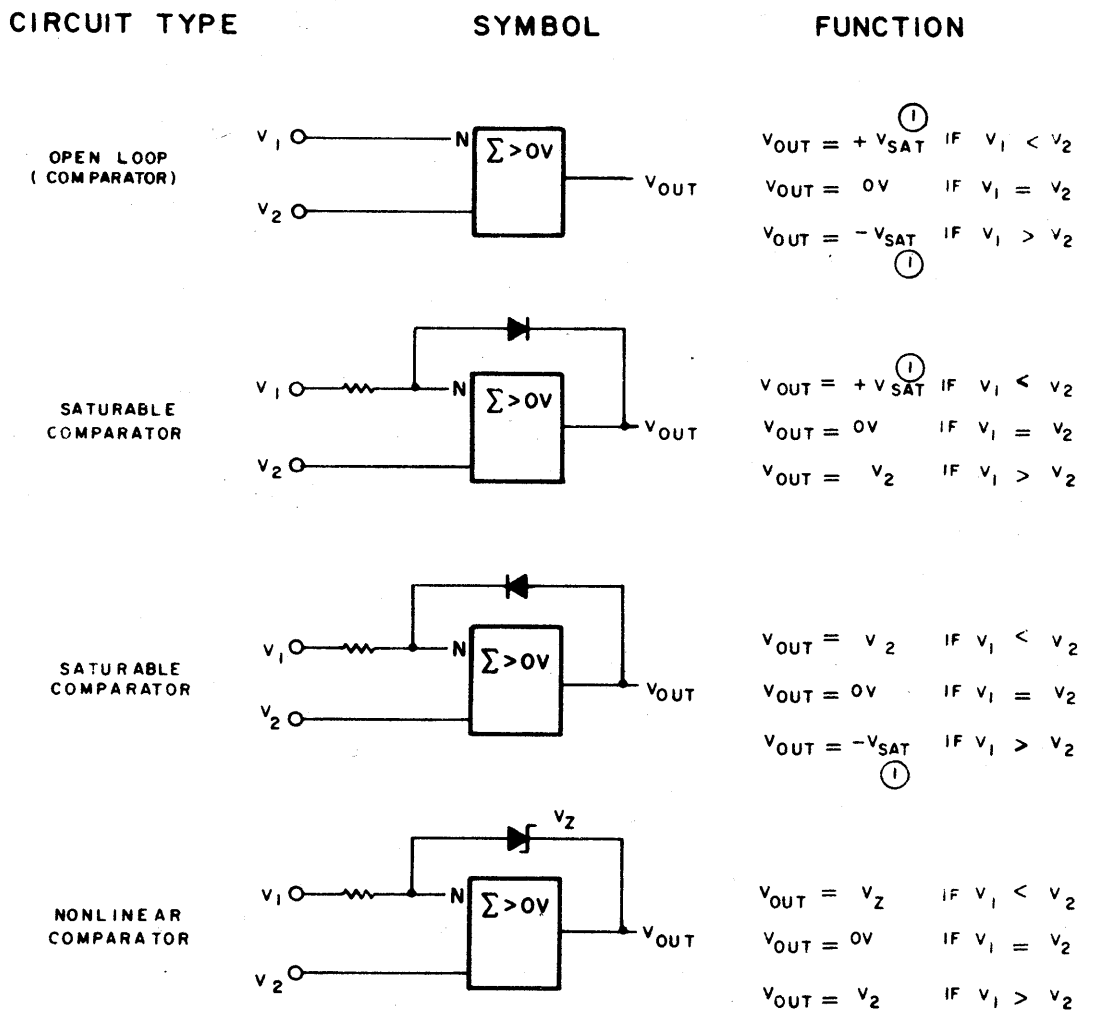


Figure 1-19. Op Amp Circuit Functions (Sheet 2 of 3)



NOTE:

(1) V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10{,}000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

7J91-3A

Figure 1-19. Op Amp Circuit Functions (Sheet 3 of 3)

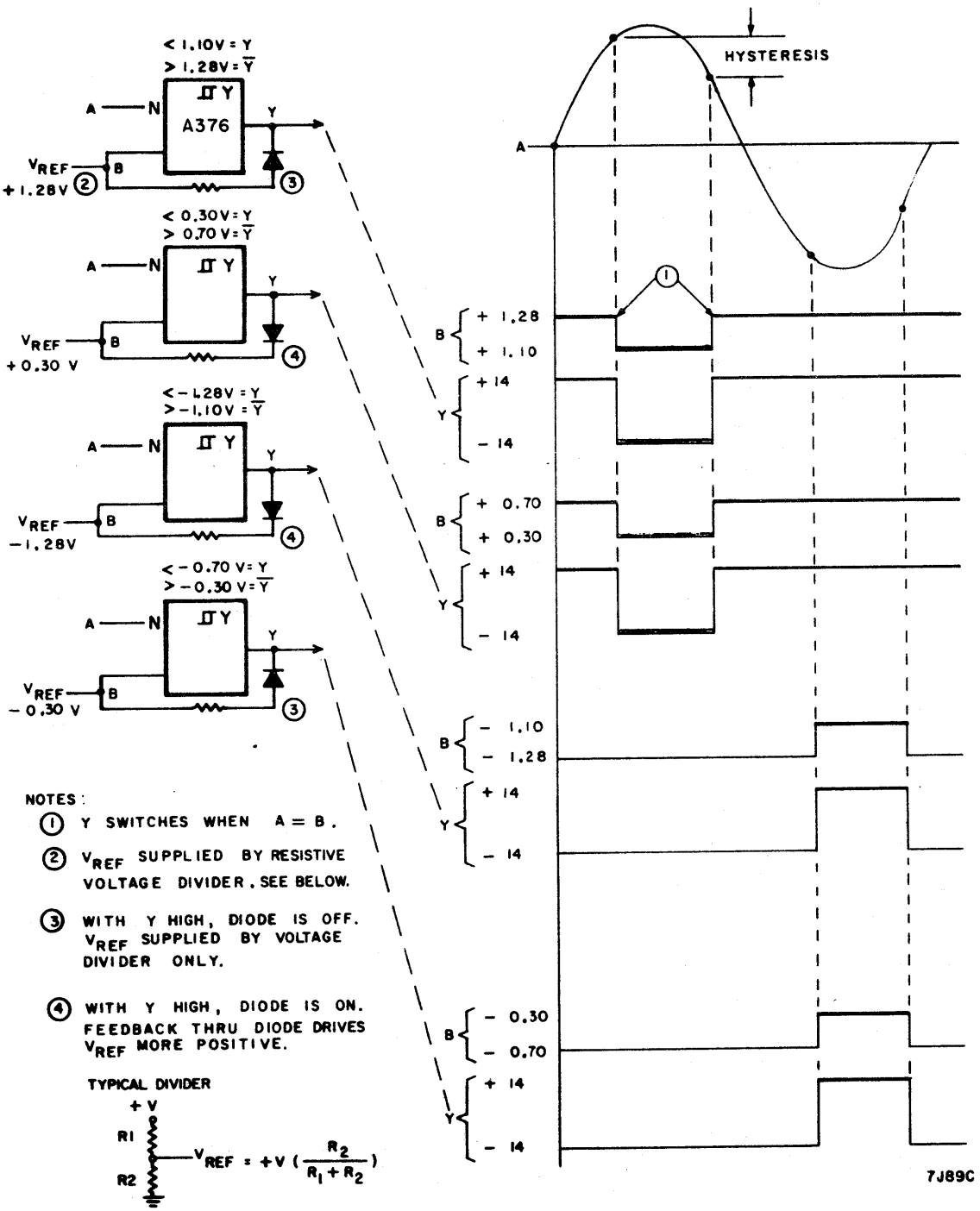


Figure 1-20. Op Amp Used as Schmitt Trigger

SECTION 2

LOGIC SYMBOLOGY

GENERAL

Logic symbols are used to portray various types of electronic circuits and are composed of the following parts:

- Symbol outline
- Qualifying symbol(s)
- Modifier(s)
- Indicator(s)
- Internal tagging information
- External pin assignments

All of these items are briefly explained in the following paragraphs.

As is shown in figure 2-1, the symbol outline merely determines the limits and shape of the logic symbol. In some cases, the outlines used to represent certain functions in a logic diagram set will differ from the standard ones shown in this manual. However, the pin numbers and meanings are the same.

The qualifying symbols shown in the figure denote basic operations being performed by the function. A 1 indicates an OR circuit, while an & indicates an AND circuit. A complete listing of the many meanings of qualifying symbols appears later in this explanation. In some cases, a functional name may replace a qualifying symbol (e.g., ALU, meaning Arithmetic Logical Unit.) The qualifying symbol appears in the neck of the common control block of certain symbol outlines, as shown.

QUALIFYING SYMBOLS

Qualifying symbols and functional names used in binary combinational logic are listed below. Combinational logic means that for each function or interconnection of binary functions at the input of a logical device, there corresponds only one binary state at its output.

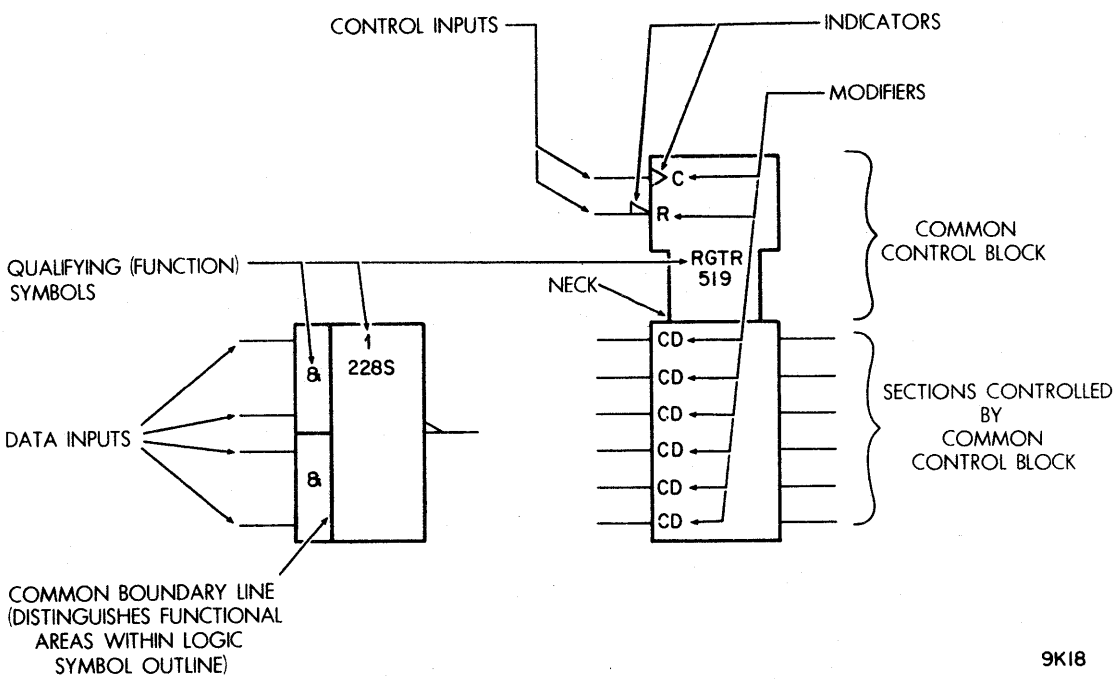


Figure 2-1. Typical Logic Symbols

COMBINATIONAL LOGIC QUALIFYING SYMBOLS

&-AND: Output of element assumes its active state if and only if (IFF) all inputs are in active states.

&-Wired AND: Same as AND gate above except that AND function is accomplished by wiring outputs together rather than by using gates involving other elements. Output of a Wired AND cannot be an input to a Wired OR.

1-OR: Output of element assumes its active state IFF one or more of its inputs assumes its active state.

1-Wired OR: Same as OR gate above except that OR function is accomplished by wiring outputs together rather than by using gates of other elements.

=1-Exclusive OR: Output assumes its active state IFF one of its two inputs becomes active.

≥m-Logic Threshold: Output assumes its active state IFF the number of inputs which assume their active states reaches or exceeds the number (m) specified in the qualifying symbol.

=m-m and only m: Output assumes its active state IFF m of its n inputs (where n > m) assume their active state.

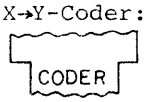
=Logic identity: Output assumes its active state IFF all inputs assume same state.

2K+1-Odd and only odd: Output assumes its active state IFF an odd number of inputs assume their active states.

2K-Even and only even: Output assumes its active state IFF an even number of inputs assume their active states.

X/Y-Level converter: Converts binary signal of one pair of states to corresponding levels of second pair of logical states.

X→Y-Coder: Input code X converted to output code Y per weighting technique of modifiers or table. Logic sets using common control block as shown here may use the functional name CODER.



X MAX→Y-Priority Coder: An element with multiple inputs and outputs in which resultant outputs are a representation of the active input with the largest coefficient.

DEMUX-Demultiplexer: A function or array of functions in which data input is selectively routed to one of several outputs as determined by control lines.

MUX-Multiplexer: A function or array of functions in which control lines determine which one of several inputs is selectively routed to the output.

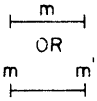
ALU-Arithmetic and Logic Unit: Performs either arithmetic or logic functions (or both) according to internal notations or by external reference data.

SEQUENTIAL LOGIC QUALIFYING SYMBOLS

Qualifying symbols and functional names designated as sequential logic qualifiers are listed and explained below. Sequential logic means that for at least one combination of states of the input(s), there exists more than one possible state of the output(s). Outputs are also affected by time and previous internal states of the element as well as the normal inputs.

 - Schmitt trigger: Output of element assumes its active state IFF its hysteresis type input exceeds its active threshold value as it changes from inactive to active state. One threshold exists for positive-going signals, and another for negative-going signals.

 - Monostable element: A one-shot monostable retriggerable multivibrator which assumes its active state if the input changes from inactive to active state. Its output remains active for time period determined by element characteristics and externally connected RC components. It may be reset at any time by an input labeled R (Reset).

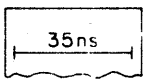


- Time delay: Output of element assumes its active state only after the period of time (m) following the transition of the input to its active state. Output reverts to inactive state only after time period (m or m' in alternate symbol) following the transition of the input to its inactive state.

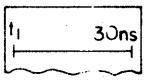
If one or both delay times are not fixed values, they are indicated by t_1 or t_2, as appropriate. Where tapped delays are used and

delay time is equal in both directions, the appropriate time period replaces m in first version of symbol and a corresponding numerical value of delay is used as an output modifier. The second version of the qualifying symbol is used IFF delays are unequal in opposite directions.

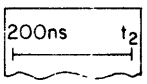
EXAMPLES:



Both zeros and ones are delayed by 35 nsec.

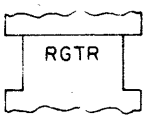


Zeros delayed by 30 nsec when input becomes a 0.

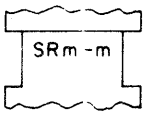


Ones delayed by 200 nsec when input becomes a 1.

(No Symbol) **Flip flop: A binary element** with two stable states. One is called set (or active) state and the other is reset (or inactive) state. Flip **flops** are identified by one or **more of** the following input signal modifiers: C,D,J,K,R,S,T.

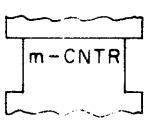


-Register: An array of flip flops having common input connections, such as reset, clock, or other gating functions.

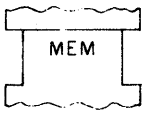


-Shift Register: m arrays of flip flops, each containing m' bits. The SR has at least one input used for transferring information in a specified direction from one bit position to another. The direction of shifting and number of bit positions shifted is indicated by input modifier which activates the shifting. IFF the shift register is dynamic, the qualifying symbol (▷ SRm-m') is used.

→ - Shift Register: An array of flip flops comprised of m bits similar to other SR, but with only serial input and output.



- Counter: An array of flip flops in which the states represent a number **that may be increased or** decreased by inputs designated by +m or -m. The counter modulus is indicated by the number used to replace m.



- Memory: An addressable array of flip flops in which input(s) and output(s) are multiplexed to and from bit positions. The number of addresses at which bits are located is indicated by address (A) modifier suffixes in common control block. Number of bits at each address is indicated by number of flip flops abutted vertically to common control block.

ANALOG QUALIFYING SYMBOLS AND FUNCTIONAL NAMES

▷m - Amplifier: A single input amplifier having a gain of m. Inversion of the signal is indicated by an N at the appropriate input or output(s).

$\sum$▷m - Summing or Differential Amplifier: The basics of single input amplifiers apply, but with additional provision for multiple inputs. Output is algebraic sum of weighted values of **inputs, times the gain factor m. Weighting values are implied to be unity if omitted from** symbol.

$\int$▷m - Integrating Amplifier: An amplifier whose output is proportionate to the integral parts of the input signal times **the gain factor m.**

>m or $\sum$<m' - Threshold or Comparator: A circuit with one analog input that provides an output proportional to the amount the input passes a predetermined threshold (applies to analog circuits).

For comparator circuits, the binary output remains inactive until the input either exceeds or becomes less than a predetermined value.

In the symbol, m is replaced by the applicable value and units of measurement.

Threshold circuits and comparators are differentiated from each other by indicators or modifiers at their outputs. Directly to the right of the symbol outline, the threshold circuit (analog output) may have an N or ∩ indicator while the comparator (binary output) may have either a # or / indicator. If the output connects to another input across a common boundary line, the threshold circuit output is indicated by an N or P; the comparator output by a polarity (▷) indicator,

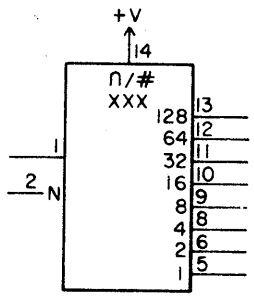
or by a modifier such as G,R, or S, or by a - (minus) across the common boundary line.

NOTE

N is never used with single-input threshold or comparator circuits.

|∩|>m - Rectifying Threshold Circuit:
|∑|>m Analog output is proportional to the amount the rectified input exceeds the predetermined value,m.

∩/# - Analog to Digital Converter: Summation of the weighting factors of the active binary outputs is a representation of the analog inputs. The minimum value of analog input that corresponds to all weighted outputs inactive, and the maximum value of analog input that corresponds to all weighted outputs active, is indicated next to the symbol. For example:



ALL HI=+9.96V

If pin 1=+9.96V relative to pin 2, all outputs will be HI. If pins 1 and 2 same voltage, all outputs will be LO.

#/∩ - Digital to Analog Converter: Analog output is a representation of the summation of the weighting factors of the active binary inputs. A voltage value is stated next to symbol as it is for A/D converter previously explained.

λ/# - Optical to Digital Converter: The binary output is active for analog or binary light inputs greater than stated threshold value. The binary output is inactive for inputs less than threshold. The output is indeterminate for light input values within the defined threshold tolerance of the element.

#/λ - Digital to Optical Converter: The optical output has the highest light intensity for an active binary input and the lowest intensity for an inactive binary input.

λ/∩ - Optical to Analog Converter: The analog output (No N indicator) is more positive in proportion to increasing analog light inputs, and conversely more negative for decreasing light inputs.

∩/λ - Analog to Optical Converter: The optical output has an increasing light intensity in proportion to the analog input (No N indicator) becoming more positive and a decreasing light intensity in proportion to the analog input becoming more negative.

mVR - Regulator or Reference: The output provides a regulated or
mAR reference value of m amperes or m volts including the effect of external components.

V/V - Voltage to Voltage Converter:
m Output voltage is isolated from power supply connections at top or bottom of symbol outline. A value is substituted for m.

m
⊢—⊣ - Delay element: An analog function similar to that used in Sequential Logic except that the delayed output is not usable for unequal delays in both positive and negative directions, but must allow for continuous analog values (not just binary states). A value or a time unit such as ns replaces the time delay period, m.

>——< - Bilateral Switch: A binary-controlled switch which passes or blocks analog or binary signals in either direction. It passes signals if the affecting inputs are active and does not amplify.

F▷m - Amplifier: An amplifier with special transfer functions. Mathematical symbols are preferred as a replacement for F. Appropriate values are used to replace m. Some typical functions for F are:

SIN	Sine
COS	Cosine
d/dt	differentiation
∫	integration
$\cap^m$	exponential power
LN	Log natural
LOG_{10}	Logarithm to base 10
×	multiply

÷ divide

m m' band pass

m m' band reject

m/m' positive & negative clamping function

m/m' bidirectional threshold circuit

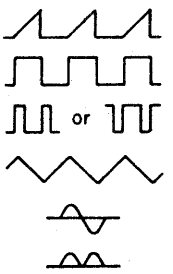
m resonant circuit

m notch filter

GENERATOR QUALIFYING SYMBOLS

The following symbols apply to both binary logic or analog functions.

G
m
m' - Generator: A cyclic or static signal source as indicated by m. The m is replaced by an appropriate graphical signal or static value generated. The m' is replaced by the frequency, such as 6 kHz. Some typical graphics for m are:



!G! - Generator: A synchronously started and stopped generator.

OTHER QUALIFYING SYMBOLS

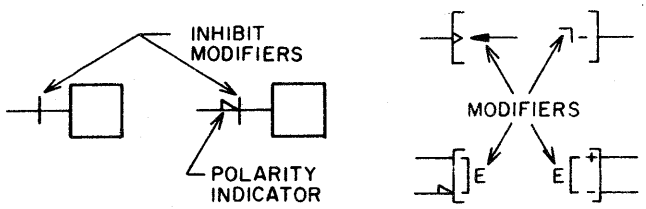
/m
m/
/m/ - Variable Parameter Function: A parameter of the basic function, m, is variable.

m*
m**
F - Incomplete Symbol: A symbol requiring additional information to interpret, but with similarity to any symbol m shown.

MODIFIERS

Modifiers are identifiers used to describe any special relation of an input or output to other input(s) or output(s) and/or to the qualifying symbol. They pertain to the virtual inputs or outputs as contrasted to indicators which pertain to the real or measurable inputs or outputs.

All modifiers (except the inhibit) are placed inside the symbol outline. The inhibit modifier is placed outside the symbol (see below).



BASIC MODIFIERS

Unless otherwise noted, the basic modifiers described in the following paragraphs are active, IFF:

1. Their input is active and the necessary A,C,F, and G affecting inputs prefixing the modifier are also active according to dependency notation, or,

2. One or more of the V (OR) relationship affecting inputs prefixing the modifier are active.

D - Data: Analog or binary input clocked in by a control (C) input.

E - Extender: Input or output used to expand the inputs of one element with outputs of another.

I - Initial Conditions: An analog initial conditions input which is always gated by a control (C) input, and whose analog value causes the sequential analog function to take on a proportionate analog value.

S - Set Input: A binary input that causes a sequential analog or binary element (such as a flip flop) to assume its set condition.

T - Toggle Input: A binary input that causes a flip flop or other sequential binary function to change its state each time the T input assumes its active state.

R - Reset Input: A binary input that causes a sequential analog or binary element (such as a flip flop) to assume its reset condition.

J - Input: A binary input analagous to the S input, but modified such that if both J and K inputs assume their active states simultaneously, the flip flop changes to the opposite state.

K - Input: A binary input analagous to the R input, affecting a flip flop in the same way as a J input.

÷ - Divisor Input: An analog divisor input for use with a function that includes analog division.

↗ - Parameter Input: An analog input which controls a variable characteristic of the function as denoted by the qualifying symbol or by tagging.

+m, -m - Increment or Decrement Input: A binary input that causes the states of flip flops serving as a counter to change the binary number by +m or -m each time the +m or -m input is active.

→ m, ← m - Shift Down (Right) or Shift Up (Left) Input: A binary input that causes the flip flops forming a shift register to shift m positions down (or right) or up (or left) each time the appropriate input is active.

⊣ - Inhibit Input: A binary input used to block the active state outputs of a non-sequential binary function.

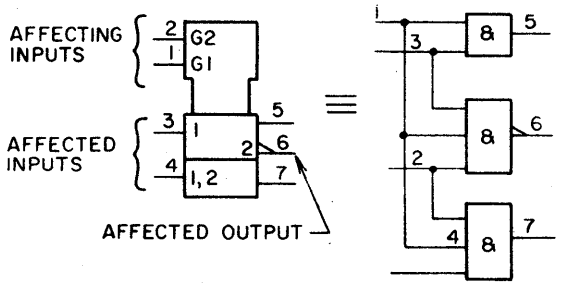
m ⌐ - Output Delay: A binary output which changes state only after the referenced input (m) returns to its inactive state (whether HI or LO).

Øm - Phase Relationship: A binary output which is active according to the phase relationship denoted by m.

(m) - Coincident Input or Output: A restrictive modifier that is not associated with any input or output, but restricts the number of inputs or outputs which may be active simultaneously.

DEPENDENCY MODIFIERS

Dependency notation is a means for obtaining simplified symbols to represent complex elements by denoting the relationships between inputs, or between inputs and outputs, without showing all elements or interconnections. The input or output that is dependent upon another input is called the affected input or output, and the input on which it depends is called the affecting input. An affecting input has an effect only on those inputs or outputs which relate to it according to the notations discussed in the following paragraphs.



A - Address: A binary affecting input, or affected input(s) and output(s) used as data ports of addressable memories.

C - Control (Clock): A binary affecting input or affected input(s) used where more than a simple AND relationship is implied to those inputs or outputs labeled with the same identifier. Also, it is used as a data gate as contrasted to an active state gate (See G).

G - Gate or AND: A binary affecting input having an AND relationship to the active state. Two affecting inputs labeled G but having different identifier suffixes stand in no relation to each other. IFF they have the same identifying character, they stand in an OR relationship.

NOTE

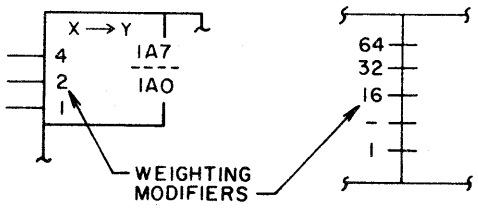
When inputs are affected by both G and C modifiers (e.g., data -- or D -- input), the AND relationship is between G and the active state of the input signal. G **does not** affect control (C modifier) inputs.

V - OR: A binary affecting input having an OR relationship to those inputs or outputs which are labeled with the same identifier. Two inputs labeled V having different identifying characters stand in no relation to each other.

F - Free: A binary affecting input, or affected analog or binary inputs or outputs, acting as a connect switch when active or a disconnect when inactive.

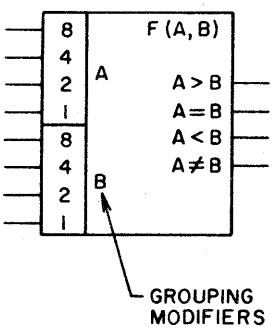
WEIGHTING MODIFIERS

Weighting modifiers show the relative coefficients applicable to various inputs and/or outputs. For example:



GROUPING MODIFIERS

Grouping modifiers are used to designate a group of two or more inputs or two or more outputs to simplify reference to that group of inputs or outputs. For example:

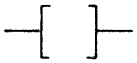


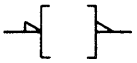
INDICATORS

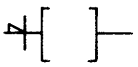
An indicator is a symbol used to specify physical values and/or properties of an input or output connection. Explanations of various groups of indicators follow:

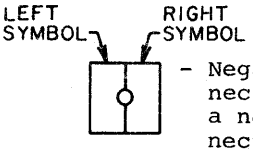
BINARY INDICATORS

All binary inputs or outputs have active state indicators (implicit or explicit) to specify the active state relative to the logic function.

 - Implied Indicator: The absence of the polarity indicator (▷) implies a static logical HI.

 - Polarity Indicator: Indicates the active state is a static LO.

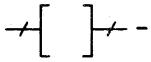
 - Inhibit/Polarity Indicator: Same as polarity indicator above, except signal is blocked when a static LO.

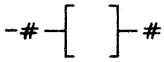


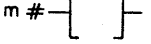
- Negating Indicator (internal connections only): Used to indicate a negating type of internal connection. The bubble indicates the inactive state output of the left symbol will provide an active state input for the right symbol. The m in the second symbol represents a modifier.

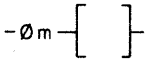
 - Dynamic Active State: The triangle represents the transition from the inactive to active static state of the input (not merely the presence of the active static state).

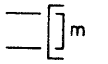
SUPPLEMENTARY BINARY INDICATORS

 - Non-Standard Logic Level: Slash mark used on signal lines (input and/or output) to indicate binary levels that differ from those defined as standard.

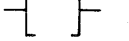
 - Binary Logic: This indicator differentiates binary from analog logic levels.

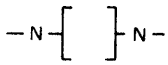
 - Serial Binary Bit: This indicator denotes a line carrying m bits of binary information in serial form. The m is replaced by the number of bits in each repetitive pattern.

 - Phase Line: This indicator denotes a line carrying a phase reference signal that must be differentiated from other binary or analog signals. The m is replaced with the appropriate character.

 Grouping Bracket: This indicator represents two or more grouped lines (such as a differential pair) carrying only one bit of binary information and represents a single input.

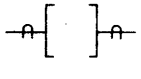
ANALOG INDICATORS

 Implied Indicator: The absence of the N indicator implies a non-inverting input relative to other inputs or outputs.



Sign Indicator: Indicates an inverting input or output.

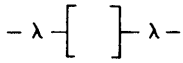
Internal Sign Indicator: This indicator is similar to the polarity indicator used in binary circuits. Here N means inversion, and P means non-inversion.



Analog Signal: This indicator is used to differentiate analog signals from binary (#).

SUPPLEMENTARY ANALOG AND BINARY INDICATORS

Wired Connection: This indicator represents an analog or binary line that enters a wired function when necessary to distinguish that its value or state may be affected by one or more outputs elsewhere.



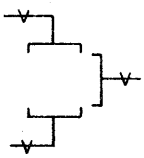
Optical Signal Path: This indicator shows that a path of light is the conductor rather than an electrical wire.

LO Output Only: The minus sign denotes that an element's output is capable of supplying LOs only (binary) or negative-going drive signals (analog).

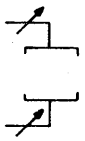
HI Output Only: The plus sign denotes that an element's output is capable of supplying HIs only (binary) or positive-going drive signals (analog).

Implied HI-LO Output: The absence of plus or minus indicates the element is capable of supplying HIs or LOs or positive or negative-going drive signals.

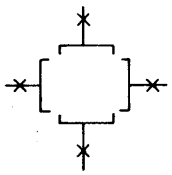
MISCELLANEOUS INDICATORS



Voltage Indicator: Denotes that this line carries a power supply or reference voltage when necessary to differentiate it from binary or analog signals.



Parameter Control: This indicator denotes a line used for varying the characteristic(s) of an analog or binary function indicated by a qualifying symbol.

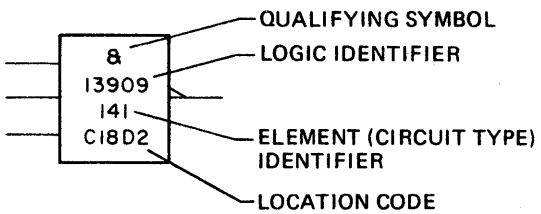


Non-Binary and Non-Analog Indicator: Denotes that the line so marked does not carry binary or analog information (when necessary to distinguish it from other lines, and no other indicators apply).

INTERNAL TAGGING

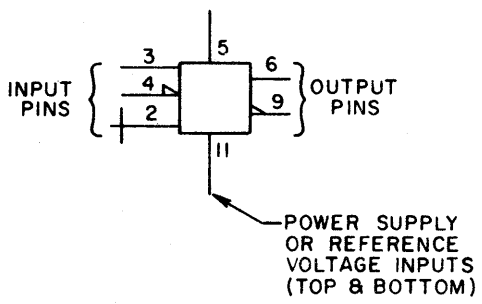
Internal tagging information, as applicable, is placed on successive lines within the symbol outline in the following order:

1. Qualifying symbol representing a function (when used). Circuits such as flip flops do not have a qualifying symbol.
2. Logic identifier such as I3909, K3900, etc. (Optional.)
3. Element (circuit type) identifier.
4. Physical location code.



In symbols having a common control block, tagging information is placed in the neck of the symbol, as shown in Figure 2-1.

EXTERNAL PIN ASSIGNMENTS



SECTION 3

DATA SHEETS

INTRODUCTION

Magnetic Peripherals, Incorporated uses three methods to identify ICs on logic diagrams. These methods, and how they relate to locating specific data sheets in this manual, are described below.

1. Element Identifier -- a corporation-wide designator of three or more digits, followed when applicable by a letter that usually signifies the relative speed of the circuit: 146, 146H. Identifiers with four or more digits are usually the same as the vendor type number: 4001, 10125, 100114.

2. Vendor Type Number -- a designator of up to six digits that may have a "speed" letter imbedded: 74H51, 5603. Prefix letters that specify a particular vendor are usually (but not always) omitted. Thus, the Texas Instruments chip SN74H51 would appear in the logic symbol on the diagram as 74H51. Because speed variations are not used in this manual as a means of classifying ICs, SN74H51 (or 74H51) would be shown here as 7451. Suffix letters that usually designate different methods of physically packaging an IC are shown on the logic diagram and also here: 741C, 741S, 340T.

3. Unique Microcircuits Identifier -- a designator for ICs that are produced by (or specifically for) MPI. The limited usage of these circuits does not warrant having corporate element identifiers assigned to them.

The data sheets are arranged in two groups, each preceded by a divider page identified as follows:

- DATA SHEETS ARRANGED BY ELEMENT IDENTIFIER:
  Here the element identifier becomes the base page number: 139, 140 ... 149, etc. If the data requires more than one page, the base page number is followed by a dash number: 162-1, 162-2, etc.

- DATA SHEET LIST ARRANGED BY VENDOR TYPE NO. OR UNIQUE MICROCIRCUIT IDENTIFIER.
  Here the sheets are arranged first by number, then by letter. Thus, 5AA precedes 7451, which comes before 74153, and they all appear before SNG82.
  No specific attempt has been made in this grouping to separate Vendor Type numbers from Unique Microcircuit identifiers.

  Keep in mind that if the Vendor Type Number is the same as the Element Identifier, the number will appear in the first section of this list. Also, such numbers will not appear in the cross-reference list because cross-referencing is not needed.

DATA SHEET INTERPRETATION

All of the data sheets in this section contain the following kinds of information:

1. LOGIC SYMBOL -- The ANSI/CDC symbol for the high-active version of the microcircuit and, where applicable, the alternate low-active version. Pin numbers are included as part of the symbol. Special notations to clarify the various input and output functions are added when helpful, but are not to be construed as part of the symbol.

2. DESCRIPTION -- An explanation of the function or functions performed by the microcircuit.

3. NOTES -- Helpful information, such as:

   - Vendor identification number
   - Package pin configuration. Defines pins used for external voltage sources (VCC, VEE, GND, etc.) and keys, slots or marks used to orient the microcircuit.

In addition, the following information is included on individual data sheets, when applicable:

4. FUNCTIONAL DIAGRAM -- Basic logic symbols (NAND, NOR, FF, etc.) arranged to show the internal logic of the microcircuit.

5. TRUTH TABLE -- A table showing the state(s) of the microcircuit's output for varying input conditions.

6. TIMING DIAGRAM -- Used to clarify complex timing relationships between inputs and outputs.

DATA SHEET LIST

The list on the following pages shows the order in which the data sheets appear, and also provides a quick reference to the family (TTL, ECL, CMOS) to which a particular microcircuit belongs. If a circuit requires more than one data sheet, the number of sheets is given in parentheses.

If the logic symbol that you are trying to find the data sheet for is identified by a number that you can't find in the data sheet list, turn to the Cross Reference List on the page following the Data Sheet List. If you still can't find the data sheet, it probably does not exist at present. If this happens, fill out the Comment Sheet at the back of this manual, and drop it in the mail.

DATA SHEET LIST

BY ELEMENT IDENTIFIER

TTL

130 (see 139)
139
140
141
142 (2)
143
144 (2)
145
146
147
148
149
158 (3)
159 (3)
161
162 (2)
163
164 (2)
166 (2)
167 (2)
170 (2)
172
173
175
176
180
182 (2)
188
189
191 (2)
193
195
200
201
202
203
205
206
207
208
209
210
212
213
216 (2)
218
220
222
223
224
225
226
227
228
229

TTL

230
233
240
242 (2)
243
247

OP AMPS

300
301
302
304
306
307
308
309
310
313
315
316
318
320 (2)
321
322
324
326
327 (2)
329
330
331
332/353
333
334 (2)
338 (2)
339
340
341
344
352/352A
353 (see 332)
356
357
363 (3)
368 (2)
370
386
394
431

TTL

500 (3)
501 (2)
502
505 (2)
506 (3)
507 (2)
508 (2)
509 (2)
510 (2)
512 (3)
514
515 (2)
519 (2)
520 (2)
521
522 (see 568)
524 (2)
525 (3)
527 (2)
528 (3)
529
530
531 (2)
532 (2)
537
538
539 (2)
542 (2)
543 (3)
544
550 (2)
551
552
554 (2)
559
563 (3)
568
571 (3)
572
579 (2)
581
582
585 (see 6802)
586 (see 6821)
587 (see 6840)
768
774
775 (2)
779

TTL

902
905
909
910
911
912
915
916 (3)
921
922
923
926
927
930
934
939
949
950A/5600 (3)
951
986 (2)

ARRAYS

3046
3096

CMOS

4001
4011
4016
4017 (2)
4023
4027
4049
4052
4053
5100, 5200, 5300, 5400 (9)
5700 (2)

ECL

10101
10102
10104
10105
10106
10107
10109
10114
10115
10116
10117
10124
10125
10131
10136 (3)
10141 (3)
10192
10198
12040 (2)

DATA SHEET LIST

BY VENDOR TYPE NO./UNIQUE MICROCIRCUIT IDENTIFIER

VENDOR TYPE NO./ELEMENT IDENTIFIER

CROSS-REFERENCE LIST

Vendor	Element	Vendor	Element	Vendor	Element
304	320	3060	175	7453	209
305	332	3060A	386	7454	225
309H	352A	3062	164	7455	220
309K	352	3450	949	7464	205
318H	322	3524	363	7474	175
319	339	4021	529 C	7475	551
320	356	4022	529	7483	521
339	341	4024	582	7485	524
340	357	4044	581	7486	149
358N	344	4194	331	7489	774
376	353	4195	333	7493	537
521F	162S	4344	581	7495	506
531	308	5012	926	7496	515
555	916	5558	324	7498	568
562B	579	5711	321	7805	357
685	330	7090	300	7808	357
710	307	7400	140	7812	357
711	130	7401	202	7815	357
711C	139, 370	7402	148	7818	357
715	304	7403	202	7820	910
723C	334	7404	146	7824	357
733	302	7405	203	7830	909
741	313	7406	200	7905	356
741C (T099)	301	7407	227	7912	356
741C (14-pin)	326	7408	201	7915	356
741C (8-pin)	340	7409	201	8T23	921
741S (8-pin)	340A	7409 (S/LS)	229	8T24	922
747	306	7410	141	8T26	934
1403U	394	7411	213	8093	216
1408	986	7412	230	8097	939
1414	310	7420	208	8123	530
1437	338	7421	212	8206	775
1458	324	7425	207	8209	768
1468	327	7427	224	8214	542
1540	329	7430	206	8231	166
1723C	334	7432	218	8241	222
3001	309	7437	210	8262	559
3002	172	7440	143	8281	163
3003	218	7442	507	8291	182
3004	173	7450	145	8570	527
3021	149	7451 (L/LS)	223	8820	910
3040	315	7451 (S)	228	8830	909

Continued on next page

VENDOR TYPE NO./ELEMENT IDENTIFIER (CONTD)

CROSS REFERENCE LIST

Vendor	Element	Vendor	Element	Vendor	Element
9000	142	9748	912	74181	509
9001	144	9749	912	74182	510
9002	140	14433	368	74191	512
9003	141	72558	318	74193	500
9005	145	74104	142	74194	528
9007	147	74105	144	74195	159
9009	143	74106	242	74197	182
9015	188	74112	243	74199	543
9016	146	74113	164	74200	775
9024	240	74123	193	74221	233
9300	159	74132	923	74260	226
9301	191	74133	247	74279	544
9309	170	74138	563	74280	572
9312	166	74139	538	74298	554
9313	166	74150	531	74367	939
9314	550	74151	505	75107	162
9316	158	74153	508	75108	162C
9318	532	74154	167	75154	902
9321	538	74155	525	75283	571
9322	189	74156	525	75450	180
9324	501	74157	189	75451	905
9334	552	74158	539	75452	930
9336	512	74161	158	75453	927
9352	507	74164	527	75461	951
9366	500	74170	514	93415	779
9396	515	74174	519	93419	768
9601	161	74175	520	5065989	915
9602	195	74180	502	LH0002CH	316
9743	911				

DATA SHEETS ARRANGED BY ELEMENT IDENTIFIER

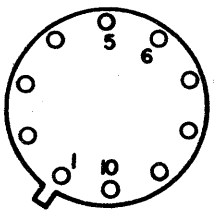
DESCRIPTION

The 139 circuit consists of two high-gain voltage comparators with separate differential inputs and a common output. Individual strobes (G) allow independent gating of the inputs to each section.

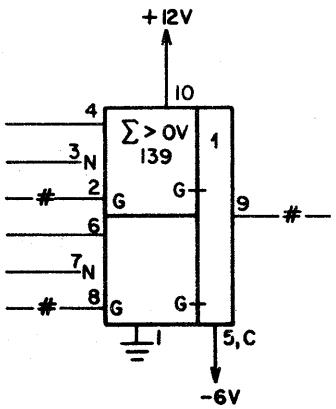
The circuit has a voltage gain of 500.

NOTES:

1. Vendor identification: 711C
2. Package pin configuration:



(Bottom View)



(# IDENTIFIES BINARY LOGIC SIGNAL)

LOGIC SYMBOL

139
Rev M
Sheet 1 of 1

DESCRIPTION

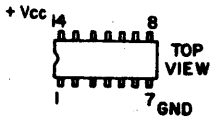
The 140 circuit is a four-section (quad), 2-input, positive NAND gate.

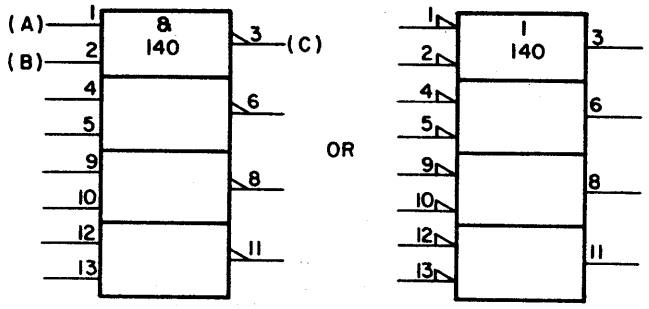
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
140	7400,9002
140H	74H00
140L	74L00
140LS	74LS00
140S	74S00

3. Package pin configuration.





LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE
(FOR ONE GATE)

140
Rev J
Sheet 1 of 1

DESCRIPTION

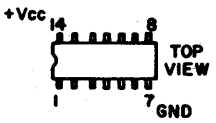
The 141 circuit is a three-section, 3-input, positive NAND gate.

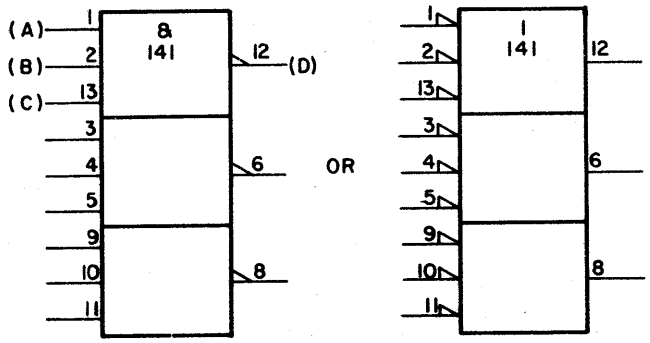
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
141	7410,9003
141H	74H10
141L	74L10
141LS	74LS10
141S	74S10

3. Package pin configuration.





LOGIC SYMBOL

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE

141
Rev J
Sheet 1 of 1

DESCRIPTION

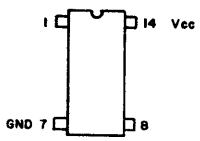
The 142 circuit is a J-K master-slave flip-flop with asynchronous set (S) and clear (R) inputs. Input J-K is common to both the J- and the K- input AND networks, and may be used as a gating input.

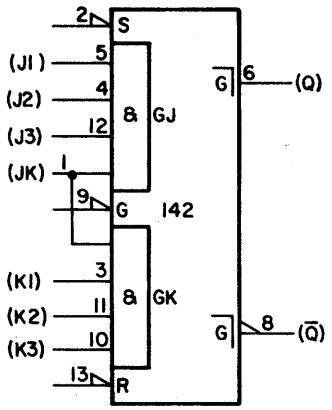
Information is received by the master while the clock (G) is low, and transferred to the slave section on the leading edge (negative-to-positive transition) of the clock pulse. On the trailing edge of the clock pulse, information is transferred to the outputs.

Bringing S or R low will cause the FF to set or clear, respectively. Conflicting synchronous inputs may cause spikes at the output during the preset-preclear operation, but these will disappear with the clock pulse.

NOTES:

1. Vendor identification: 74104/9000
2. Package pin configuration:





LOGIC SYMBOL

INPUTS AT tn			OUTPUTS AT tn+1	
JK	J *	K *	Q	$\overline{Q}$
L †	X	X	Qn	$\overline{Qn}$
H	L †	L †	Qn	$\overline{Q}$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Qn}$	Qn

* J = J1 J2 J3
K = K1 K2 K3

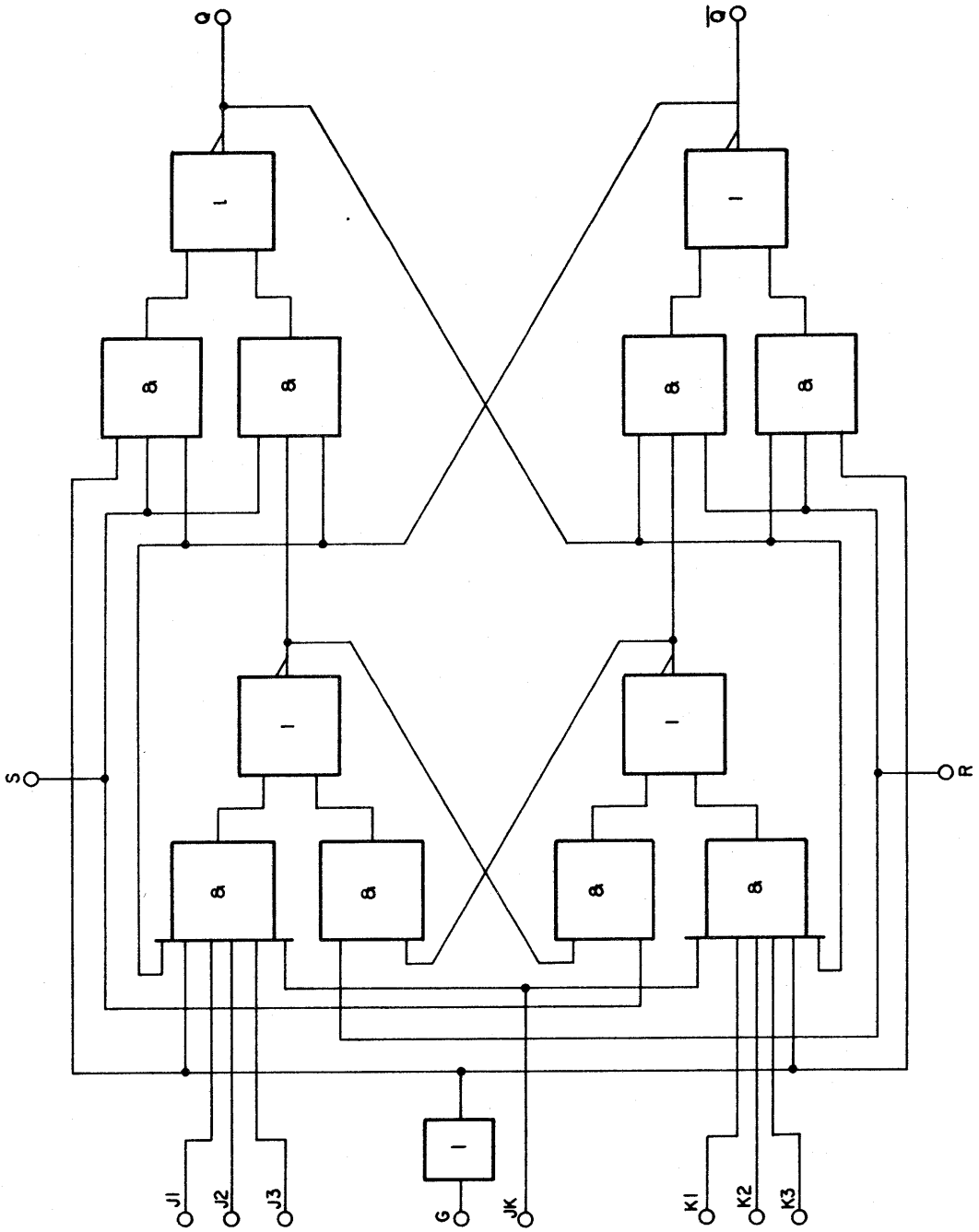
† THESE LOW LEVELS MUST BE MAINTAINED WHILE THE CLOCK IS LOW

tn BIT TIME BEFORE CLOCK PULSE

tn+1 BIT TIME AFTER CLOCK PULSE

TRUTH TABLE

142
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

142
Rev J
Sheet 2 of 2

DESCRIPTION

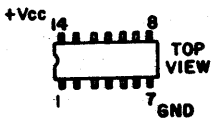
The 143 circuit is a two-section, 4-input, positive NAND gate.

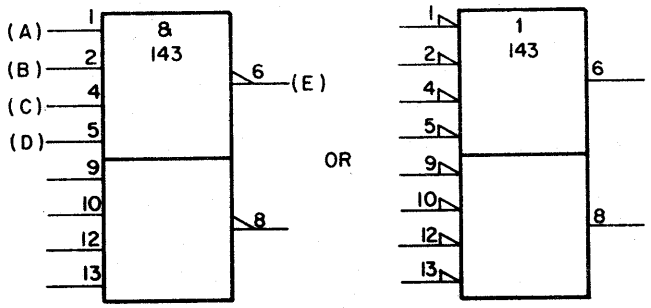
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
143	7440,9009
143H	74H40
143S	74S40

3. Package pin configuration.





LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE
(FOR ONE GATE)

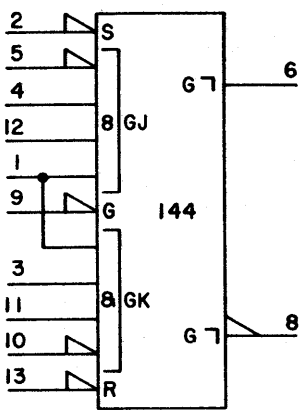
143
Rev J
Sheet 1 of 1

DESCRIPTION

The 144 circuit is a master/slave JK flip-flop with direct (asynchronous) set and reset inputs that override the J and K (synchronous) inputs. Pin 1, common to both J and K inputs, simplifies design in applications using a single gate-control source.

If either pin 2 or pin 13 is held LOW and the FF is clocked with opposing data at the J-K inputs, the LOW output may momentarily spike HIGH, synchronous with the low-to-high transition of the clock (pin 9). This situation can be avoided by disabling pin 1 whenever the asynchronous inputs are active.

Data is accepted by the master while the clock is LOW. Transfer from master to slave occurs on the positive-going edge of the clock. When the clock is HIGH, the J and K inputs are inhibited.



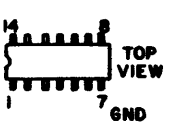
GJ-J INPUT CONDITIONED BY CLOCK (G)
GK-K INPUT CONDITIONED BY CLOCK (G)
G-GATE INPUT CLOCK; MUST BE PRESENT BEFORE J OR K INPUT(S) CAN BE TRANSFERRED TO OUTPUT(S)
S-SET INPUT: WHEN "L", FF IS SET REGARDLESS OF OTHER INPUT CONDITION
R-RESET (CLEAR) INPUT: WHEN "L", FF IS CLEARED REGARDLESS OF OTHER INPUT CONDITIONS

LOGIC SYMBOL

NOTES:

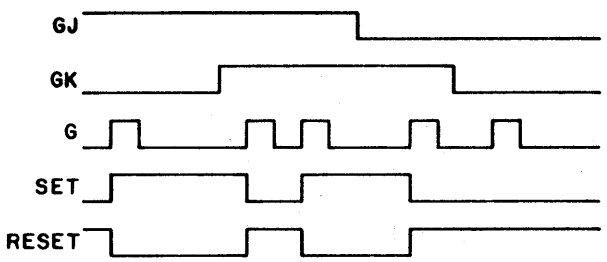
1. **Vendor identification:**
   74105
   9001

2. **Package pin configuration.**



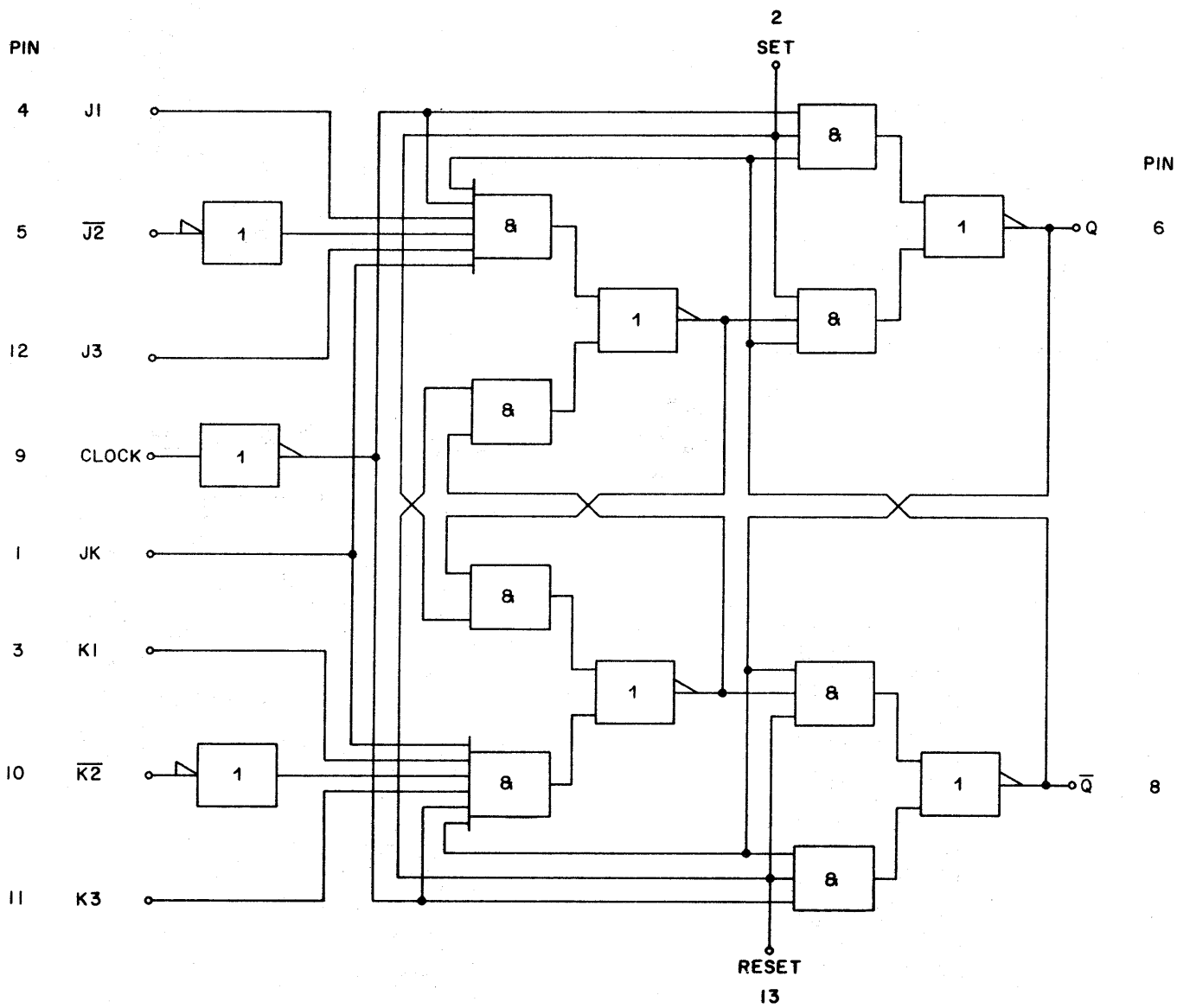
INPUTS		OUTPUTS BEFORE CLOCK		OUTPUTS AFTER CLOCK	
GJ	GK	SET	RESET	SET	RESET
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

TRUTH TABLE



TIMING SEQUENCE

144
Rev M
Sheet 1 of 2



FUNCTION DIAGRAM

144
Rev J
Sheet 2 of 2

DESCRIPTION

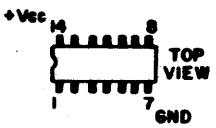
Circuit 145 is a dual, expandable AND-OR-INVERT gate. Section B of this circuit is expandable. If not expanded pins 11 and 12 are open.

NOTES:

1. If not used, expander pins may not be shown.
2. Vendor identification:

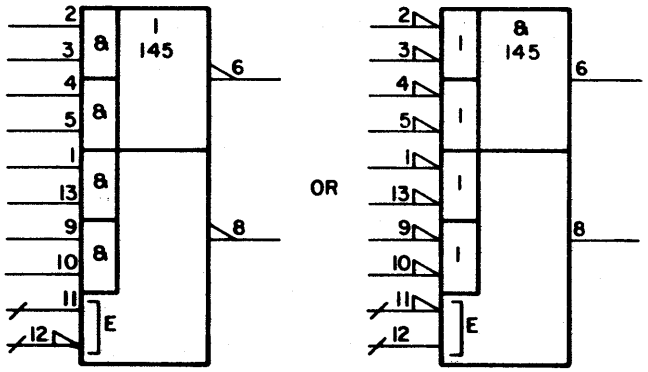
Element	Vendor Number
145	9005
145H	74H50

3. Package pin configuration.

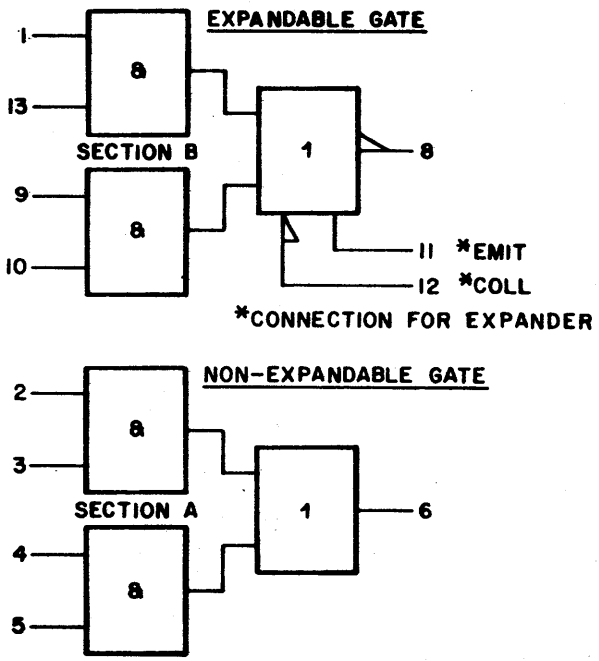


A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



PIN ASSIGNMENTS

145
Rev J
Sheet 1 of 1

DESCRIPTION

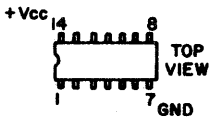
The 146 circuit is a six-section (hex) inverter.

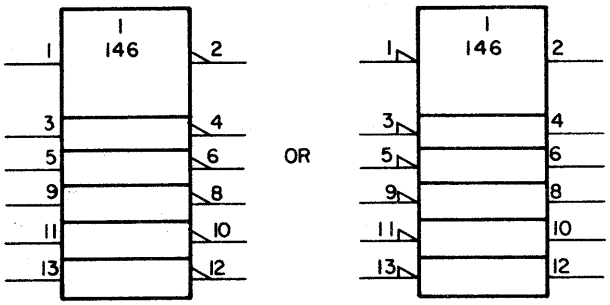
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
146	7404,9016
146H	74H04
146L	74L04
146LS	74LS04
146S	74S04

3. Package pin configuration.





LOGIC SYMBOL

146
Rev J
Sheet 1 of 1

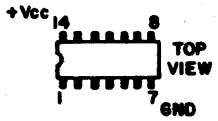
DESCRIPTION

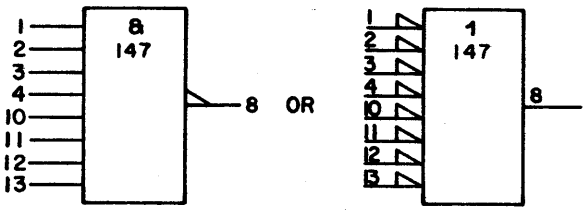
The 147 circuit is an 8-input, positive NAND gate.

NOTES:

1. Vendor identification: 9007

2. Package pin configuration.



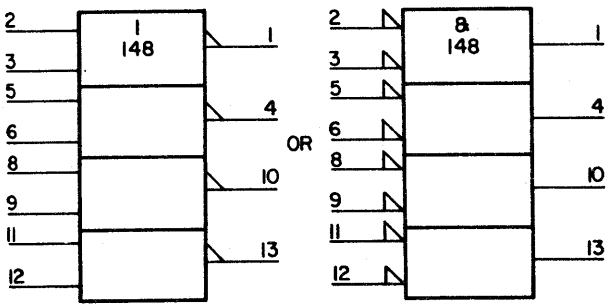


LOGIC SYMBOL

147
Rev J
Sheet 1 of 1

DESCRIPTION

Element 148 is a quad, 2-input, positive NOR gate.



LOGIC SYMBOL

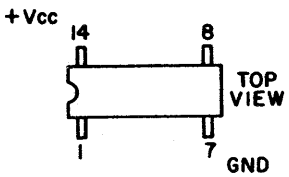
NOTES:

1. Symbols may appear separately.

2. Vendor identification:

Element	Vendor Number
148	7402
148L	74L02
148LS	74LS02
148S	74S02

3. Package pin configuration.



148
Rev J
Sheet 1 of 1

DESCRIPTION

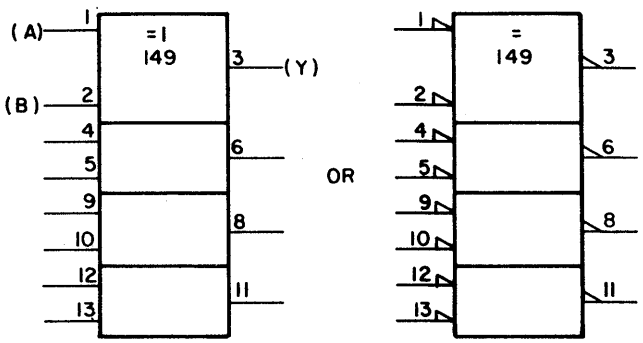
The 149 circuit is a quad, 2-input, Exclusive OR gate that performs the function $Y=A\overline{B} + \overline{A}B$. For low-active inputs, the circuit acts as an equivalence (identity) gate.

NOTES:

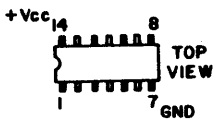
1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
149	7486
149H	3021
149LS	74LS86
149S	74S86

3. Package pin configuration.



LOGIC SYMBOL



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

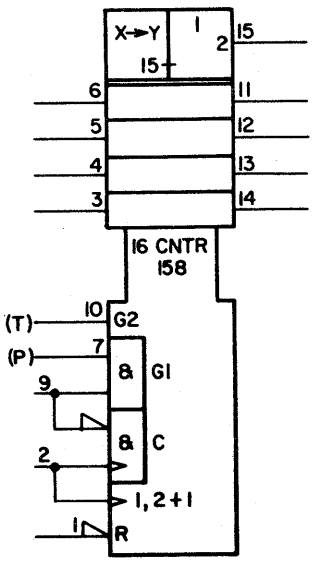
TRUTH TABLE

DESCRIPTION

The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.

In order for the counter to count, the load (pin 9), clear (R), and P and T enable inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

When P is low, the clock input is disabled so that the counter can not count. When T is low, the clock input and carry output are both disabled.



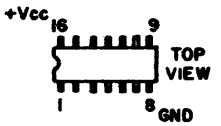
LOGIC SYMBOL

NOTES:

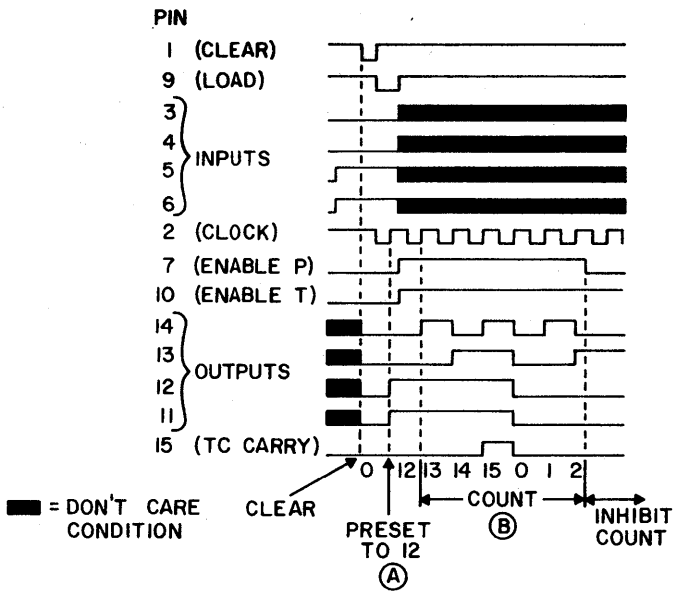
1. **Vendor identification:**

Element	Vendor Number
158	74161,9316
158A	74161
158LS	74LS161

2. **Package pin configuration.**



158
Rev J
Sheet 1 of 3



NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

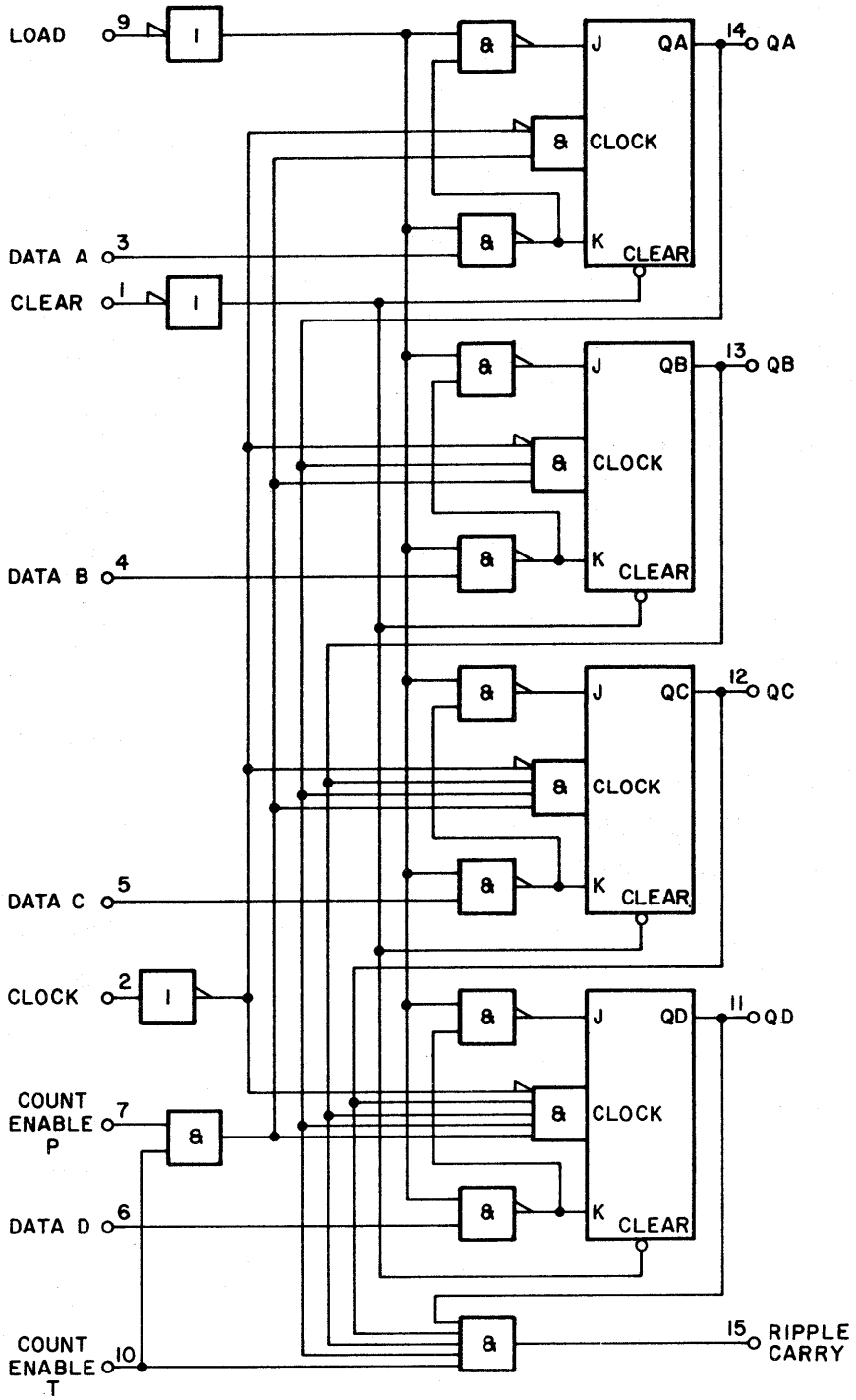
Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE



FUNCTION DIAGRAM

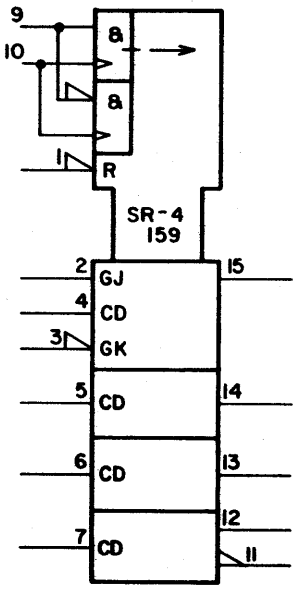
158
Rev J
Sheet 3 of 3

DESCRIPTION

The 159 circuit is a synchronous 4-bit shift register capable of shifting, counting, storage, and serial code conversion.

Data entry is synchronous; the outputs change state after each low to high transition of the clock. When the load/shift input is low, the parallel inputs determine the next condition of the shift register. When the load/shift input is high, the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through the J-K (serial) inputs. By tying the J and K inputs together, D-type entry is obtained.

A low level to the clear input will clear the outputs to a low level regardless of the levels to any input.



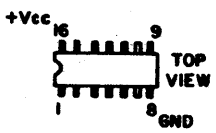
LOGIC SYMBOL

NOTES:

1. Vendor identification:

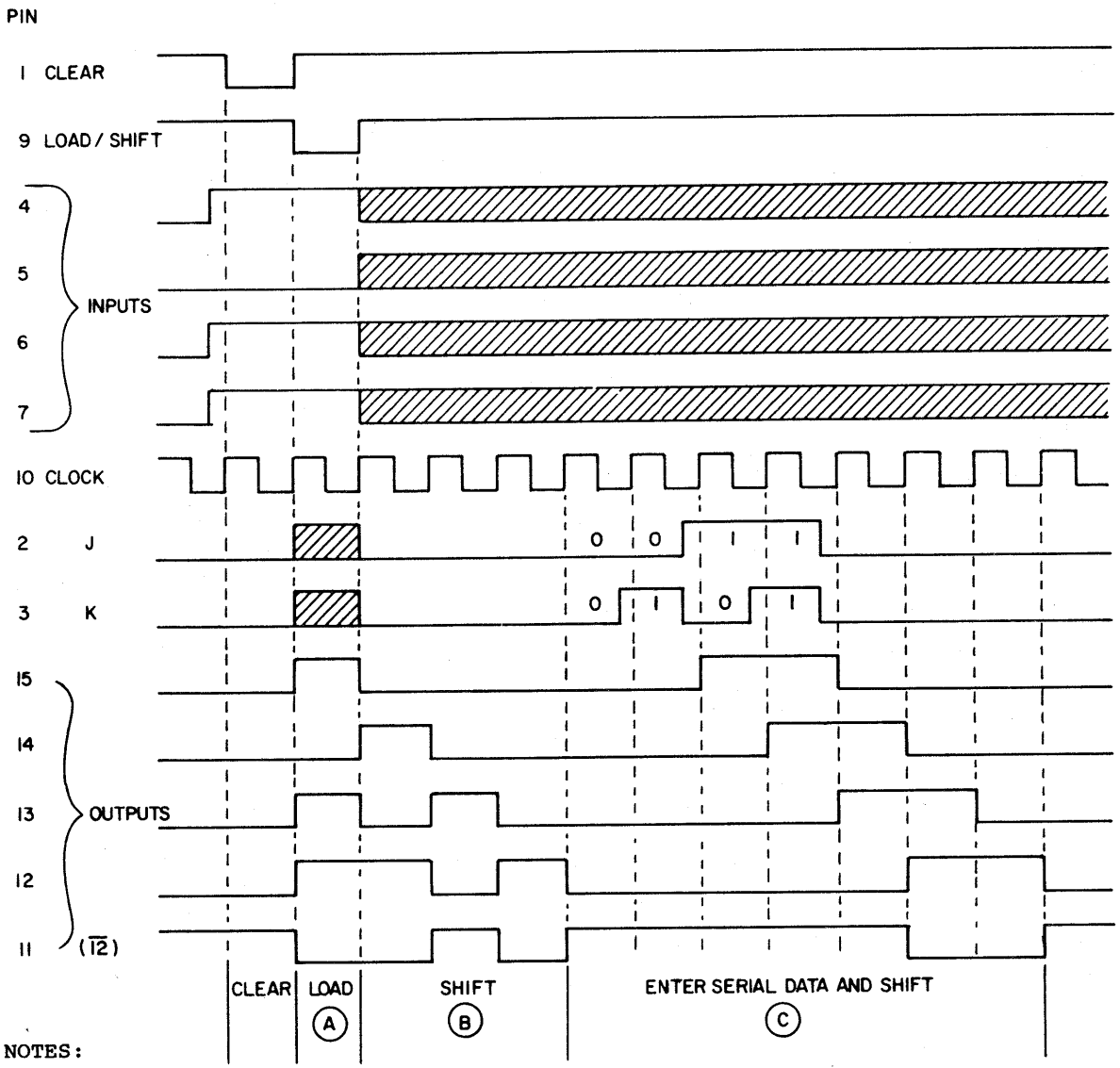
Element	Vendor Number
159	74195,9300
159LS	74LS195

2. Package pin configuration.



Pin	Function
1	Master Reset (clear)
2	First stage J input
3	First stage K input
4,5,6,7	Parallel data inputs
9	Load/Shift control
10	Clock
12,13,14,15	Parallel outputs
11	Complementary output ($\overline{12}$) for last stage

159
Rev J
Sheet 1 of 3



NOTES:

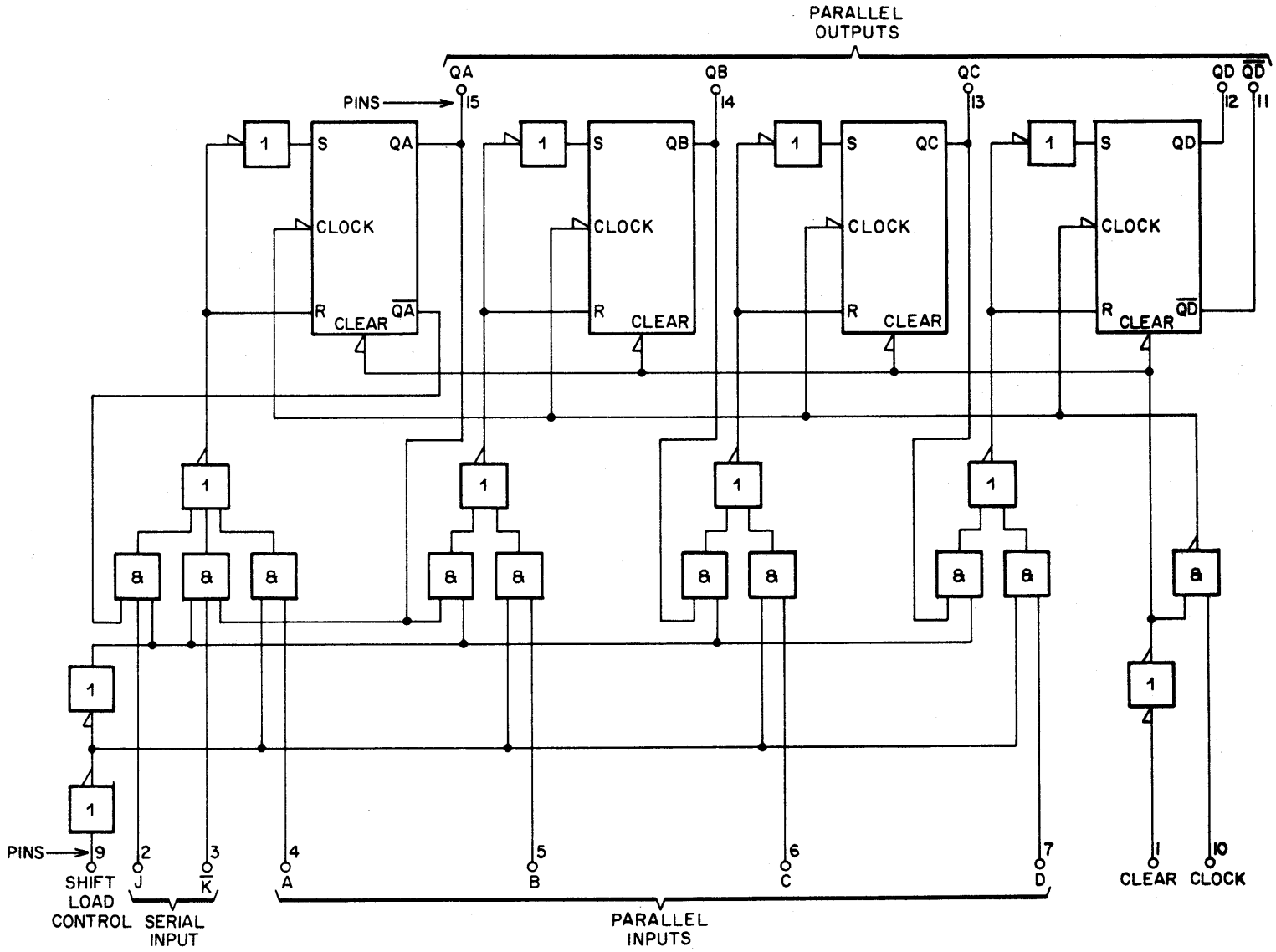
(A) Parallel data entered via CD inputs by pin 9 low and positive-going signal on pin 10.

(B) Data shifts down (Pin 15→Pin 14, etc.) with clock.

(C) Serial data entered into J-K inputs by pin 9 high and positive-going clock. Pin 4 input inhibited because pin 9 is high. Outputs follow Truth Table shown below. (Were J and K tied together, output at pin 15 would track the J input with no deviation from the Truth Table.)

INPUT PINS		OUTPUT PIN
2	3	15
0	0	0
0	1	0(NO CHANGE)
1	0	1(TOGGLES)
1	1	1

159
Rev J
Sheet 2 of 3

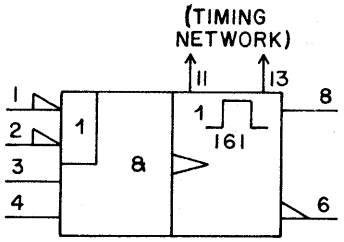


FUNCTION DIAGRAM

DESCRIPTION

The 161 circuit is a monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 3 and 4 trigger on the positive going edge of the input pulse and pins 1 and 2 trigger on the negative going input pulse. The 161 circuit will retrigger while in the pulse timing state (pin 8 high); the end of the last pulse will be timed from the last input.

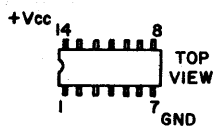


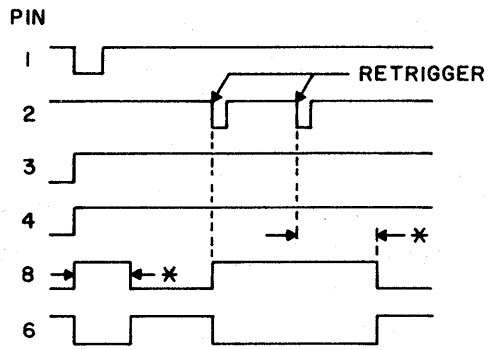
LOGIC SYMBOL

NOTES:

1. Vendor identification: 9601

2. Package pin configuration.





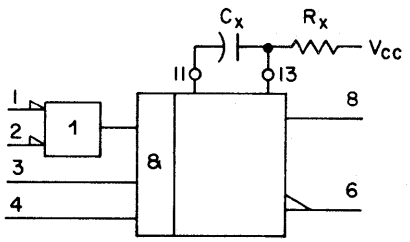
*PULSE WIDTH DETERMINED BY RC TIMING NETWORK

TIMING SEQUENCE

INPUT PINS				OPERATION	OUTPUT PINS	
1	2	3	4		8	6
H→L	H	H	H	TRIGGER	⎍	⎎
H	H→L	H	H	TRIGGER	⎍	⎎
L	X	L→H	H	TRIGGER	⎍	⎎
X	L	L→H	H	TRIGGER	⎍	⎎
L	X	H	L→H	TRIGGER	⎍	⎎
X	L	H	L→H	TRIGGER	⎍	⎎
H	H	H	H		L	H
X	X	L	X		L	H
X	X	X	L		L	H

X=DON'T CARE

TRUTH TABLE



OUTPUT PULSE WIDTH (t) IS DEFINED AS FOLLOWS:

$$t = 0.32\ R_x\ C_x \left[1 + \frac{0.7}{R_x}\right]$$

R_x IS IN kΩ, C_x IS IN pF, t IS IN ns

FUNCTION DIAGRAM

161
Rev J
Sheet 1 of 1

DESCRIPTION

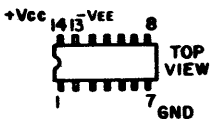
The 162 circuit is a dual differential line receiver. A minimum differential voltage of 25 mV is required to insure a high or low output level. Common mode voltages of ±3V or less will be rejected. The maximum allowable differential input voltage is 5 volts. The 162C features open-collector outputs.

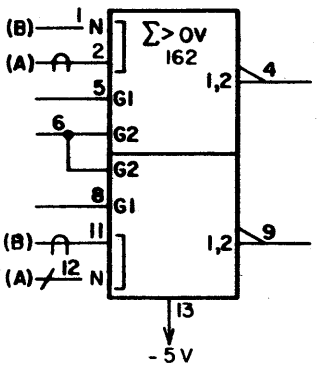
NOTES:

1. The two sections may be shown separately.
2. Vendor identification:

Element	Vendor Number
162	75107
162C	75108 *
162S	NE521F

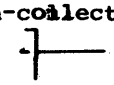
3. Package pin configuration.

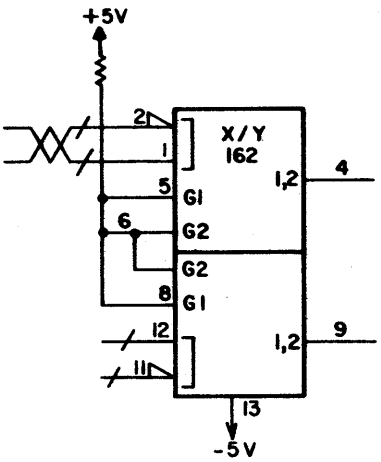




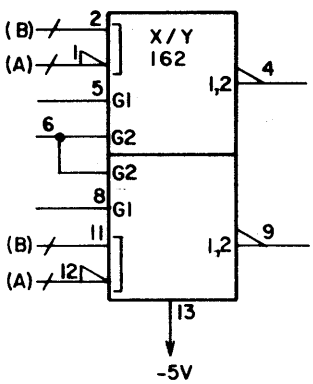
ANALOG TO DIGITAL CONVERTER APPLICATION

* 162C symbol is similar to others, but has the open-collector modifier by each output:

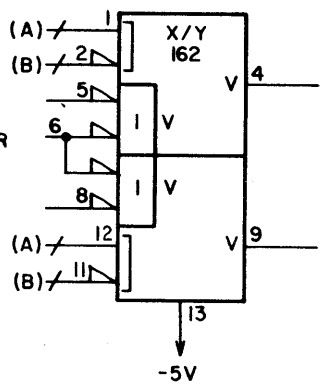


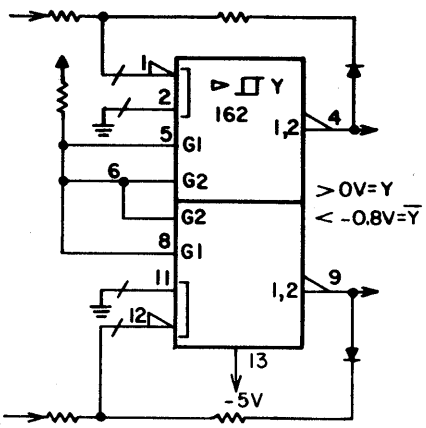


TWISTED PAIR RECEIVER APPLICATION



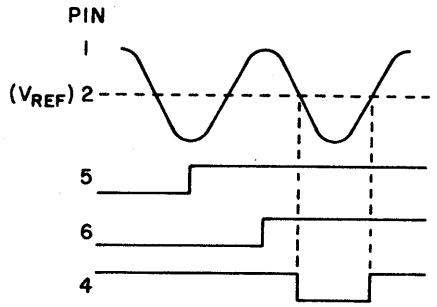
OR





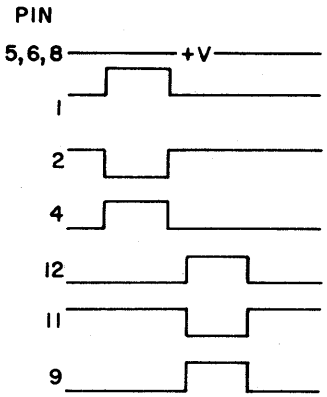
162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING GI AND G2 STROBE INPUTS.

LOGIC SYMBOLS

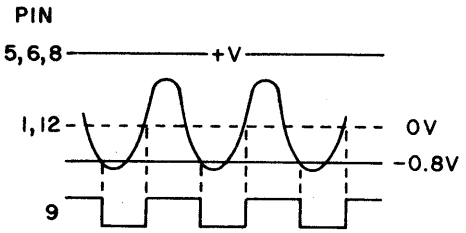


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH AND PIN 1 IS MORE NEGATIVE THAN PIN 2. G2 IS COMMON TO BOTH CONVERTERS.

162 ANALOG TO DIGITAL CONVERTER APPLICATION



162 TWISTED PAIR RECEIVER APPLICATION



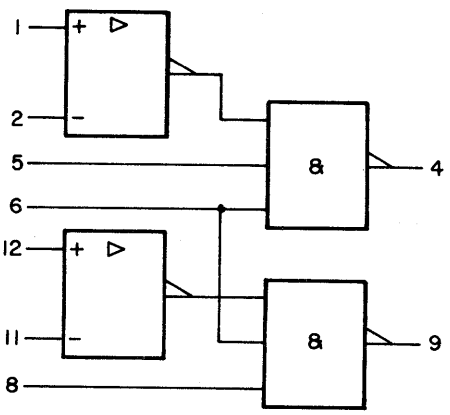
162 SCHMITT TRIGGER

TIMING SEQUENCE

DIFFERENTIAL INPUTS	STROBES		OUTPUT
	G1	G2	
$V_{ID} \geq 25MV$	L OR H	L OR H	H
$-25MV < V_{ID} < 25MV$	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25MV$	L OR H	L	H
	L	L OR H	H
	H	H	L

THE DIFFERENTIAL INPUT VOLTAGE POLARITIES SHOWN MEASURED AT PIN A WITH RESPECT TO PIN B. A MINUS POLARITY INDICATES THAT PIN A IS MORE NEGATIVE THAN PIN B.

TRUTH TABLE
(RCVR APPLICATION)



FUNCTION DIAGRAM

162
Rev J
Sheet 2 of 2

DESCRIPTION

Element 163 is a 4-bit binary counter, the first stage of which is independently clocked. This permits utilizing the first stage as an independent FF while using the other stages as an 8-counter, or using the IC as a 16-counter by cascading the first stage output to the input of the second stage.

For symbol outline and truth table, refer to the data sheet for element 182.

NOTES:

1. Vendor identification: 8281

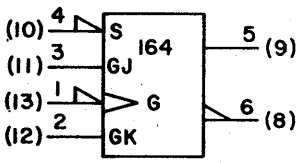
2. Package pin configuration:

   14-pin DIP (see element 182)

163
Rev J
Sheet 1 of 1

DESCRIPTION

The 164 circuit is a dual negative-edge-triggered JK flip-flop. Each flip-flop is provided with a direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions.



LOGIC SYMBOL

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the set-up and hold-times. The inputs are inhibited when the clock is low and enabled when the clock rises. The JK inputs continuously respond to input information when the clock is high. The data state at the inputs throughout the interval between set-up and hold time is stored in the flip-flop when the clock pulse goes low. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input.

INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

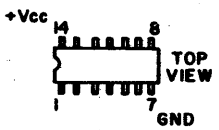
TRUTH TABLE

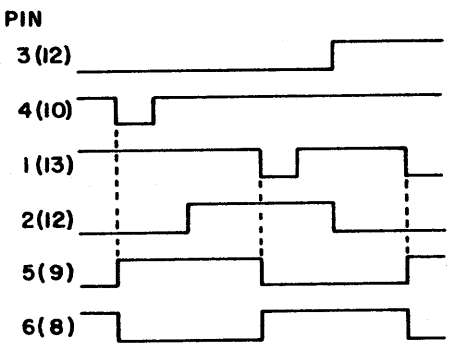
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

Element	Vendor Number
164H	3062
164S	74S113

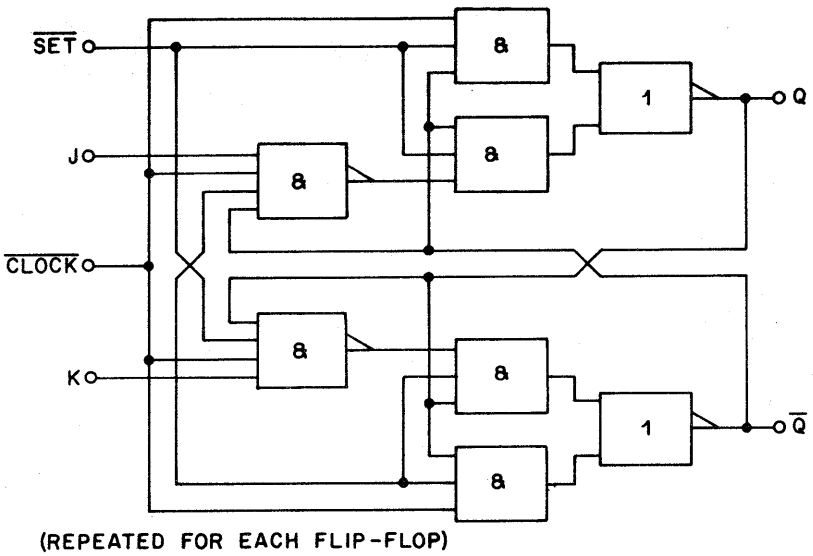
3. Package pin configuration.

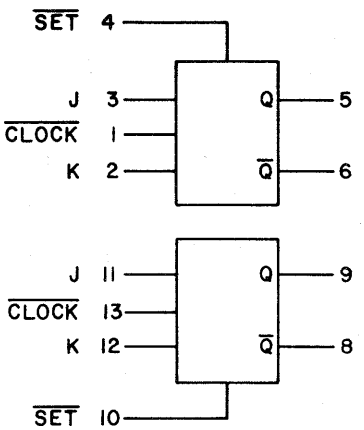




TIMING SEQUENCE

164
Rev J
Sheet 1 of 2





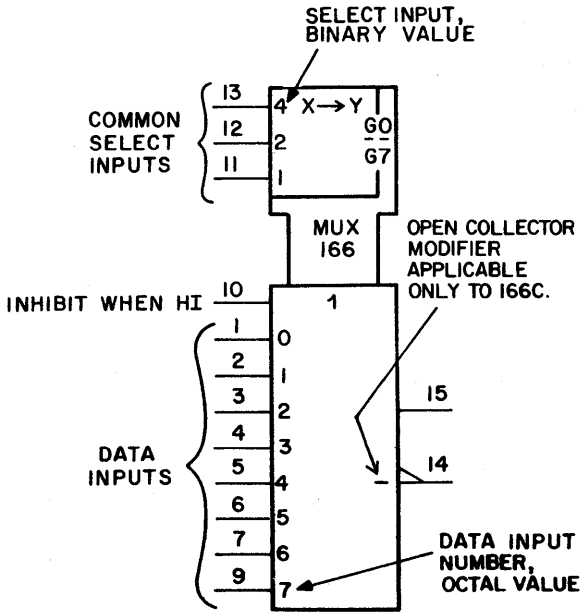
FUNCTION DIAGRAM

164
Rev J
Sheet 2 of 2

DESCRIPTION

The 166 circuit is a 1-of-8 (8-bit) multiplexer that can select one bit of data from up to eight sources. It has complementary outputs, an active low enable, and internal select decoding. With the enable inactive (high), output pin 15 is low and the complementary output pin 14 is high regardless of all input conditions. Data is routed from a particular data input to the outputs according to the binary code applied to the three select inputs.

Element 166C is identical in pin configuration and function, but provides an open-collector output on pin 14.



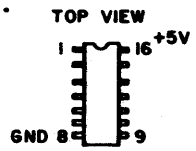
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
166	9312
166C	9313,8231

2. Package Pin configuration.

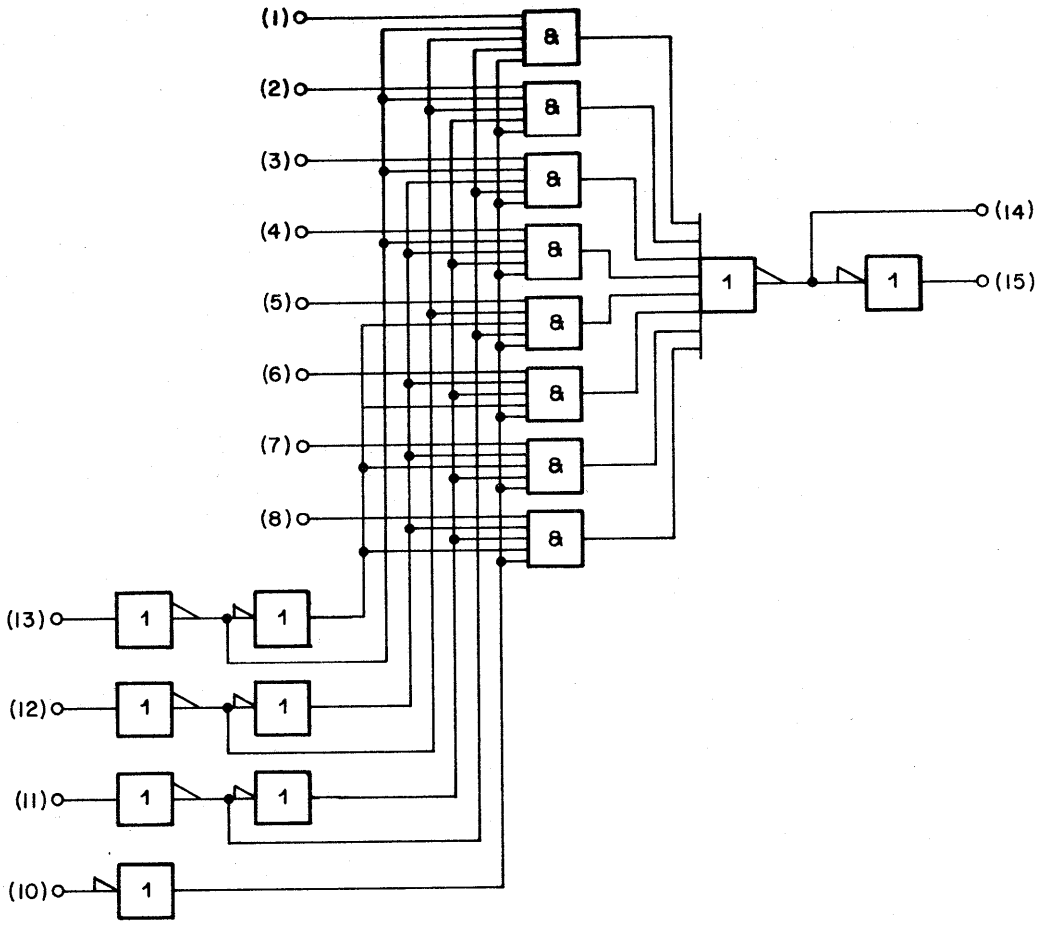


COMMON SELECT PIN			INPUT PIN GATED TO OUTPUT PIN 15 WHEN PIN 10 IS LOW *
13	12	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	9

*PIN 14 OUTPUT IS THE COMPLEMENT OF PIN 15. IF PIN 10 IS HIGH, PIN 15 IS LOW AND PIN 14 IS HIGH, REGARDLESS OF SELECT/DATA INPUTS.

TRUTH TABLE

166
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

166
Rev J
Sheet 2 of 2

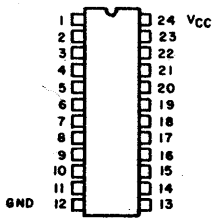
DESCRIPTION

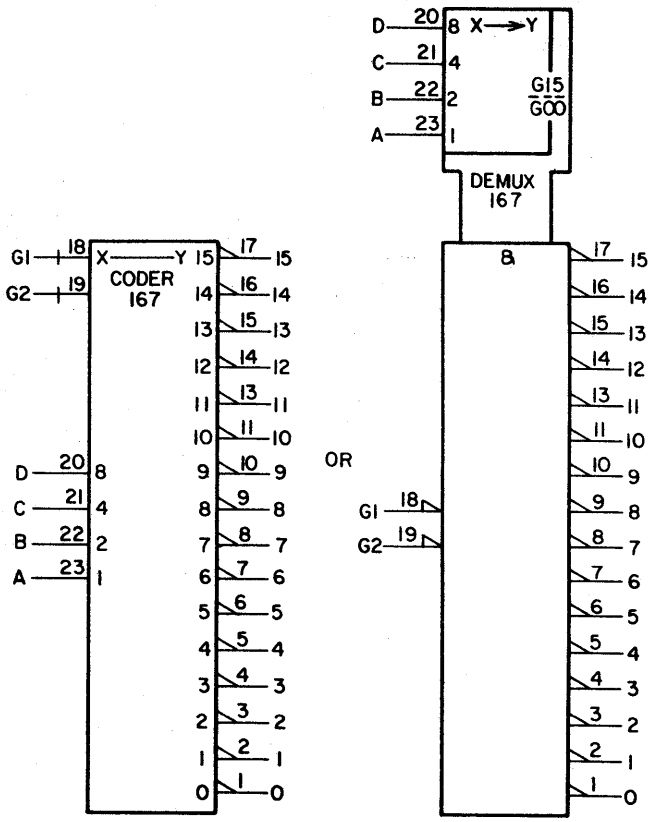
The 167 circuit is a 4-line-to-16-line decoder/demultiplexer. When inputs G1 and G2 are both low, the 167 decodes binary-coded data appearing on inputs A, B, C, and D. As shown in the truth table, one of the outputs 0 through 15 will be low corresponding to the binary coded data on the inputs.

This circuit also performs a demultiplexing function. To do this, it uses the A, B, C, D inputs to address an output, and routes data from the G1 or G2 input to the addressed output. When either G1 or G2 is high, all outputs are high. Thus data may enter at either G1 or G2 with the other input held low.

NOTES:

1. Vendor identification: 74154
2. Package pin configuration:



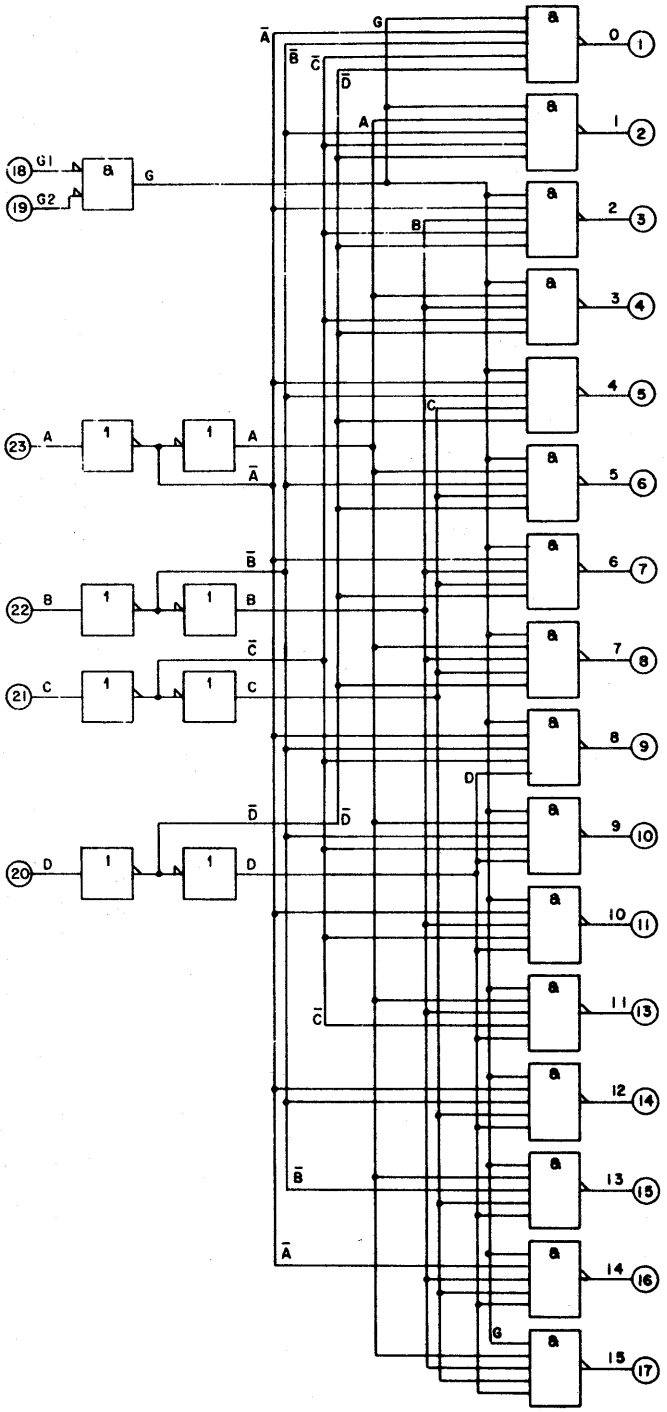


LOGIC SYMBOL

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

TRUTH TABLE

167
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

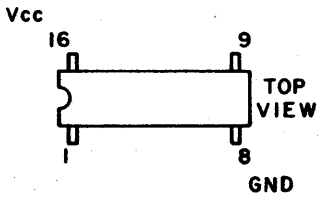
167
Rev J
Sheet 2 of 2

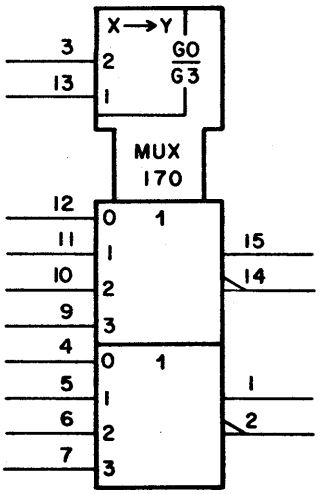
DESCRIPTION

The 170 circuit is a dual 4-input multiplexer. The binary code at select inputs (pins 3 and 13) determines the input selected.

NOTES:

1. Vendor identification: 9309
2. Package pin configuration.





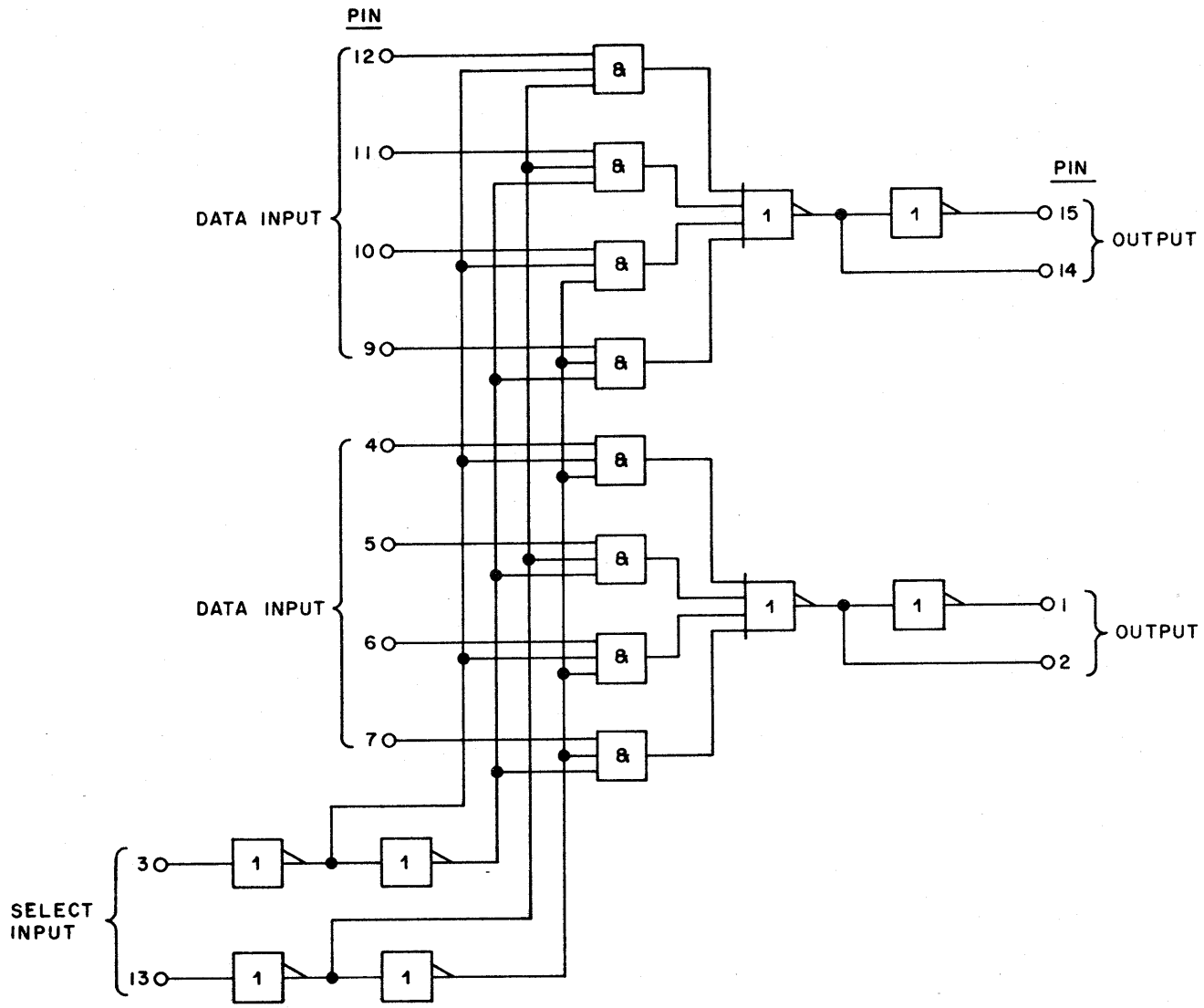
LOGIC SYMBOL

SELECT INPUTS		INPUTS				OUTPUTS	
3	13	4	5	6	7	1	2
		12	11	10	9	15	14
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = HIGH OR LOW LEVEL

TRUTH TABLE

170
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

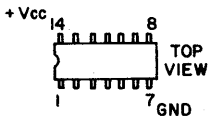
170
Rev J
Sheet 2 of 2

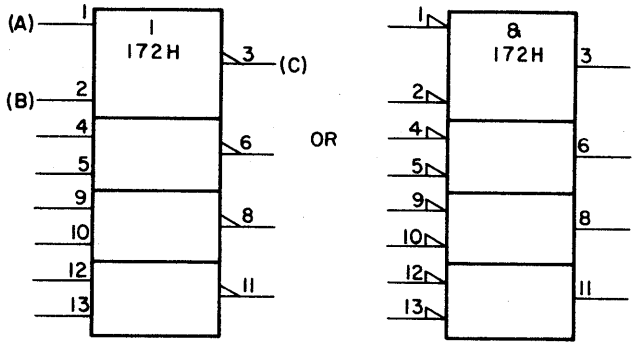
DESCRIPTION

The 172H circuit is a quad, 2-input, positive NOR gate.

NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification: 3002
3. Package pin configuration.





LOGIC SYMBOL

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

TRUTH TABLE

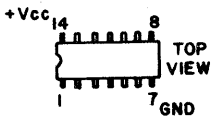
172
Rev J
Sheet 1 of 1

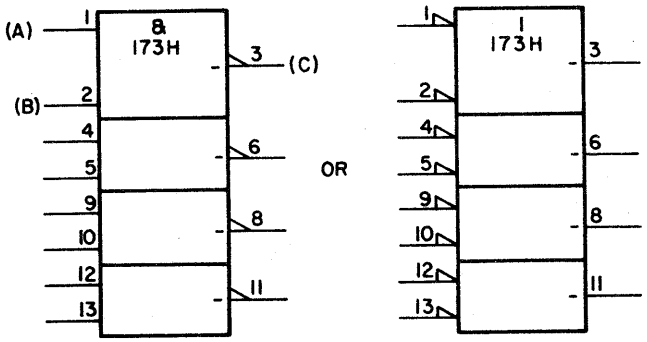
DESCRIPTION

The 173H circuit is a quad, 2-input,positive NAND gate with an open collector output.

NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification: 3004
3. The output of each gate is an open collector.
4. Package pin configuration.





LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE

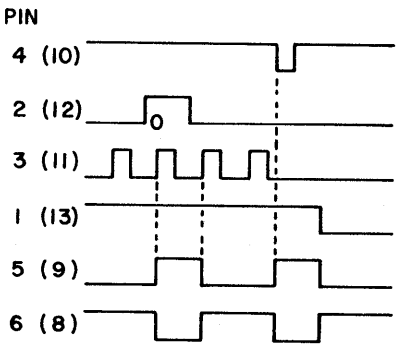
173
Rev J
Sheet 1 of 1

DESCRIPTION

The 175 circuit is a dual, positive-edge-triggered, D-type flip-flop. This device consists of two completely independent D flip-flops, both having direct SET and RESET inputs for asynchronous operations such as parallel data entry in shift register application.

Information at input CD is transferred to output Q (pin 5/9) on the positive-going edge of the clock pulse. Clock pulse triggering occurs at a voltage level of the pulse and is not directly related to the transition time of the positive-going pulse. When the clock is at either the high or low level, the CD-input signal has no effect.

The flip-flop can also be set or cleared directly at any time regardless of the state of the clock by applying a low input to the SET or RESET inputs.



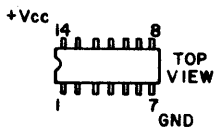
TIMING SEQUENCE

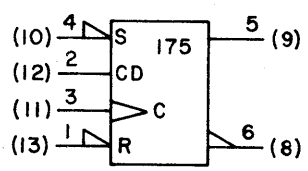
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

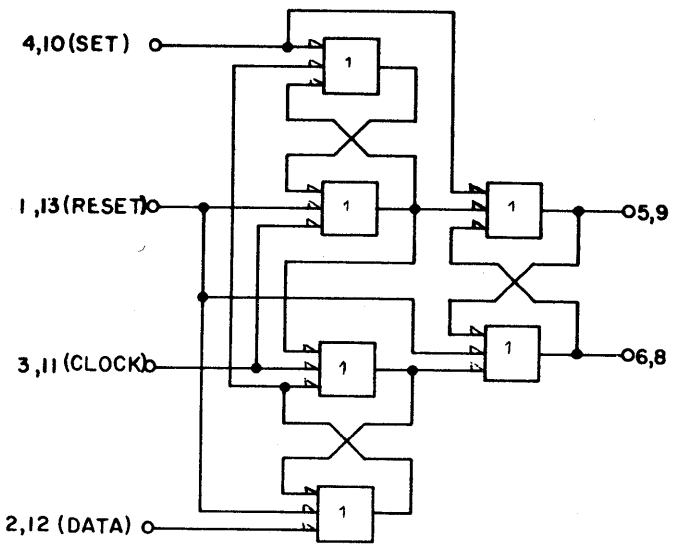
Element	Vendor Number
175	7474
175H	3060
175LS	74LS74
175S	74S74

3. Package pin configuration.





LOGIC SYMBOL



FUNCTION DIAGRAM
(EACH FLIP-FLOP)

175
Rev K
Sheet 1 of 1

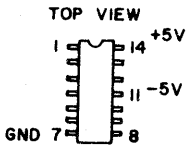
DESCRIPTION

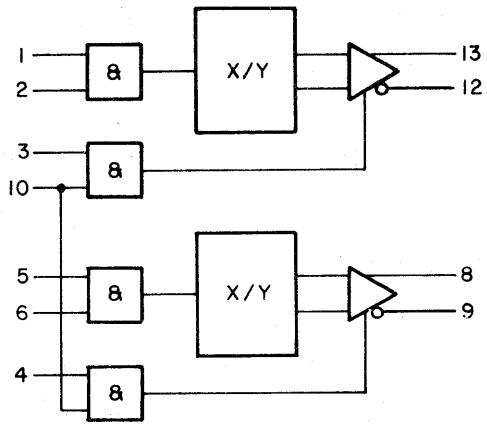
The 176 circuit is a dual, current-mode line driver. Low-active inhibits are provided for each section (pins 3,4) and a third (pin 10) is common to both sections. When both inhibits for a section are high (inactive), a constant-current output is switched to either of the two output pins, depending upon the state of the two DTL/TTL inputs (see truth table). With either inhibit input low, both output pins are switched off.

"On" state output current is typically 12mA. "Off" state output current is 100 μA, max. The output common-mode voltage range is -3V to +10V with respect to circuit ground. Outputs are to a twisted-pair transmission line.

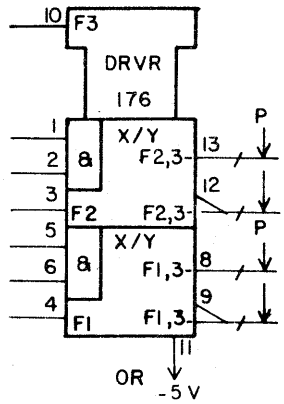
NOTES:

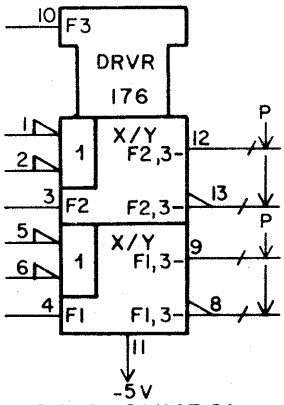
1. Type 176 Vendor identification: 75110
2. Package pin configuration.



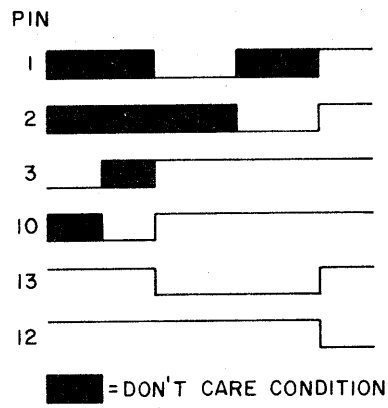


FUNCTION DIAGRAM





LOGIC SYMBOL



TIMING SEQUENCE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS *		OUTPUT CONDITION
1, 5	2, 6	3, 4	10	9, 12	8, 13	
X	X	L	X	OFF	OFF	INHIBITED
X	X	X	L	OFF	OFF	
L	X	H	H	ON	OFF	ACTIVE DATA STATE
X	L	H	H	ON	OFF	
H	H	H	H	OFF	ON	

L = LOW, H = HIGH, X = DON'T CARE

TRUTH TABLE

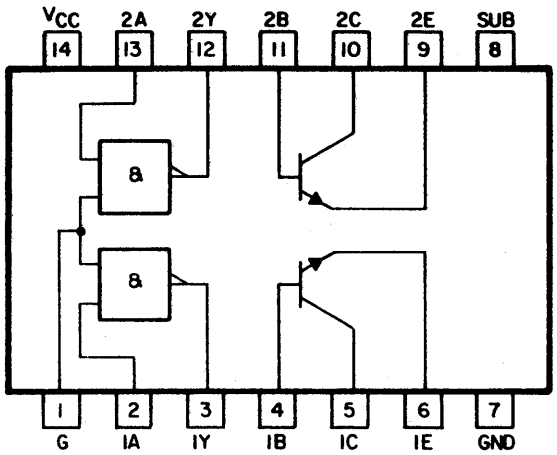
176
REV L
Sheet 1 of 1

DESCRIPTION

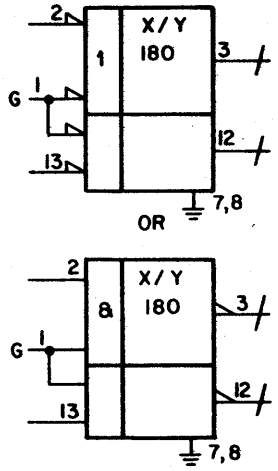
Element 180 consists of two positive NAND drivers with a common strobe (G), as shown in the Basic Symbol. The package also provides two high-current, high-voltage n-p-n transistors with separate pin-outs. The representation of the transistor-only function depends upon how each transistor is connected (see Supplemental Symbols).

NOTES:

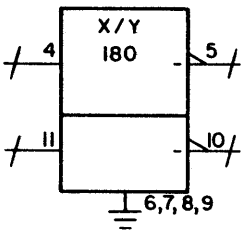
1. Vendor identification: 75450A
2. Package pin configuration and functional diagram:



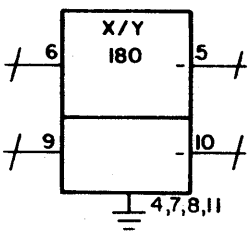
TOP VIEW



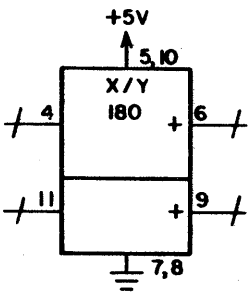
BASIC SYMBOL



GROUNDED EMITTER



GROUNDED BASE



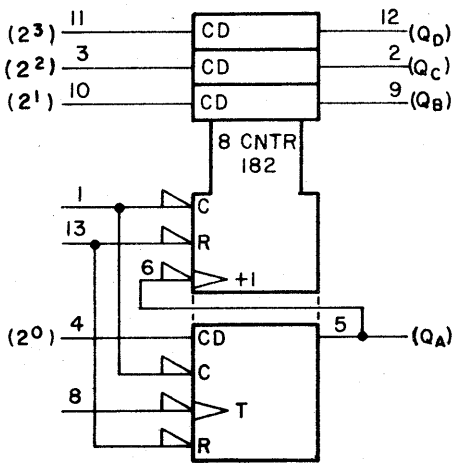
EMITTER FOLLOWER

SUPPLEMENTAL SYMBOLS

180
Rev J
Sheet 1 of 1

DESCRIPTION

Circuit type 182 is a 4-bit binary counter. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The direct clear (pin 13), when taken low, sets all outputs low regardless of the states of the clocks (pins 8 and 6). The 182 is fully programmable; that is, the counter may be preset to any state by placing a low ("0") on the count/load input (pin 1) and entering the desired data at the inputs. The outputs will then change to agree with the data inputs independent of the state of the clock inputs. This allows the 182 to be used as a 4-bit latch (register application) by inactivating the clock inputs and using the count/load input as a data strobe.



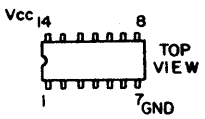
LOGIC SYMBOL

NOTES:

1. Vendor identification:

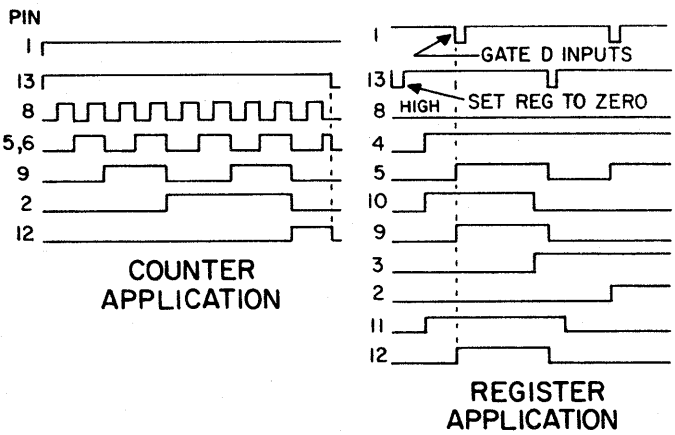
Element	Vendor Number
182	74197,8291
182S	82S91

2. Package pin configuration.



COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

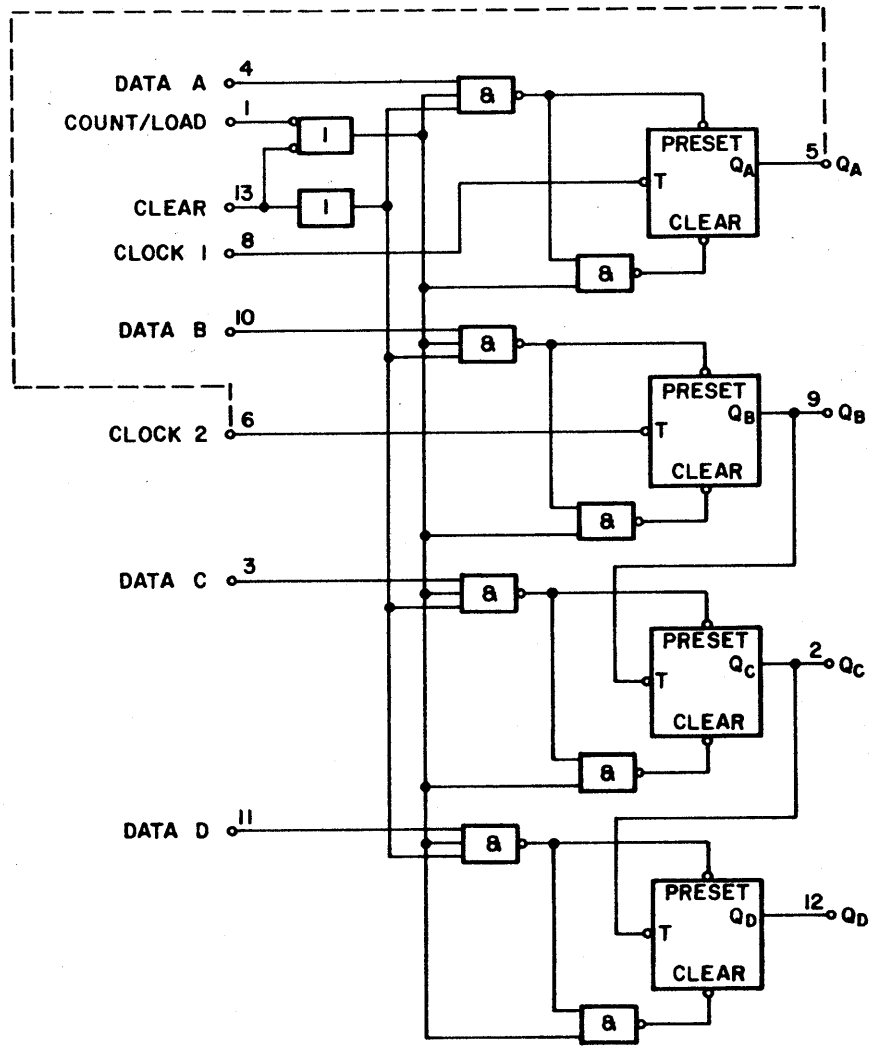
TRUTH TABLE
(WITH PINS 5 AND 6 WIRED TOGETHER)



TIMING SEQUENCE

182
Rev J
Sheet 1 of 2

CONNECT PINS 5 & 6 FOR 4-BIT COUNTING, USING DATA INPUT A. AS A 3-BIT COUNTER, DATA INPUT B IS USED. FIRST STAGE MAY THEN BE USED AS AN INDEPENDENT DATA LATCH IF COUNT/LOAD AND CLEAR FUNCTIONS COINCIDE WITH THOSE OF THE COUNTER.



FUNCTION DIAGRAM

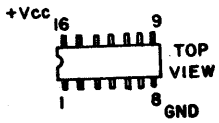
182
Rev J
Sheet 2 of 2

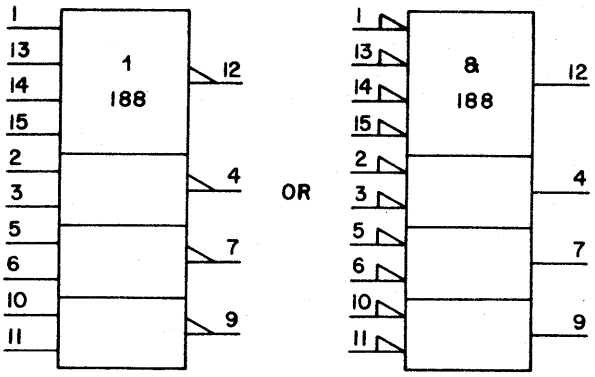
DESCRIPTION

The 188 circuit consists of one 4-input and three 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 9015
3. Package pin configuration.





LOGIC SYMBOL

188
Rev J
Sheet 1 of 1

DESCRIPTION

Circuit type 189 is a quad 1-of-2 (2-input) multiplexer.

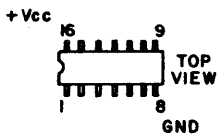
When the inhibit (pin 15) is high all outputs are held low.

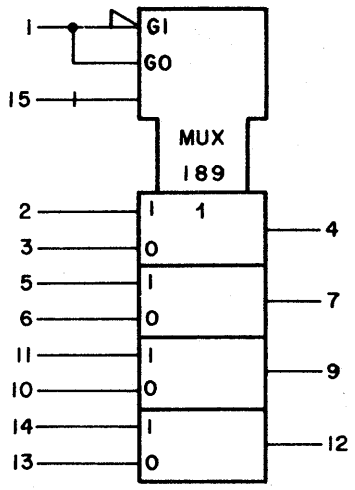
NOTES:

1. Vendor identification:

Element	Vendor Number
189	74157/9322
189L	74L157
189LS	74LS157
189S	74S157

2. Package pin configuration.

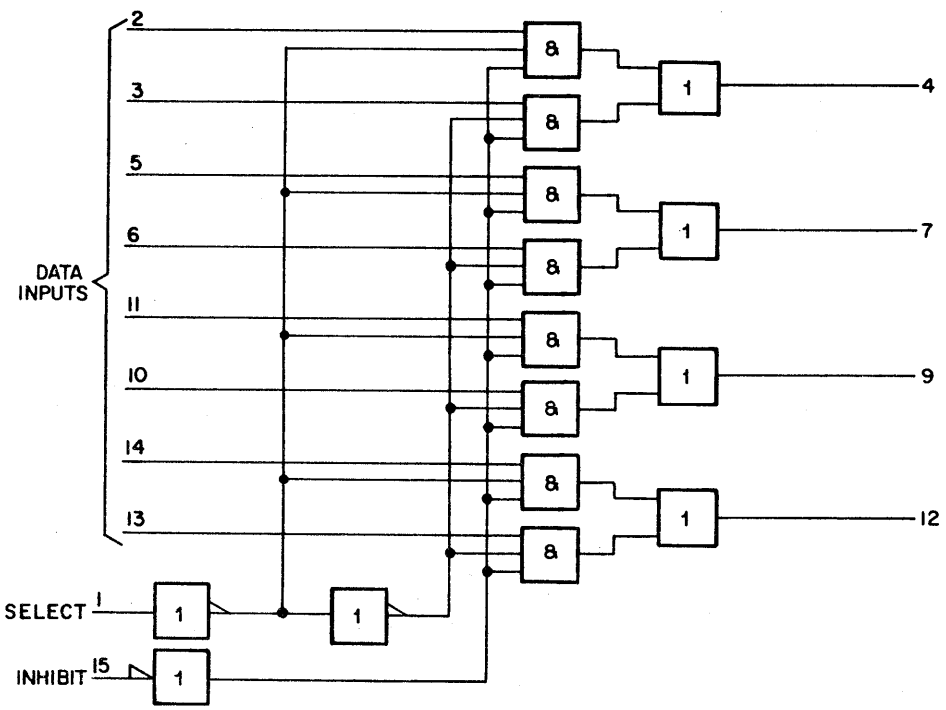




LOGIC SYMBOL

INH	SEL	INPUTS		OUTPUT
		1	0	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

TRUTH TABLE
(ANY SECTION)
L = LOW LEVEL
H = HIGH LEVEL
X = IRRELEVANT



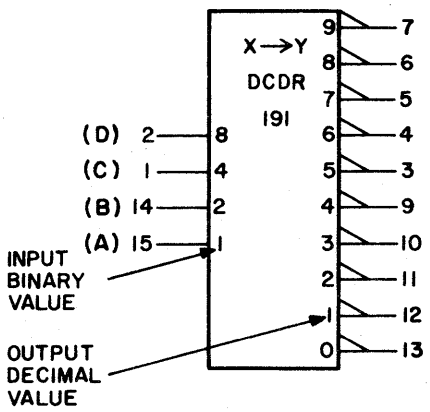
FUNCTION DIAGRAM

189
Rev J
Sheet 1 of 1

DESCRIPTION

Circuit type 191 is a BCD-to-decimal (1-of-10) decoder. Four active-high BCD inputs provide one of ten mutually exclusive active-low outputs. When a binary code greater than 9 is applied, all outputs are high. This facilitates BCD to decimal conversions and eight-channel demultiplexing and decoding.

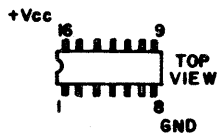
The 191 circuit can serve as a one-of-eight decoder with the D input acting as the active-low enable. Eight-channel demultiplexing then results when the desired output is addressed by inputs A, B, and C.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 9301
2. Package pin configuration.

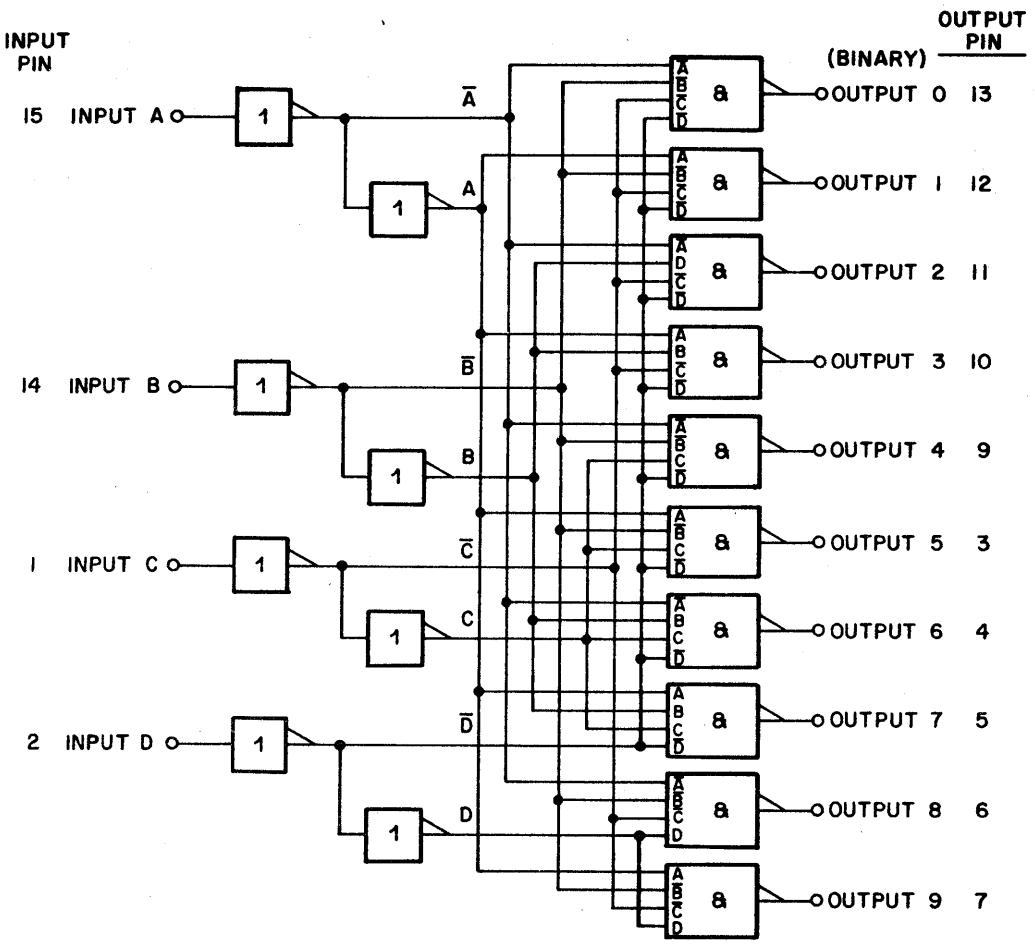


INPUT PIN				LO ("0") OUTPUT PIN (OTHER OUTPUTS = "1")
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	X

* = ALL OUTPUT PINS HIGH

TRUTH TABLE

191
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

191
Rev J
Sheet 2 of 2

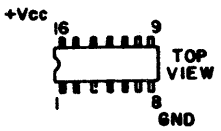
DESCRIPTION

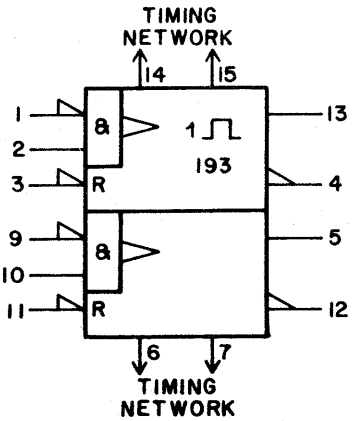
The 193 circuit is a two-section retriggerable monostable multivibrator. Triggering the input before the output pulse is terminated extends the output pulse duration. The overriding clear input (pin 3/11) immediately terminates any output pulse.

Successive inputs having a cycle time shorter than the delay time produce a constant high output from pin 13/5.

NOTES:

1. Vendor identification: 74123
2. Package pin configuration.

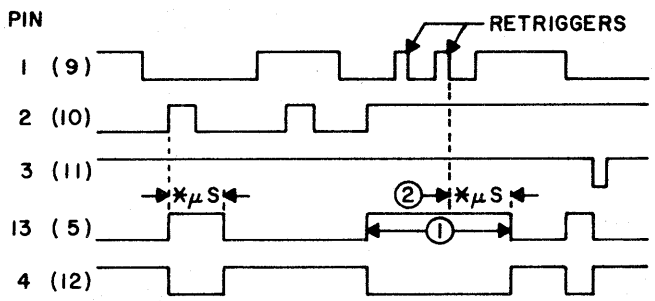




LOGIC SYMBOL

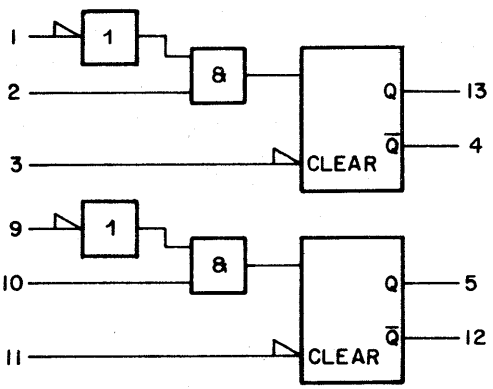
INPUT PINS		OUTPUT PINS	
1 (9)	2 (10)	13 (5)	4 (12)
H	X	L	H
X	L	L	H
L	↑	⊓	⊓
↓	H	⊓	⊓

TRUTH TABLE



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.
① OUTPUT HELD HIGH DURING RETRIGGER PULSE.
② OUTPUT TIMES OUT FROM EDGE OF LAST TRIGGER PULSE.

TIMING SEQUENCE

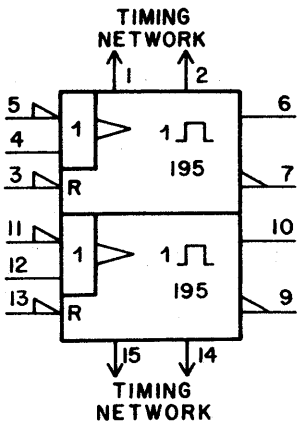


FUNCTION DIAGRAM

193
Rev J
Sheet 1 of 1

DESCRIPTION

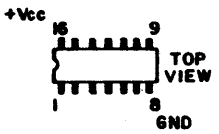
The 195 circuit is a dual retriggerable monostable multivibrator. Input pins 4 and 12 trigger on the positive-going edge of the input pulse and pins 5 and 11 trigger on the negative-going edge. The 195 circuit will retrigger while in the pulse timing state (pin 3/13 high) and the end of the last pulse will be timed from the last input. A low level to the reset input (pin 3/13) resets pin 6/10 to low level and inhibits data inputs.



LOGIC SYMBOL

NOTES:

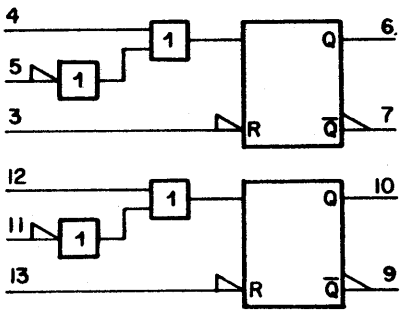
1. The full timing network would be shown on the logic diagram.
2. Vendor identification: 9602
3. Package pin configuration.



4. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low level pulse, X = irrelevant (any input, including transitions).
5. Output pulse width (t) is defined as follows:

$$t = 0.32\ R_x\ C_x \left[1 + \frac{0.7}{R_x}\right]$$

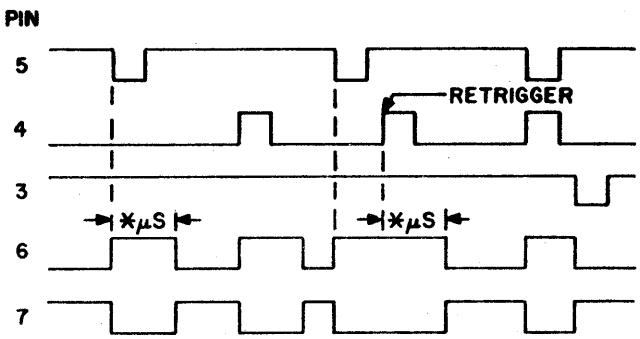
R_x is in kΩ, C_x is in pF t is in ns



FUNCTION DIAGRAM

INPUT PINS			OUTPUT PINS	
5(11)	4(12)	3(13)	6(10)	7 (9)
↓	L	H	⎍	⎏
H	↑	H	⎍	⎏
X	X	L	L	H

TRUTH TABLE
(SEE NOTE 4)



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.

TIMING SEQUENCE

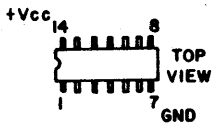
195
Rev J
Sheet 1 of 1

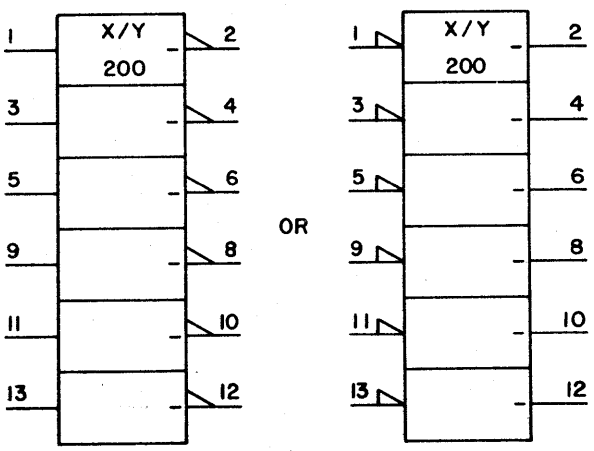
DESCRIPTION

The 200 circuit is a hex inverter buffer/ driver with an open-collector output.

NOTES:

1. Symbol sections may be shown separately.
2. Vendor identification: 7406
3. Package pin configuration.





LOGIC SYMBOL

200
Rev J
Sheet 1 of 1

DESCRIPTION

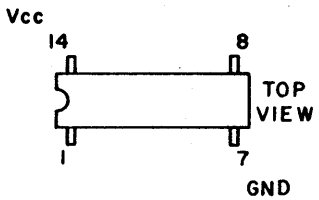
The 201 circuit is a quad, 2-input, positive AND gate. Version 201C provides open-collector outputs.

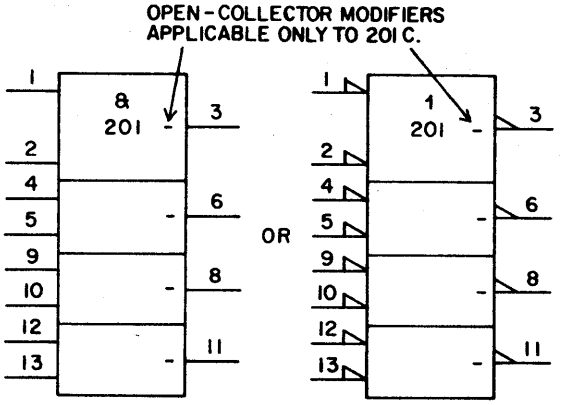
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
201	7408
201H	74H08
201L	74L08
201LS	74LS08
201C	7409

3. Package pin configuration.





LOGIC SYMBOL

INPUT	OUTPUT
0 0	0
0 1	0
1 0	0
1 1	1

TRUTH TABLE
(FOR ONE GATE)

201
Rev J
Sheet 1 of 1

DESCRIPTION

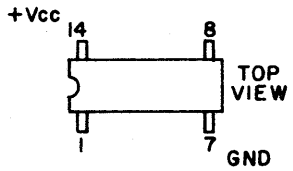
The 202 circuit is an quad, 2-input,positive NAND gate with an open-collector output.

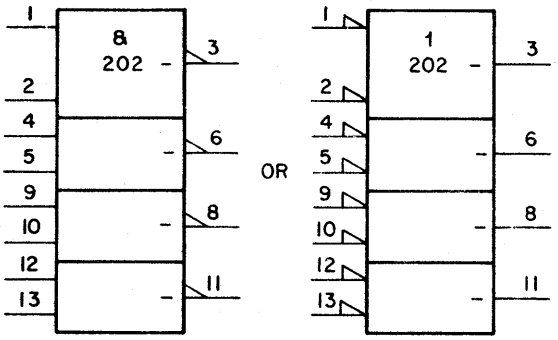
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

Element	Vendor Number
202	7403
202H	74H01
202LS	74LS03
202S	74S03

3. Package pin configuration.

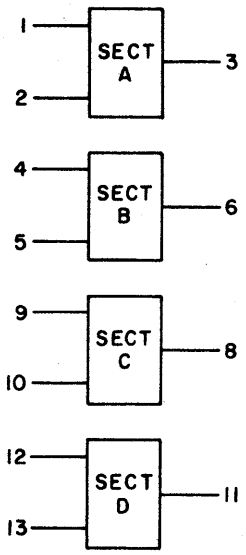




LOGIC SYMBOL

INPUT	OUTPUT
0 0	1
0 1	1
1 0	1
1 1	0

TRUTH TABLE



FUNCTION DIAGRAM

202
Rev J
Sheet 1 of 1

DESCRIPTION

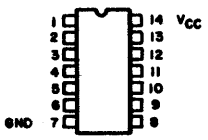
The 203 circuit consists of six individual inverters with open-collector outputs. Each output must be connected to an external pull-up resistor tied to VCC. Each inverter performs the function $Y=\overline{A}$.

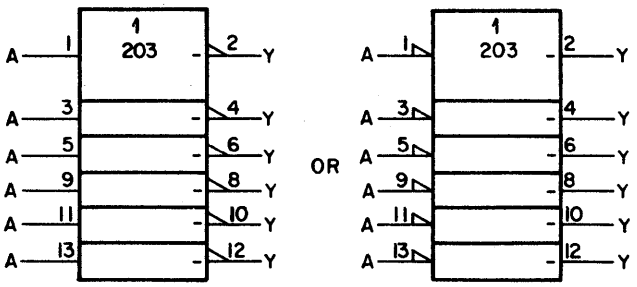
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
203	7405
203H	74H05
203LS	74LS05
203S	74S05

3. Package pin configuration:





LOGIC SYMBOL

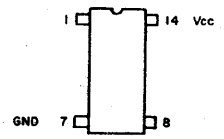
203
Rev J
Sheet 1 of 1

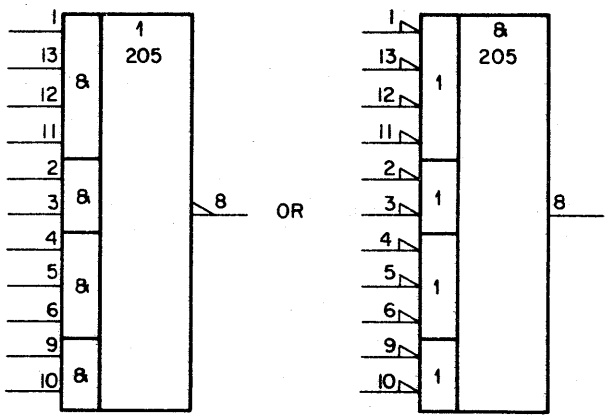
DESCRIPTION

The 205S circuit is a 4-2-3-2-input AND-OR-INVERT gate.

NOTES:

1. Vendor identification: 74S64
2. Package pin configuration:





LOGIC SYMBOL

205
Rev J
Sheet 1 of 1

DESCRIPTION

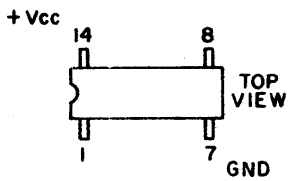
Element 206 is an 8-input,positive NAND gate.

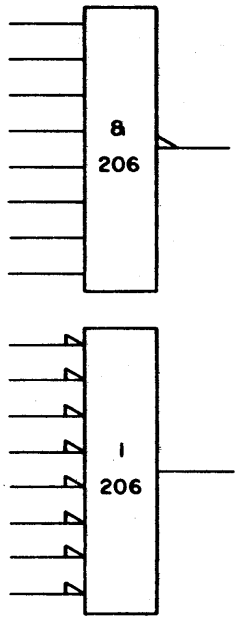
NOTES:

1. Vendor identification:

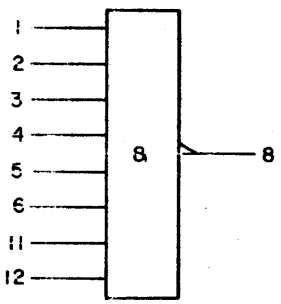
Element	Vendor Number
206	7430
206H	74H30
206L	74L30
206LS	74LS30
206S	74S30

2. Package pin configuration.





LOGIC SYMBOL



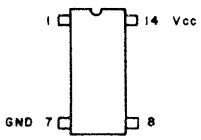
206
Rev J
Sheet 1 of 1

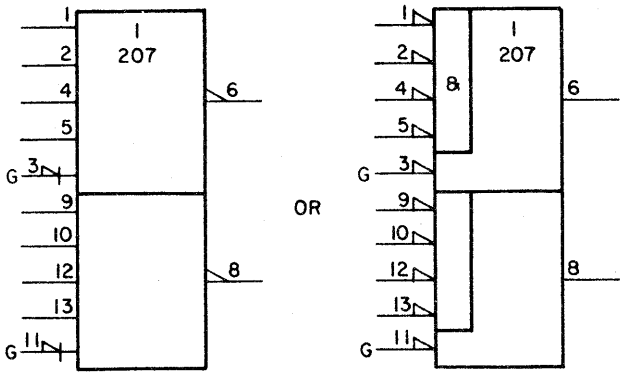
DESCRIPTION

The 207 circuit is a dual, 4-input, positive NOR gate with a separate strobe input (G) for each section.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 7425
3. Package pin configuration:

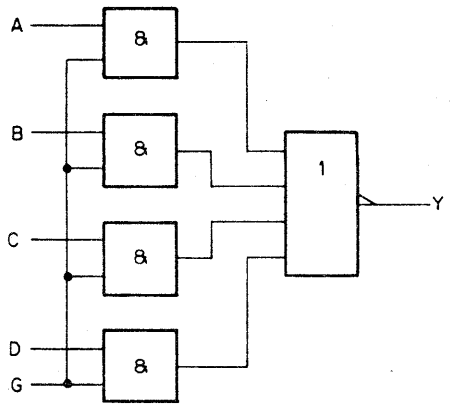




LOGIC SYMBOL

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

TRUTH TABLE



FUNCTIONAL DIAGRAM
(HIGH ACTIVE LOGIC)

207
Rev J
Sheet 1 of 1

DESCRIPTION

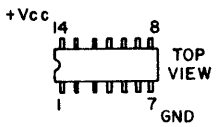
Type 208 is a dual, 4-input, positive NAND gate.

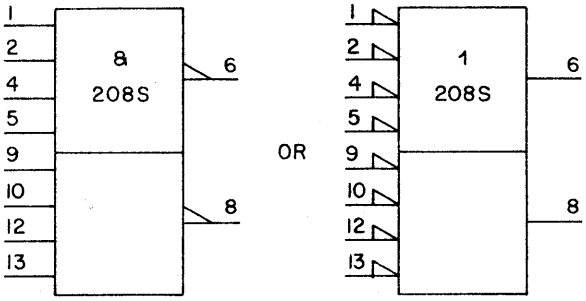
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
208	7420
208H	74H20
208L	74L20
208LS	74LS20
208S	74S20

3. Package pin configuration.





LOGIC SYMBOL

INPUTS				OUTPUT
A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE

208
Rev J
Sheet 1 of 1

DESCRIPTION

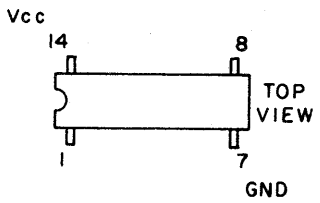
The 209 circuit is a 4-wide, 2-input AND-OR-INVERT gate. Expander gates can be connected to pins 11 and 12, otherwise these pins are left open.

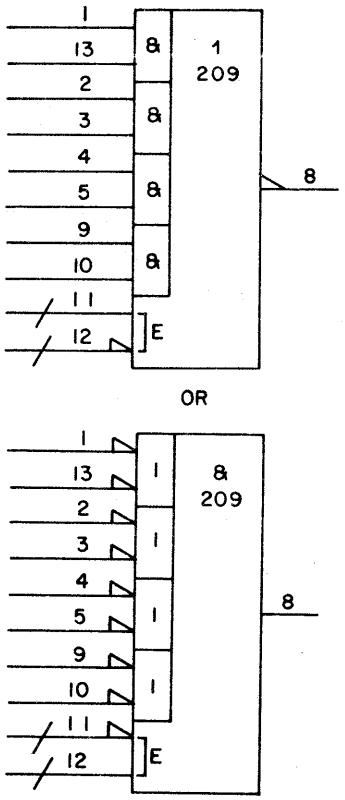
NOTES:

1. Vendor identification:

Element	Vendor Number
209	7453
209H	74H53

2. Package pin configuration.



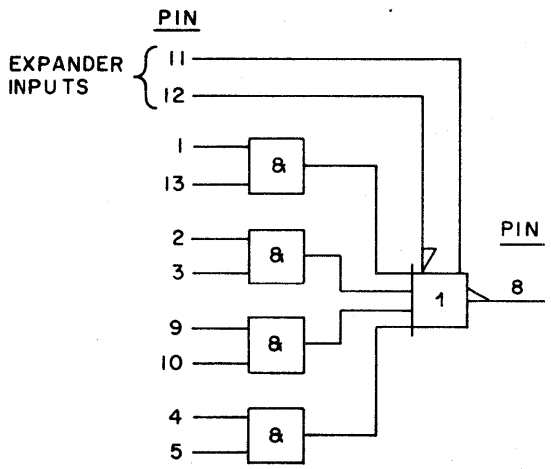


LOGIC SYMBOL

INPUT PINS								OUTPUT
1	13	2	3	9	10	4	5	8
H	H	X	X	X	X	X	X	L
X	X	H	H	X	X	X	X	L
X	X	X	X	H	H	X	X	L
X	X	X	X	X	X	H	H	L
L	X	L	X	L	X	L	X	H

H=HIGH LEVEL
L=LOW LEVEL
X=EITHER HIGH OR LOW LEVEL

TRUTH TABLE



FUNCTION DIAGRAM

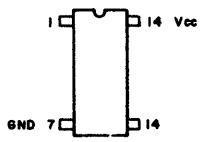
209
Rev J
Sheet 1 of 1

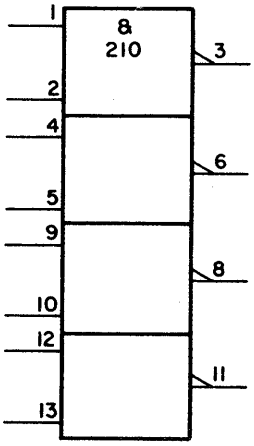
DESCRIPTION

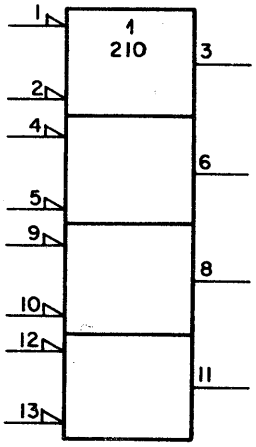
The 210 circuit is a quad, 2-input, positive NAND buffer. The buffered output provides a maximum fan-out of 30 for each section.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 7437
3. Package pin configuration:







210
Rev J
Sheet 1 of 1

DESCRIPTION

The 212 circuit is a dual, 4-input, positive AND gate.

The AND function is: $Y=ABCD$

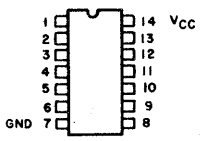
The OR function is: $\overline{Y}=\overline{A}+\overline{B}+\overline{C}+\overline{D}$

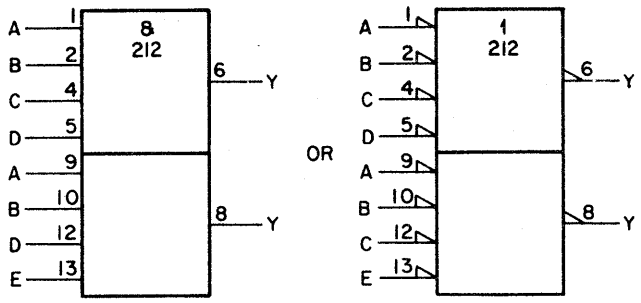
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
212	7421
212H	74H21

3. Package pin configuration:





LOGIC SYMBOL

212
Rev J
Sheet 1 of 1

DESCRIPTION

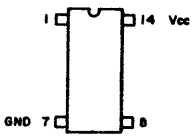
Element 213 is a triple, 3-input, positive AND gate.

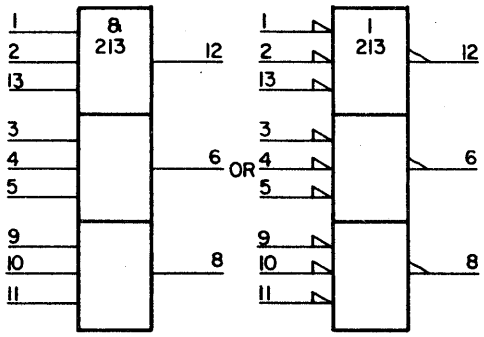
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
213H	74H11
213LS	74LS11
213S	74S11

3. Package pin configuration:



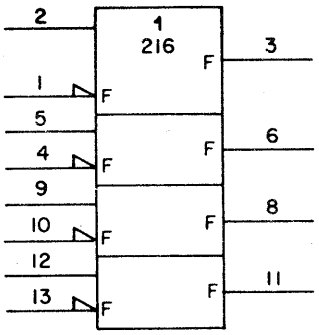


LOGIC SYMBOL

213
Rev J
Sheet 1 of 1

DESCRIPTION

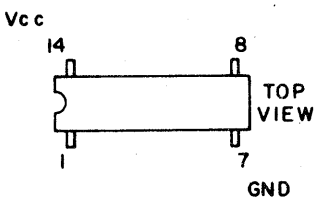
Circuit type 216 is a three-state, quad, 2-input buffer. Each buffer section has a control input and data input. A low level at the control input pin enables non-inverting data to pass through from the data input pin. A high level at the control input pin switches the buffer to the high impedance state, thus inhibiting signals applied to the data input pin. Input data applied to the buffer output pin also sees a high impedance; this is significant in applications that transmit in both directions on a common line.



LOGIC SYMBOL

NOTES:

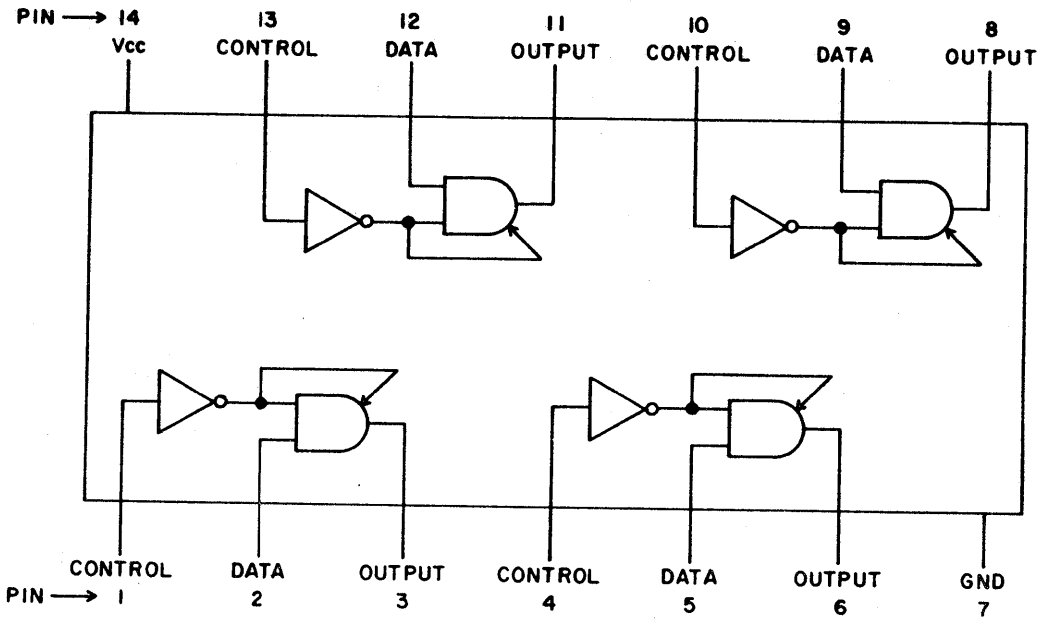
1. Symbol sections may appear separately.
2. Vendor identification: 8093
3. Package pin configuration.



DATA	CONTROL	OUTPUT
PIN 2	PIN 1	PIN 3
H	L	H
L	L	L
X	H	Hi-Z

X = EITHER HIGH OR LOW LEVEL
Hi-Z = HIGH IMPEDANCE STATE

TRUTH TABLE
(FOR ONE SECTION)



FUNCTION DIAGRAM

216
Rev J
Sheet 2 of 2

DESCRIPTION

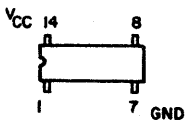
Element 218 is a quad, 2-input, positive OR gate.

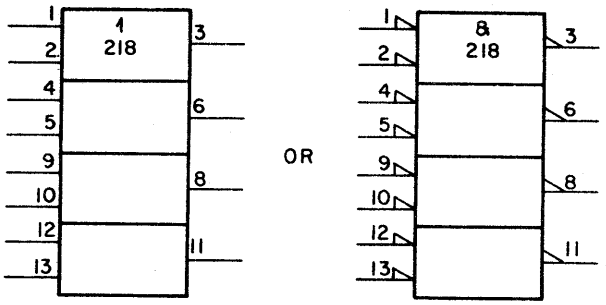
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
218	7432
218H	3003
218LS	74H32

3. Package pin configuration.





LOGIC SYMBOL

218
Rev J
Sheet 1 of 1

DESCRIPTION

The 220H circuit is an expandable, 2-wide, positive AND-OR-INVERT (AOI) gate. The number of inputs can be increased by an external "expander" circuit (e.g. 214H) that, in essence, shorts inputs X and $\overline{X}$. If the expansion feature is not used, X and $\overline{X}$ must be left open.

For AOI, the circuit function is:

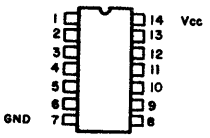
$$Y=\overline{ABCD+EFGH+X}.$$

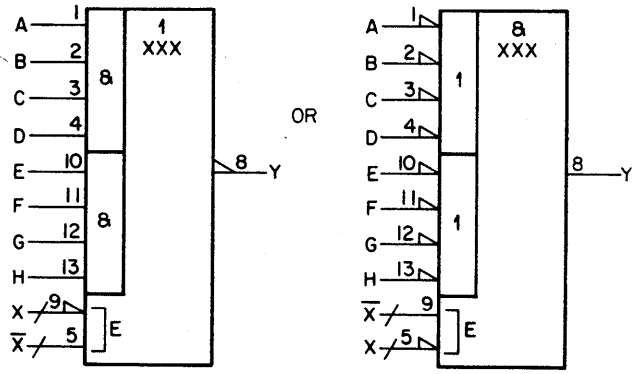
For OAI, the circuit function is:

$$Y=\overline{(A+B+C+D)(E+F+G+H)X}.$$

NOTES:

1. Vendor identification: 74H55
2. Package pin configuration:





LOGIC SYMBOL

INPUTS									OUTPUT
A	B	C	D	E	F	G	H	X	Y
X	X	X	X	X	X	X	X	H	L
X	X	X	X	H	H	H	H	X	L
H	H	H	H	X	X	X	X	X	L
L	X	X	X	←Z→				L	H
X	L	X	X	←Z→				L	H
X	X	L	X	←Z→				L	H
X	X	X	L	←Z→				L	H
←Z→				L	X	X	X	L	H
←Z→				X	L	X	X	L	H
←Z→				X	X	L	X	L	H
←Z→				X	X	X	L	L	H

H = HIGH X = DONT CARE
L = LOW Z = ANY INPUT LOW

TRUTH TABLE
(AND-OR-INVERT ONLY)

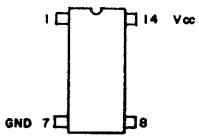
220
Rev J
Sheet 1 of 1

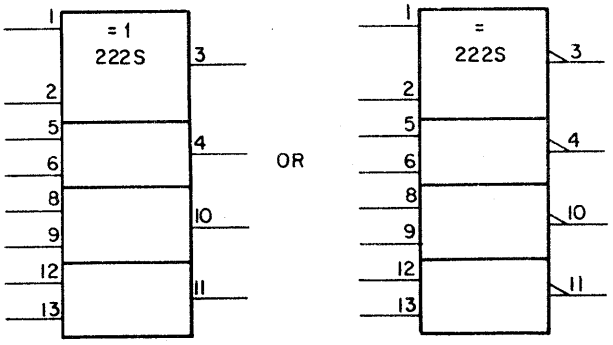
DESCRIPTION

Element 222S is a quad, 2-input, positive Exclusive OR. The 222S may also be used as an equivalence gate for low-active outputs.

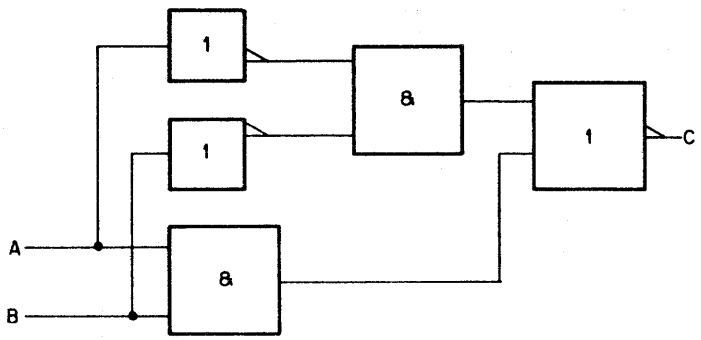
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 82S41
3. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM
(ONE SECTION)

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0

TRUTH TABLE

222S
Rev J
Sheet 1 of 1

DESCRIPTION

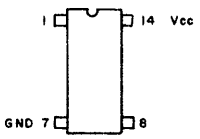
Element 223 is a dual, 2-wide, positive AND-OR-INVERT gate.

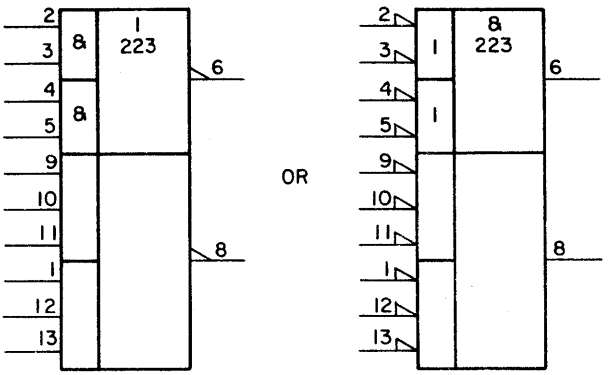
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
223L	74L51
223P	74LS51

3. Package pin configuration:





LOGIC SYMBOL

223
Rev J
Sheet 1 of 1

DESCRIPTION

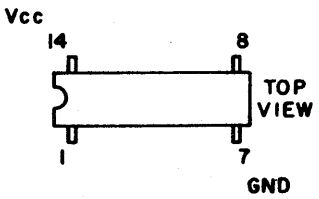
The 224 circuit is a triple, 3-input, positive NOR gate.

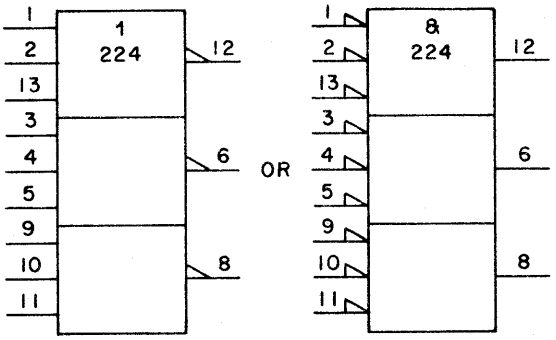
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
224	7427
224LS	74LS27

3. Package pin configuration.





LOGIC SYMBOL

INPUT			OUTPUT
1	2	13	12
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

TRUTH TABLE
(FOR ONE GATE)

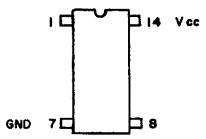
224
Rev J
Sheet 1 of 1

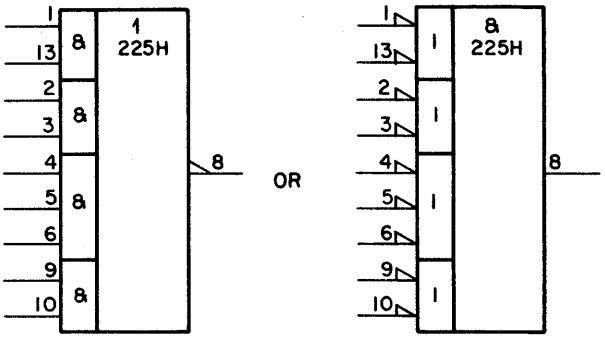
DESCRIPTION

Element 225H is a positive AND-OR-INVERT gate with a 2-2-3-2 input configuration.

NOTES:

1. Vendor identification: 74H54
2. Package pin configuration:





LOGIC SYMBOL

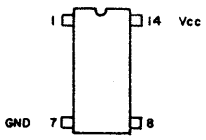
225
Rev J
Sheet 1 of 1

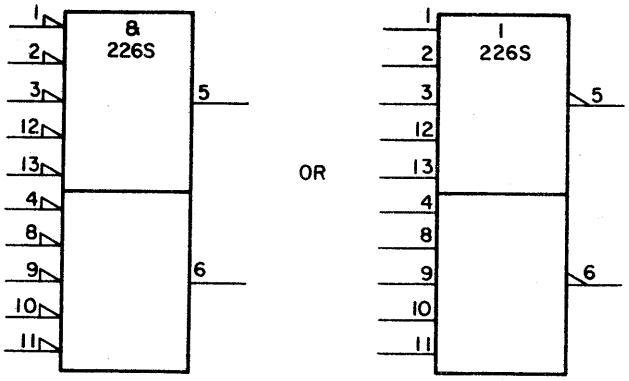
DESCRIPTION

Element 226S consists of two 5-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74S260
3. Package pin configuration:



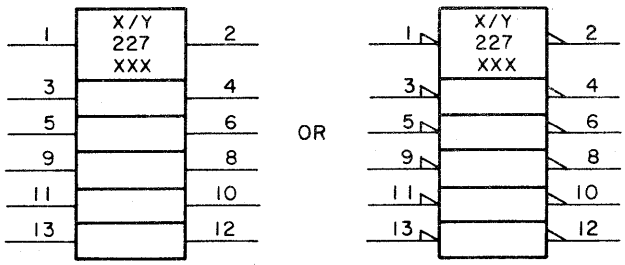


LOGIC SYMBOL

226
Rev J
Sheet 1 of 1

DESCRIPTION:

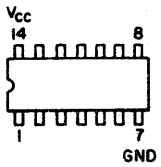
Element 227 is a hex buffer/driver with TTL-compatible inputs and open-collector outputs. The high output voltages are suitable for interfacing to high-level inputs such as CMOS, or for driving high-current loads such as lamps or relays. The 7407 may also be used as a buffer to other TTL inputs.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 7407
2. Package pin configuration:



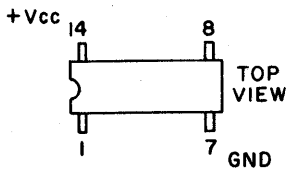
227
Rev. J
Sheet 1 of 1

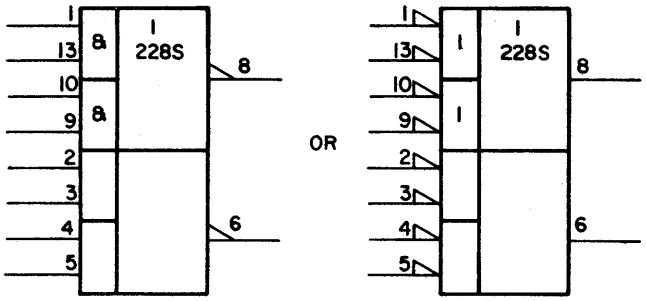
DESCRIPTION

Element 228S is a dual, 2-wide, 2-input AND-OR-INVERT gate.

NOTES:

1. Vendor identification: 74S51
2. Package pin configuration:





LOGIC SYMBOL

228
Rev J
Sheet 1 of 1

DESCRIPTION

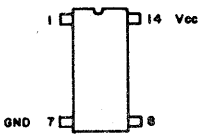
Element 229 consists of four 2-input AND gates with open-collector outputs.

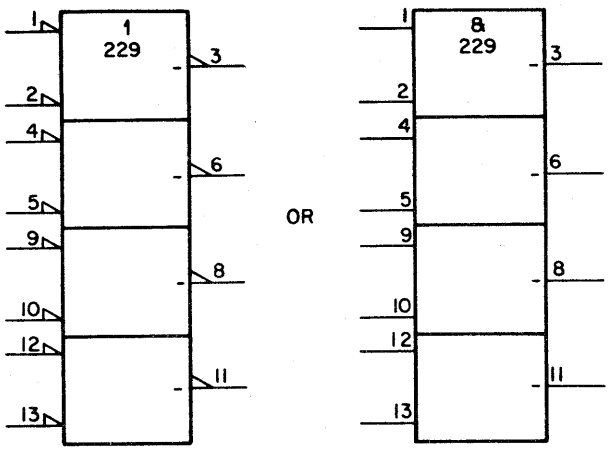
NOTES

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
229LS	74LS09
229S	74S09

3. Package pin configuration:





LOGIC SYMBOL

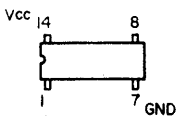
229
Rev J
Sheet 1 of 1

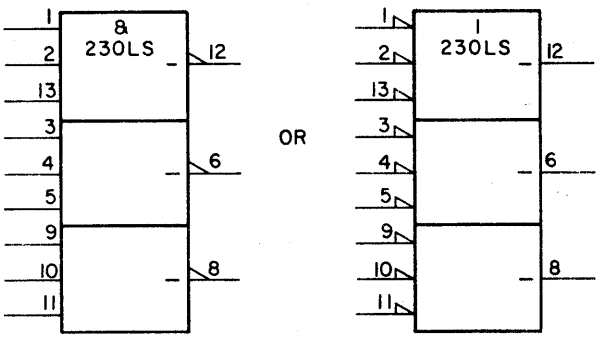
DESCRIPTION

Element 230LS is a triple, 3-input, positive NAND gate with open-collector outputs.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74LS12
3. Package pin configuration:





LOGIC SYMBOL

230LS
Rev J
Sheet 1 of 1

DESCRIPTION

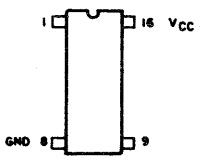
The 233 circuit is a dual monostable multivibrator (one shot) with Schmitt-trigger inputs. Each section features a positive-transition-triggered input (A) and a negative-transition-triggered input (B), either of which can act as an inhibit input.

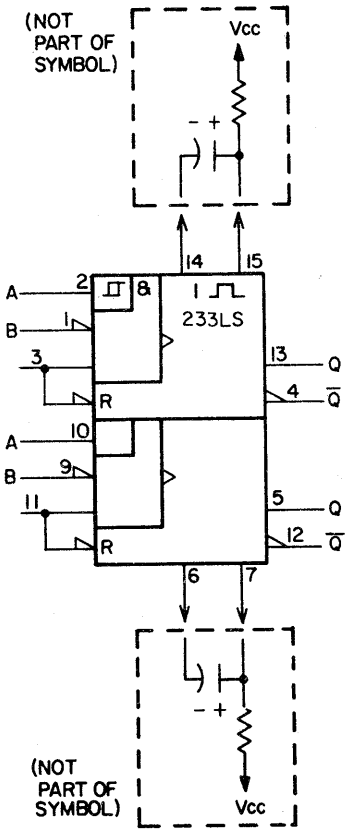
Triggering occurs at a particular voltage level and is not related to the transition time of the input pulse. Once fired, the outputs are independent of further input transitions (that is, the one-shot is not retriggerable). Bringing the Reset input low terminates any high-level output pulse.

Pulses from 30 ns to as long as 70 seconds are available with the proper external RC network.

NOTES:

1. Sections may appear separately.
2. Vendor identification: 74LS221
3. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUTS	
RESET	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	X	H	L	H
X	L	X	L	H
H	↑	L	⎍	⎎
H	H	↓	⎍	⎎

L = Low

H = High

↑ = L-to-H transition (input)

↓ = H-to-L transition (input)

⎍ = one high-level pulse (output)

⎎ = one low-level pulse (output)

X = don't care

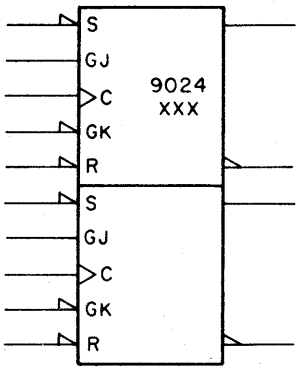
TRUTH TABLE

233
Rev J
Sheet 1 of 1

DESCRIPTION:

TTL element 240 consists of two positive-triggered $J\overline{K}$ flip-flops in one package, each featuring asynchronous set and reset (clear) inputs.

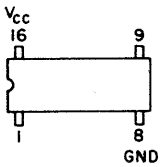
The high-active J and low-active K input configuration allows for operation as a D flip-flop by merely tying the J and K inputs together. (See Truth Tables).



LOGIC SYMBOL

NOTES:

1. Vendor identification: 9024
2. Package pin configuration:



TRUTH TABLES

Inputs		Output
Tn		Tn+1
GJ	GK	Q
L	H	Qn
L	L	L
H	H	H
H	L	$\overline{Qn}$

Tn = BIT TIME BEFORE CLOCK PULSE

Tn+1 = BIT TIME AFTER CLOCK PULSE

SYNCHRONOUS ENTRY, J-K MODE

Input	Output
Tn	Tn+1
D	Q
L	L
H	H

Tn = BIT TIME BEFORE CLOCK PULSE

Tn+1 = BIT TIME AFTER CLOCK PULSE

SYNCHRONOUS ENTRY, D MODE

Inputs		Outputs	
S	R	Q	$\overline{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No change	

ASYNCHRONOUS ENTRY, SET/RESET INPUTS

240
Rev. J
Sheet 1 of 1

DESCRIPTION

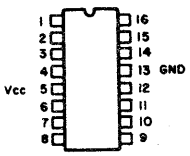
The 242H package consists of two edge-trigered J-K flip-flops with asynchronous set (S) and clear (R) inputs. Data from the J or K inputs is loaded into the FF when the clock is high, and is available at the outputs when the clock goes low.

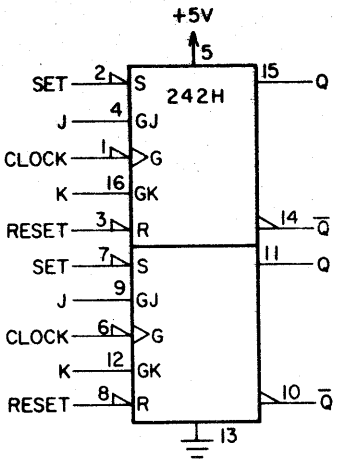
Data at J and K may change while the clock is high, but must be stable for a period of 13 nsec prior to the clock going low.

Data at the S and R inputs will override any clocked data inputs, providing that the S or R data is stable for 2 minimum of 16 nsec.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74H106
3. Package pin configuration:





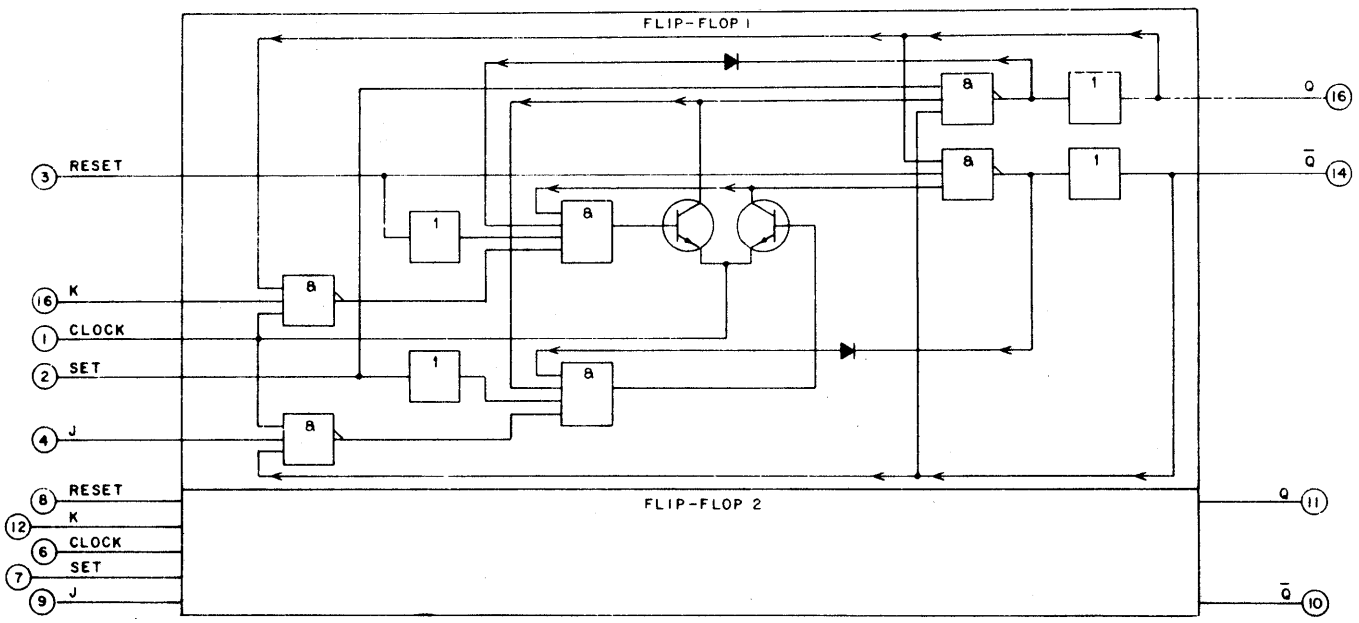
LOGIC SYMBOL

INPUTS		OUTPUT
Tn		Tn + 1
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Qn}$

Tn = BIT TIME BEFORE CLOCK PULSE
Tn + 1 = BIT TIME AFTER CLOCK PULSE

TRUTH TABLE

242H
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

242H
Rev J
Sheet 2 of 2

DESCRIPTION

The 243 package consists of two Schottky-type, edge-triggered flip-flops with asynchronous set (S) and clear (R) inputs. Data from the J and K inputs is loaded into the FF while the clock is high, and is available at the outputs when the clock goes low.

Data at J and K may change while the clock is high, but must be stable during the input set-up time, which is just prior to the clock going low. Typical set-up times are 10 nsec for the 243LS, and 3 nsec for the 243S.

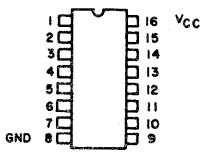
Data at the S and R inputs will override any clocked data (J-K) inputs.

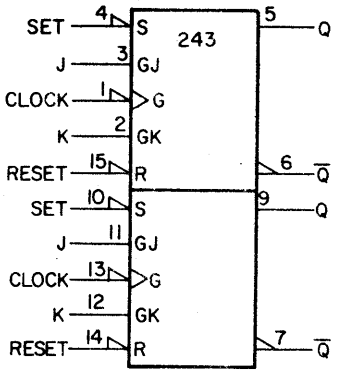
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:
3.

Element	Vendor Number
243LS	74LS112
243S	74S112

3. Package pin configuration:

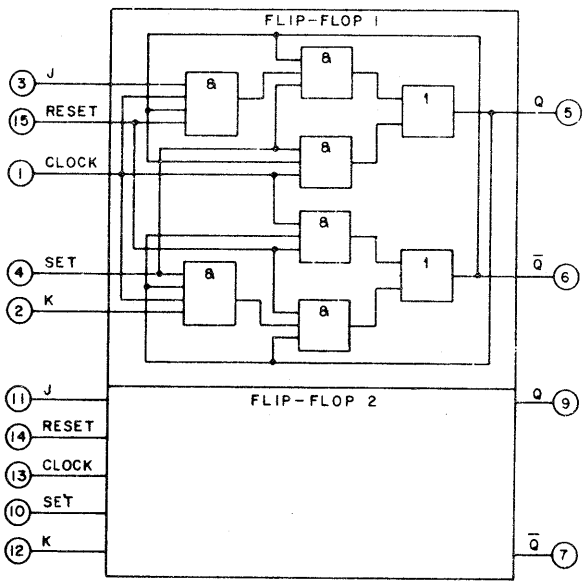




LOGIC SYMBOL

INPUTS		OUTPUT
T_n		T_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

TRUTH TABLE

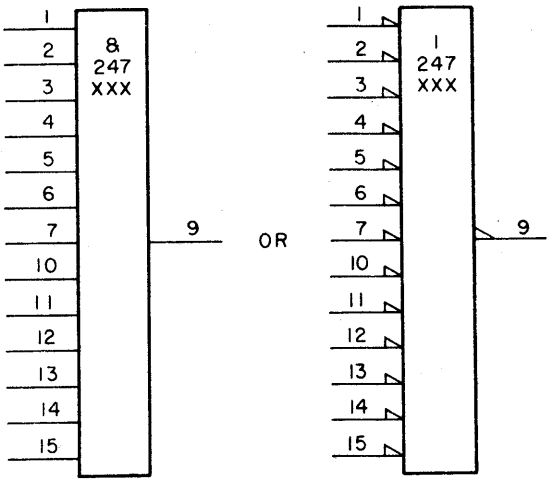


FUNCTIONAL DIAGRAM
(EITHER SECTION)

243
Rev J
Sheet 1 of 1

DESCRIPTION:

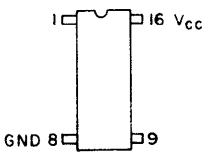
TTL element 247 is a 13-input positive AND gate. On logic diagrams, the 13 input pins are usually arranged to minimize crossed-line connections to previous ICs; the input-pin arrangement, then, may differ from that shown in the logic Symbol at the right.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 74LS133
2. Package pin configuration:

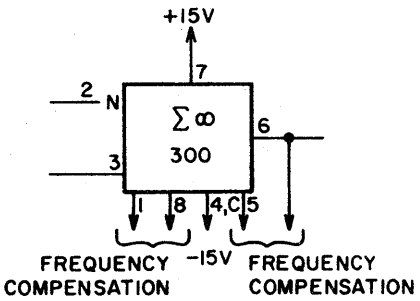


247
Rev. J
Sheet 1 of 1

DESCRIPTION

Element 300 is a high-gain operational amplifier mounted on a single chip.

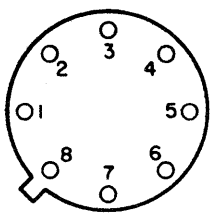
Pin	Function
1	Input Frequency Comp.
2	Inverting Input
3	Non-inverting Input
4	-V (Connected to Case)
5	Output Frequency Comp.
6	Output
7	+V
8	Input Frequency Comp.



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 709C



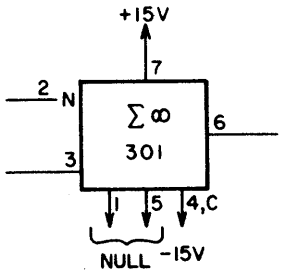
PACKAGE PIN CONFIGURATION
(Bottom View)

300
Rev M
Sheet 1 of 1

DESCRIPTION

Element 301 is a frequency compensated, high gain, operational amplifier.

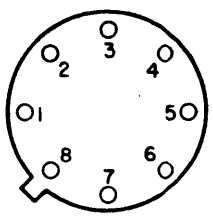
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 741C

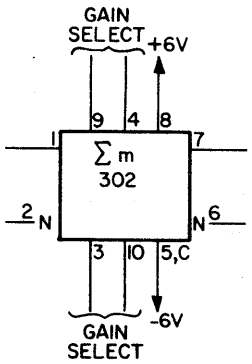


PACKAGE PIN CONFIGURATION
(Bottom View)

301
Rev M
Sheet 1 of 1

DESCRIPTION

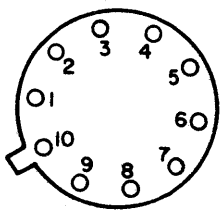
Element 302 is a high performance, wide-band amplifier with differential inputs and outputs. Fixed gains of 100 and 400 are obtained by jumpering gain select pins 3 and 10, or 4 and 9, respectively. A gain of 10 is realized if the four gain select pins are left open. Other gains within this 10-400 range may be obtained by using an external resistor. Emitter-Follower outputs provide low output impedance for driving capacitive loads.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 733C
2. **Package pin configuration: (pin 5 connects to case)**



(Bottom View)

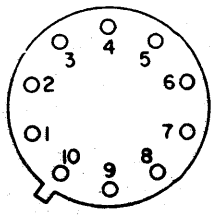
302
Rev M
Sheet 1 of 1

DESCRIPTION

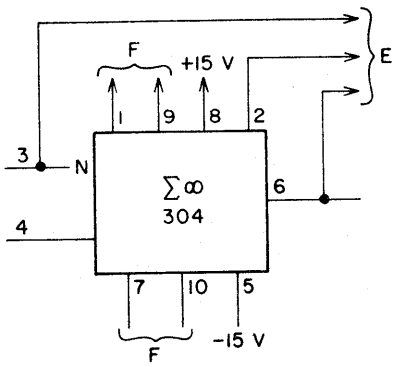
Element 304 is a high-speed, high-gain operational amplifier for use where fast signal acquisition or wide band width is required. The 304 features fast setting time, high slew rate (100 V/μs), low offsets and high output swing for large signal applications.

NOTES:

1. Vendor identification: μA715C
2. Package pin configuration:



(Bottom View)



E = EXTERNAL COMPONENTS
F = FREQ COMPENSATION

LOGIC SYMBOL

304
Rev M
Sheet 1 of 1

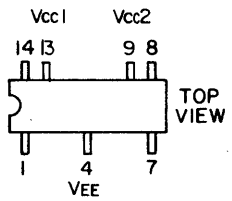
DESCRIPTION

Element 306 is a pair of frequency compensated, high gain, operational amplifier.

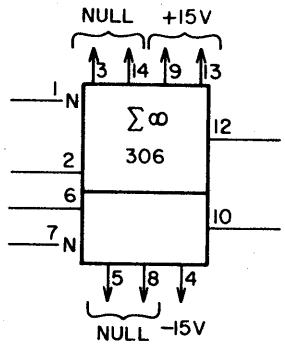
Pin	Function
1	Inverting Input A
2	Non-inverting Input A
3	Offset Null A
4	-V
5	Offset Null B
6	Non-inverting Input B
7	Inverting Input B
8	Offset Null B
9	+V (B)
10	Output B
11	No Connections
12	Output A
13	+V (A)
14	Offset Null A

NOTE:

1. Vendor Identification: 747C



PACKAGE PIN CONFIGURATION



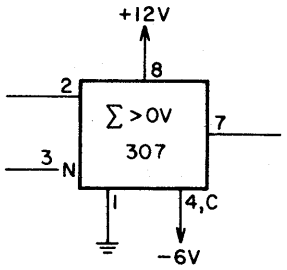
LOGIC SYMBOL

306
Rev. J
Sheet 1 of 1

DESCRIPTION

Element 307 is a differential voltage comparator.

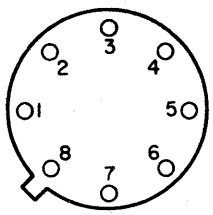
Pin	Function
1	GND
2	Non-inverting Input
3	Inverting Input
4	-V
5	No Connection
6	No Connection
7	Output
8	+V



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 710



PACKAGE PIN CONFIGURATION

(Bottom View)

307
Rev M
Sheet 1 of 1

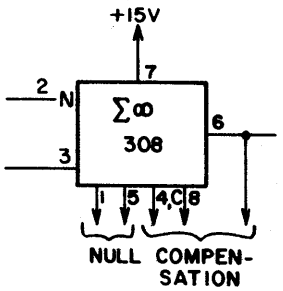
DESCRIPTION

Element 308 is a hi-slew-rate operational amplifier.

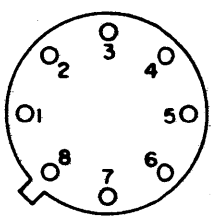
Pin	Function
1	Offset Null
2	Inverting Input
3	Non Inverting Input
4	V-
5	Offset Null
6	Output
7	V+
8	Frequency Compensation

NOTES:

1. Vendor identification: 531T



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

(Bottom View)

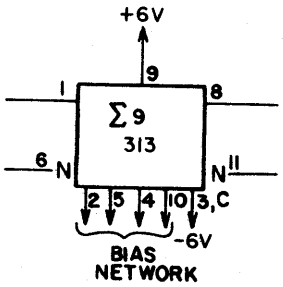
308
Rev M
Sheet 1 of 1

DESCRIPTION

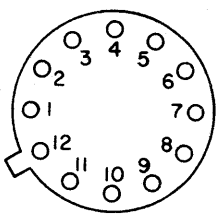
Element 309 is a wide-band differential amplifier with a nominal voltage gain of 9.

NOTES:

1. Vendor identification: 3001



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

(Bottom View)

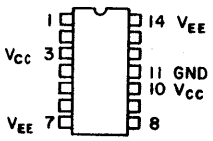
309
Rev M
Sheet 1 of 1

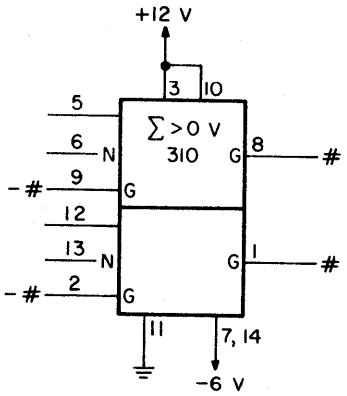
DESCRIPTION

Element 310 is a dual differential-voltage comparator. Maximum common-mode input voltage range is ±7 V. Maximum differential input voltage range is ±5 V. A minimum differential input voltage of 5.0 mV is required to switch the output.

NOTES

1. To show symbol sections separately, duplicate the V_{CC} and V_{EE} pins (2 each) and Ground symbol for each section.
2. Vendor identification: MC1414
3. Package pin configuration:





LOGIC SYMBOL

DIFFERENTIAL INPUT	STROBE (G)	OUTPUT
$V_{ID} \geq 5.0$ mV	L	L
	H	H
-5.0 mV $< V_{ID} < 5.0$ mV	L	L
	H	?
$V_{ID} \leq -5.0$ mV	L	L
	H	L

? = INDETERMINATE OUTPUT

TRUTH TABLE

310
Rev J
Sheet 1 of 1

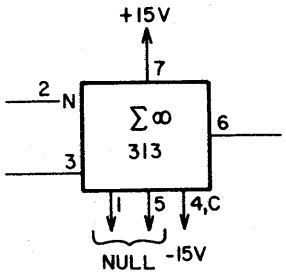
DESCRIPTION

Element 313 is a frequency compensated, high gain, operational applifier.

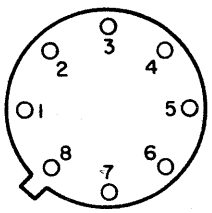
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)

NOTE:

1. Vendor Identification: 741



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

(Bottom View)

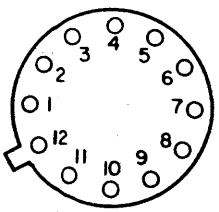
313
Rev M
Sheet 1 of 1

DESCRIPTION

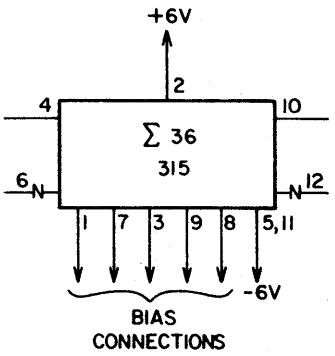
Element 315 is a wide-band amplifier for frequencies up to 200 MHz.

NOTES:

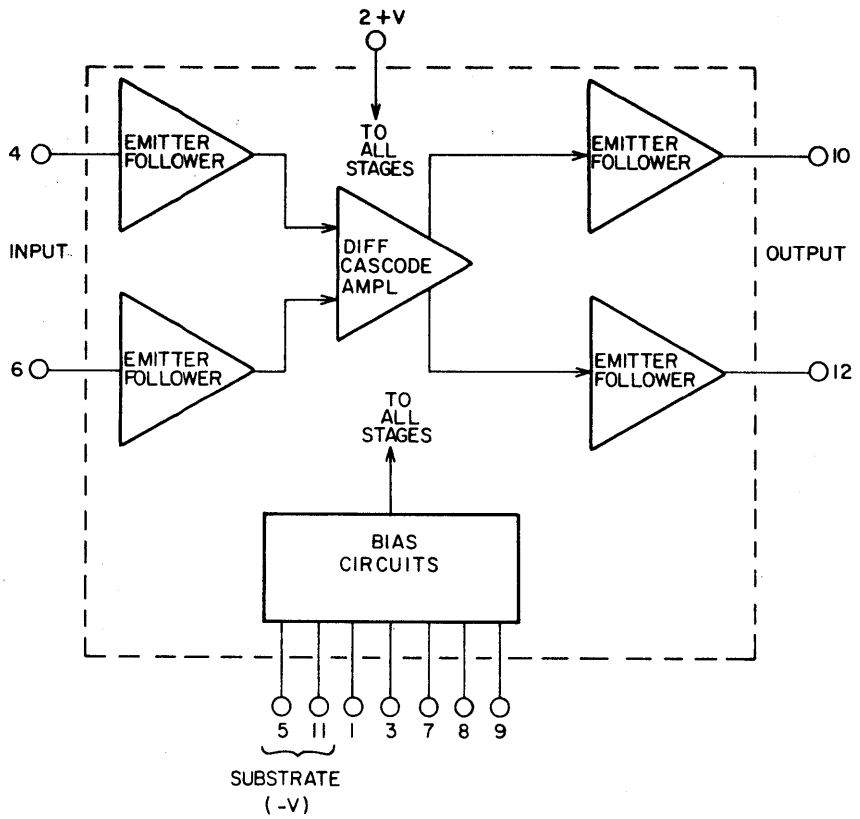
1. Vendor identification: CA3040
2. Package pin configuration:



(Bottom View)



LOGIC SYMBOL



FUNCTIONAL DIAGRAM

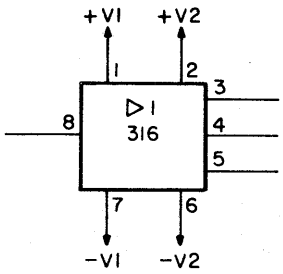
315
Rev M
Sheet 1 of 1

DESCRIPTION

Element 316 is a wide band, unity-gain current amplifier capable of providing peak currents of ±200 mA into a 50-ohm load. The symmetrical class-B output provides a constant low output impedance for both the positive and negative slopes of the output pulses.

Separate connections are provided for + (Vcc) and - (V_{EE}) voltages to both the input and output stages (see electrical schematic diagram). This increases the versatility of operation by allowing a decreased voltage to be applied to the output stage (Q3, Q4), thereby minimizing the power dissipation.

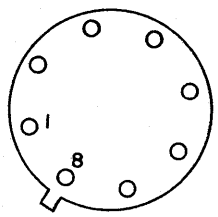
Typical applications: differential input/output op amp, booster amplifier, level shifter, pulse-transformer driver, and transmission-line driver.



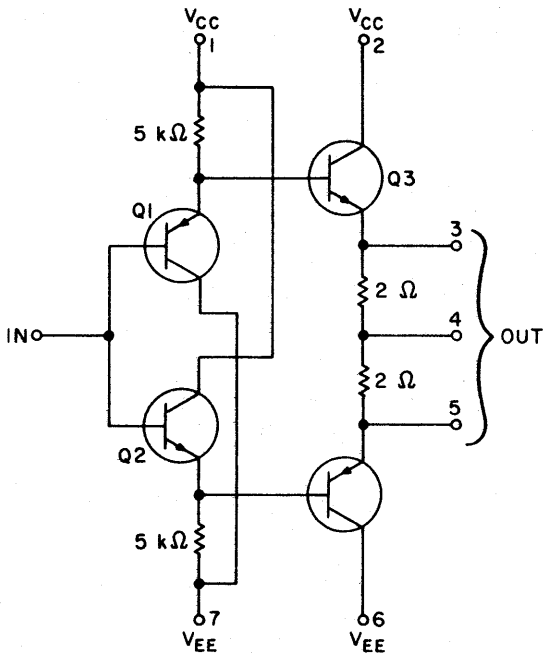
LOGIC SYMBOL

NOTES

1. Vendor identification: LH0002CH
2. Package pin configuration:



(Bottom View)



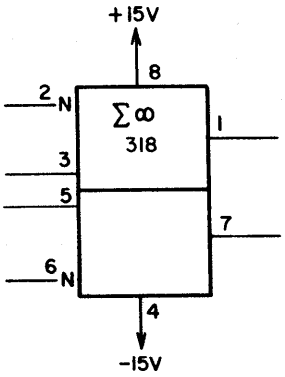
ELECTRICAL SCHEMATIC DIAGRAM

316
Rev M
Sheet 1 of 1

DESCRIPTION

Element 318 is a dual, high-performance operational amplifier.

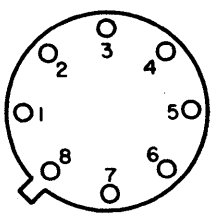
Pin	Function
1	Output A
2	Inverting Input A
3	Non Inverting Input A
4	V-
5	Non Inverting Input B
6	Inverting Input B
7	Output B
8	V+



LOGIC SYMBOL

NOTES:

1. Vendor identification: 72558



PACKAGE PIN CONFIGURATION

(Bottom View)

318
Rev M
Sheet 1 of 1

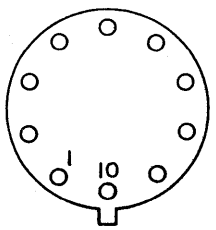
DESCRIPTION

The 320 circuit is a negative voltage regulator that can be programmed by an external resistor to provide any voltage from -40 V to 0 V while operating from a single unregulated supply. Regulation is 1 mV, no load to full load. The full-load current of 25 mA can be increased by adding external transistors.

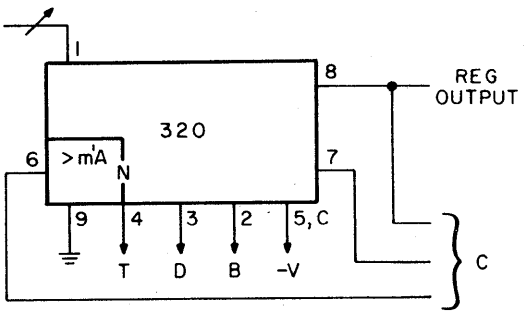
See page 320-2 for typical applications.

NOTES:

1. Vendor identification: LM304
2. Package pin configuration: (pin 10 is unused)



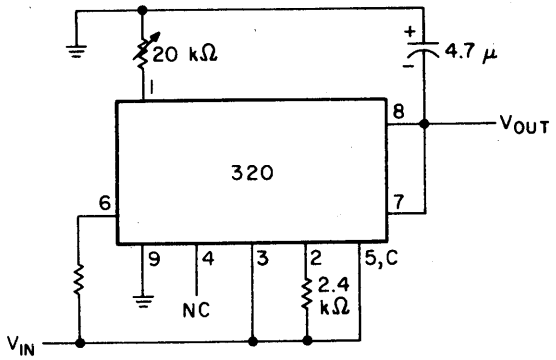
(Bottom View)



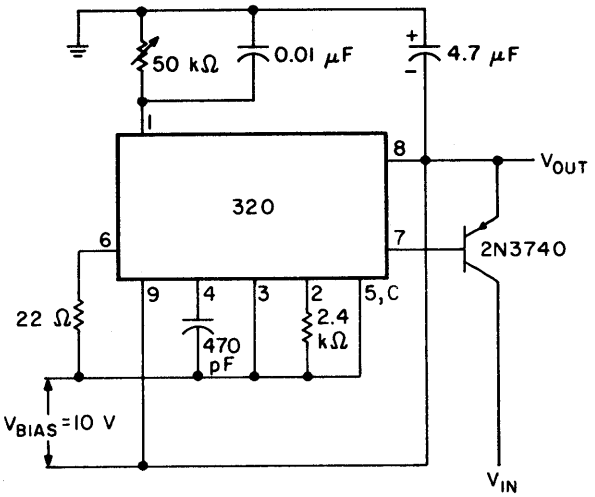
T = TERMINATION
D = DIVIDER COMPONENTS
B = BIAS CIRCUIT (REFERENCE VOLTAGE)
-V = UNREGULATED INPUT
C = CURRENT MONITOR
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY D
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY C

LOGIC SYMBOL

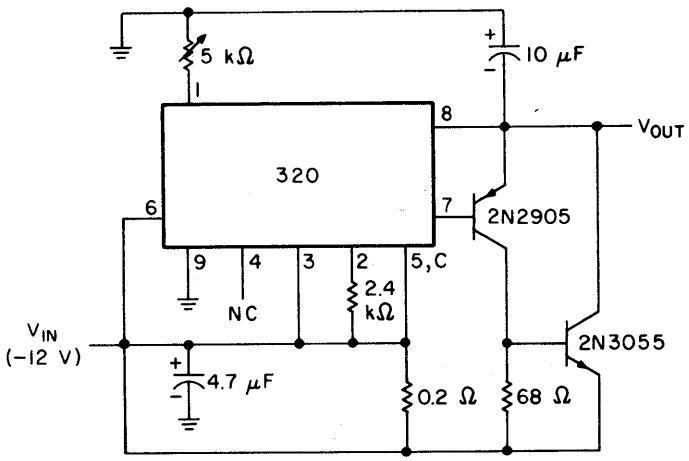
320
Rev M
Sheet 1 of 2



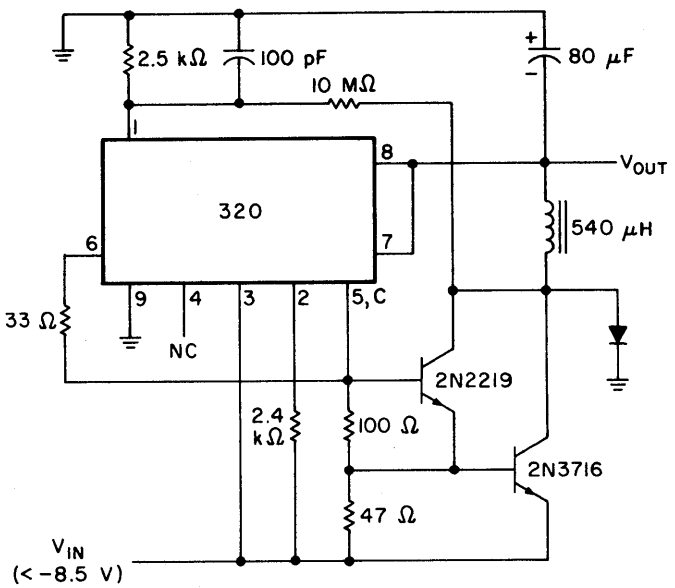
BASIC REGULATOR



SEPARATE BIAS SUPPLY



HIGH-CURRENT REGULATOR



SWITCHING REGULATOR

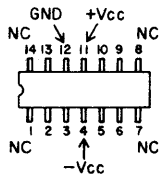
320
Rev J
Sheet 2 of 2

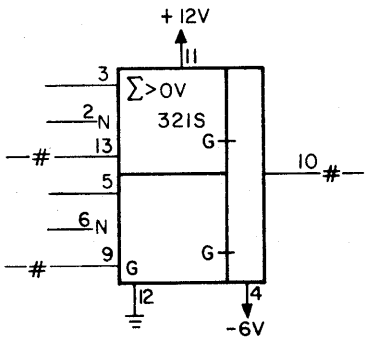
DESCRIPTION

The 321S is a dual differential comparator. Output (pin 10) is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high. A low level to pin 9 or 13 will inhibit operation of that section.

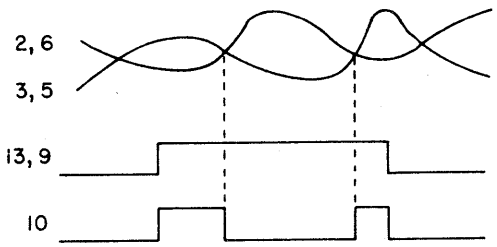
NOTES:

1. Vendor identification: TSC 5711
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION SEQUENCE

321
Rev J
Sheet 1 of 1

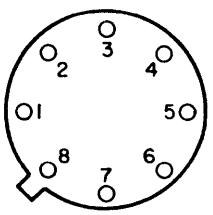
DESCRIPTION

Element 322 is a frequency compensated, high speed operational amplifier.

Pin	Function
1	Offset Null/Compensation 1
2	Inverting Input
3 3	Non-inverting Input
4	-V
5	Offset Null/Compensation 3
6	Output
7	+V
8	Compensation 2

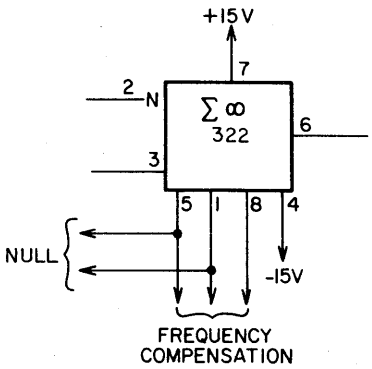
NOTE:

1. Vendor Identification: LM318H



PACKAGE PIN CONFIGURATION

(Bottom View)



LOGIC SYMBOL

322
Rev M
Sheet 1 of 1

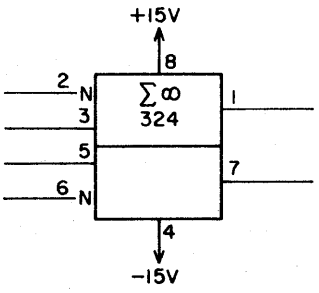
DESCRIPTION

The 324 circuit is a dual, internally compensated, high-performance operational amplifier.

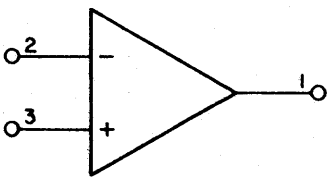
Pin	Function
1	Output A
2	Inverting Input A
3	Non-inverting Input A
4	V_{EE}
5	Non-inverting Input B
6	Inverting Input B
7	Output B
8	V_{CC}

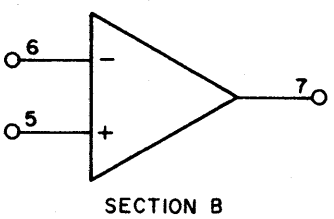
NOTE:

Vendor Identification: MC1458/N5558

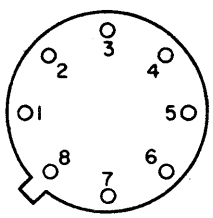


LOGIC SYMBOL





FUNCTION DIAGRAM



PACKAGE PIN CONFIGURATION

(Bottom View)

324
Rev M
Sheet 1 of 1

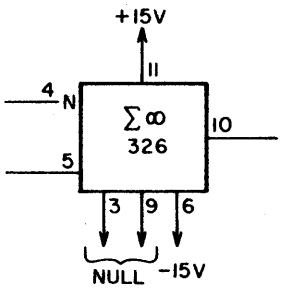
DESCRIPTION

Element 326 is a high-gain operational amplifier.

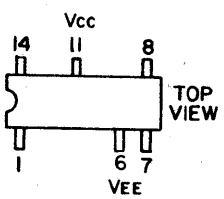
Pin	Function
1	No Contact
2	No Contact
3	Offset Null
4	Inverting Input
5	Non-Inverting Input
6	V-
7	No Contact
8	No Contact
9	Offset Null
10	Output
11	V+
12	No Contact
13	No Contact
14	No Contact

NOTE:

1. Vendor Identification: 741C



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

326
Rev. J
Sheet 1 of 1

DESCRIPTION

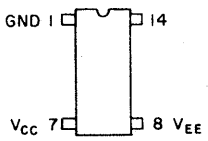
Element 327 is a dual-polarity voltage regulator for providing balanced positive and negative output voltages at currents up to 100 mA. Internally, the device is set for ±15 V outputs, but voltage and balance pins permit simultaneous adjustments from 8 to 20 volts. Input voltages up to ±30 V can be used, and current monitor connections provide for adjustable current limiting.

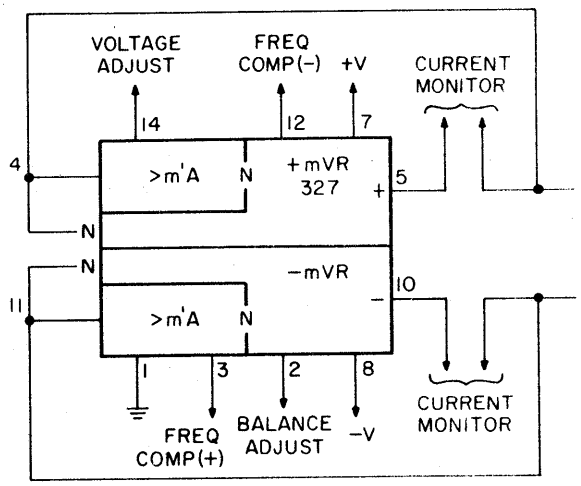
For typical applications, see page 327-2.

NOTES

1. Vendor identification: MC1468L

2. Package pin configuration

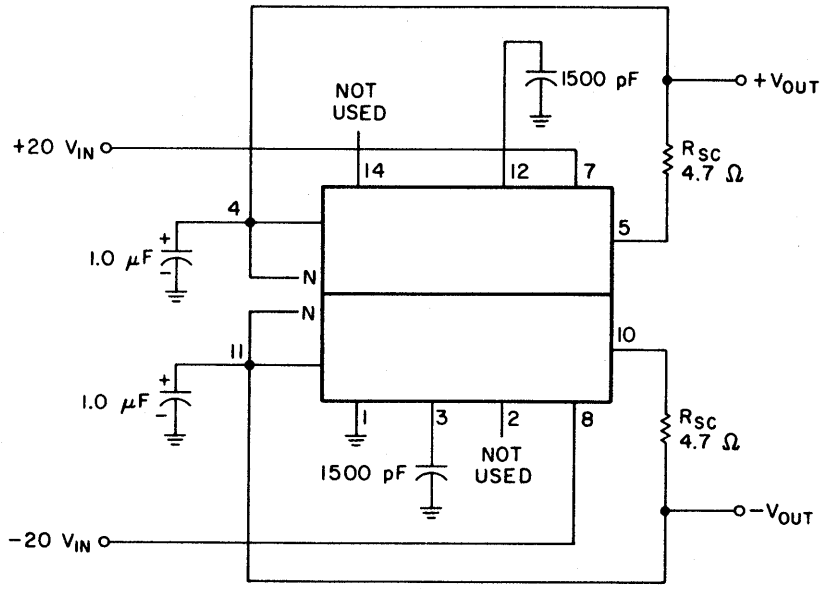




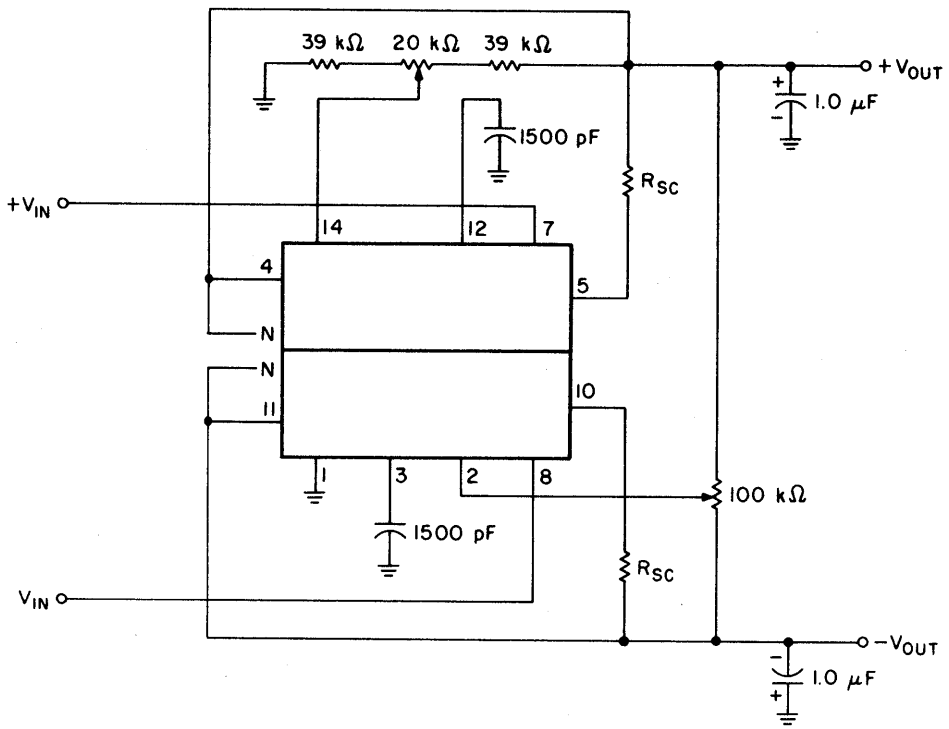
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY VOLTAGE AND BALANCE ADJUST COMPONENTS.
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY CURRENT MONITOR COMPONENTS.

LOGIC SYMBOL

327
Rev J
Sheet 1 of 2



BASIC 50 mA REGULATOR



VOLTAGE ADJUST/BALANCE CIRCUIT

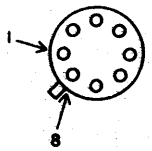
327
Rev J
Sheet 2 of 2

DESCRIPTION

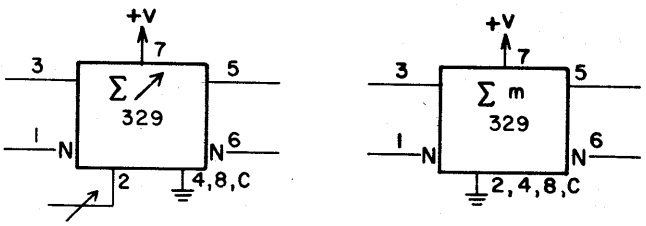
The 329 circuit is a wide-band RF/IF/Audio amplifier with external AGC control.

NOTES:

1. Vendor identification: 1590
2. Package pin configuration. (TO-99 metal case)



(Bottom View)



LOGIC SYMBOL

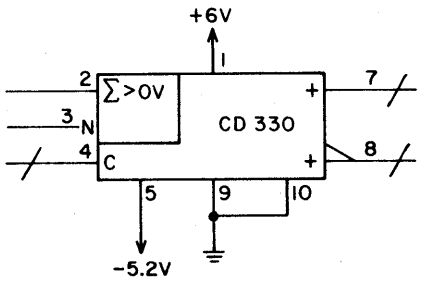
DESCRIPTION

The 330 circuit is a differential voltage comparator. The circuit has differential analog inputs and complementary logic outputs compatible with ECL. A latch function allows the comparator to be used in a sample-hold mode. If the latch enable input is high, the comparator functions normally. When the latch enable goes low, the comparator outputs are locked in their existing logical states.

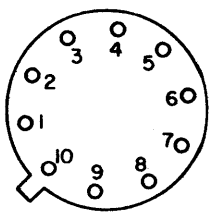
Pin	Function
1	+V
2	Non-inverting Input
3	Inverting Input
4	Latch Enable
5	-V
6	No Connection
7	Q Output
8	$\overline{Q}$ Output
9	GND
10	GND

NOTE:

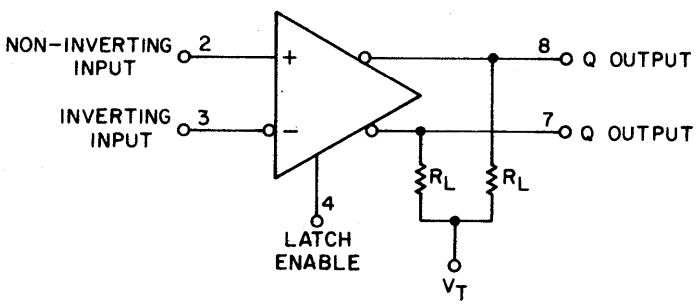
1. Vendor identification: AM685



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION
(Bottom View)



FUNCTION DIAGRAM

330
Rev M
Sheet 1 of 1

DESCRIPTION

Element 331A is a dual-polarity tracking voltage regulator that provides balanced or unbalanced positive and negative output voltages at currents up to 200 mA. A single external resistor adjustment changes both outputs between the limits of ±50 mV and ±42 V. The 331A comes in a 9-pin (type H) "top hat" package that can dissipate up to 3 W. Both output voltages drop to zero if the junction temperature rises above 175°C.

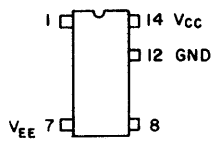
Element 331 is similar to the 331A, except that it comes in a 14-pin DIP that can dissipate up to 900 mW.

NOTES

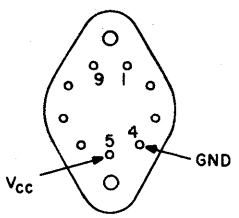
1. Vendor identification:

Element	Vendor Number
331	RC4194D
331A	RC4194TK

2. Package pin configuration:



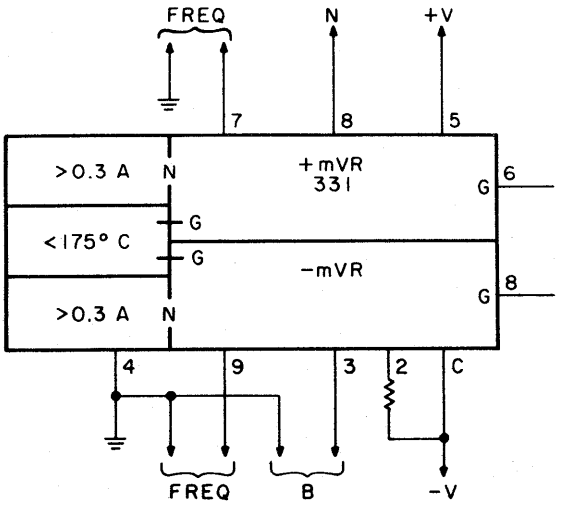
331
(Top View)



CASE CONNECTED TO V_{EE}

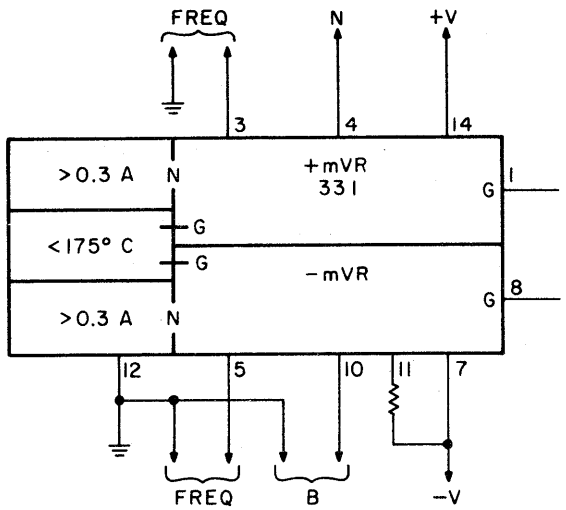
331A
(Bottom View)

331A



OR

331



REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY BIAS (B) AND BALANCE (N) COMPONENTS

LOGIC SYMBOL

331
Rev M
Sheet 1 of 1

DESCRIPTION

The 332 and 353 circuits are positive voltage regulators. Output voltage is adjustable from 4.5 to 40 volts. The full-load output current of the 332 is 45 mA, that of the 353 is 25 mA. Either of these may be increased in excess of 10A by using an external pass transistor.

The 332 comes in an 8-pin metal can, the 353 in an 8-pin DIP.

Pin	Function
1	Current Limit
2	Booster Output
3	Unregulated Input
4	Ground
5	Reference Bypass
6	Feedback
7	Compensation
8	Regulated Output

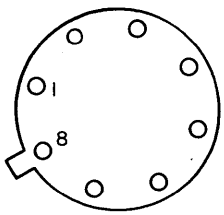
NOTES

1. Vendor identification:

Element	Vendor Number
332	LM305A
353	LM376

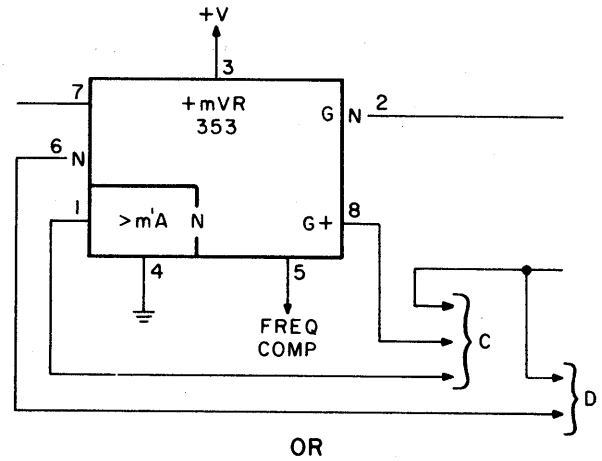
2. Package pin configurations:

353
(Top View)

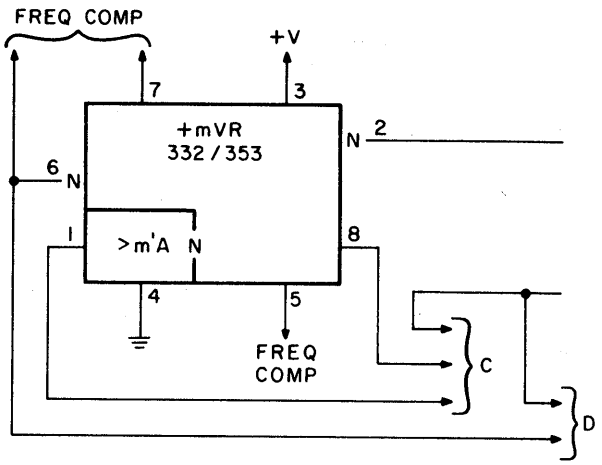


PIN 4 CONNECTED TO CASE

332
(Bottom View)



OR



REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY D DIVIDER.
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY C.

LOGIC SYMBOL

DESCRIPTION

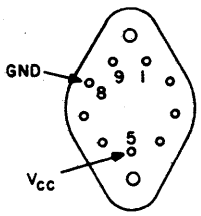
Element 333 is a dual-polarity tracking voltage regulator that provides balanced positive and negative 15 V outputs at currents up to 100 mA. The type-H packaging permits heat dissipation of up to 2.4 W. Both output voltages drop to zero if the junction temperature rises above 175°C.

The 333 circuit may also be used as a single-output regulator with up to +50 V output, where:

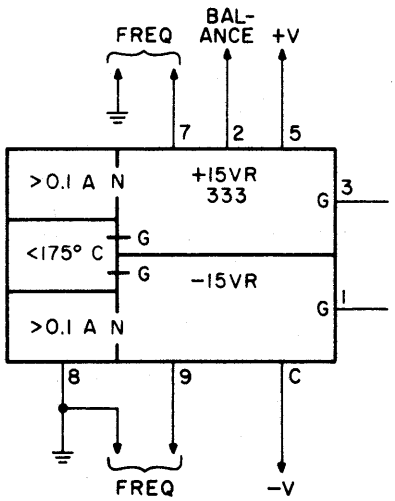
(V out +3 V) <V in <60 V

NOTES

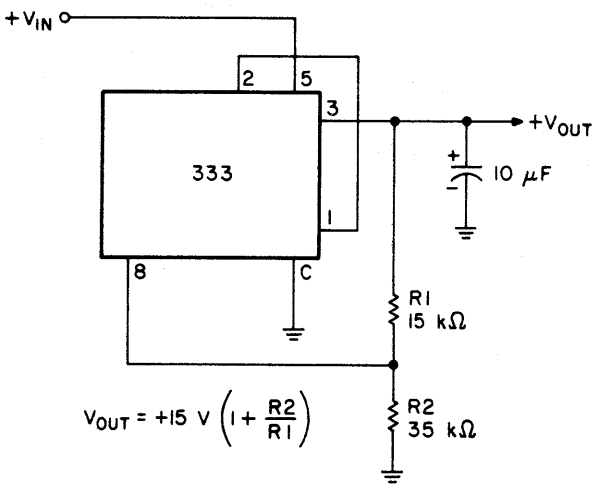
1. Vendor identification: RC4195TK
2. Package pin configuration:



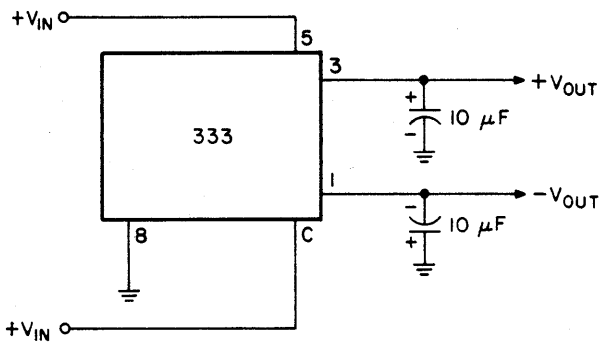
V_{EE} CONNECTED TO CASE
(Bottom View)



LOGIC SYMBOL



SINGLE +50 V OUTPUT
($I_O \leq 100$ mA)



BALANCED OUTPUT
($\pm I_O \leq 100$ mA)

TYPICAL APPLICATIONS

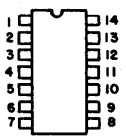
DESCRIPTION

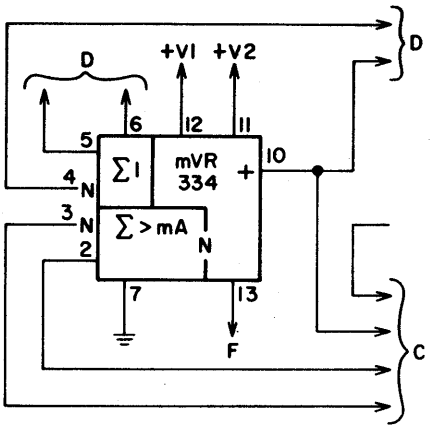
The 334 circuit is a monolithic voltage regulator. Internal circuitry consists of a voltage reference, a differential error amplifier, and a series pass transistor. Typical applications for this device are shown in figures A and B on page 334-2.

Pin	Function
1	No Connection
2	Current Limit
3	Current Sense
4	Inverting Input
5	Non-inverting Input
6	Voltage Reference
7	Ground
8	No Connection
9	Not Used (Connects to pin 10 thru a 6. V Zener diode)
10	+V out
11	+V2 (V_C)
12	+V1 (V_{CC})
13	Compensation
14	No Connection

NOTES:

1. Vendor identification: MC1723C, LM723C
2. Package pin configuration:





C=CURRENT MONITOR COMPONENTS
D=DIVIDER COMPONENTS
F=FREQUENCY COMPENSATION COMPONENTS

	Nom.	Min.	Max.	Units
Output Current			150	mA
Input Voltage Range		9.5	40.0	V
Output Voltage Range		2.0	37.0	V
Load Regulation*		0.03	0.2	%VO
Reference Voltage	7.15	6.8	7.5	V
In/Out Voltage Differential		3.0	38.0	V

* IL = 1 mA to 50 mA

LOGIC SYMBOL

334
Rev J
Sheet 1 of 2

Typical Application:

Figure A provides an output current up to 150 mA. For higher currents, figure B is substituted, using an external transistor to source the high current. Here, the series output resistor, RSC, senses the output current. Output voltage is applied to one input (pin 4) of the error amplifier. Resistors R1 and R2 drop the internal reference voltage to the desired output reference voltage, which is applied to the other error amplifier input (pin 5).

In figure B, the output voltage is compared with the output reference voltage. Any difference voltage is amplified, and the resulting regulator output drives the series pass transistor in direct proportion to the output load. If the current limit is reached, the output current remains constant, and the output voltage decreases for a greater load. Capacitor 'C' provides for frequency compensation.

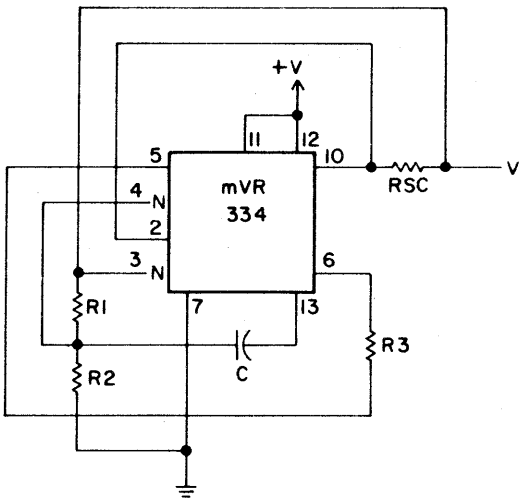


FIGURE A

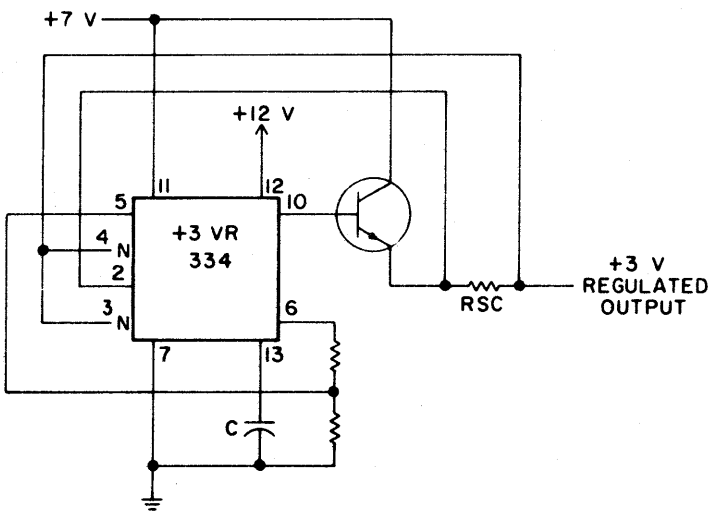


FIGURE B

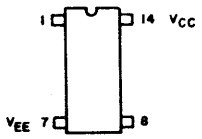
334
Rev J
Sheet 2 of 2

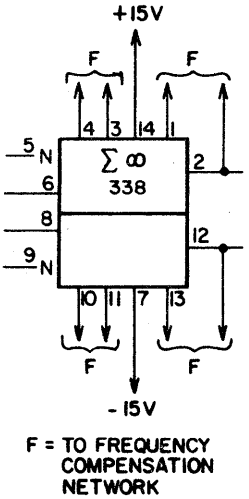
DESCRIPTION

Element 338 is a dual high-gain operational amplifier.

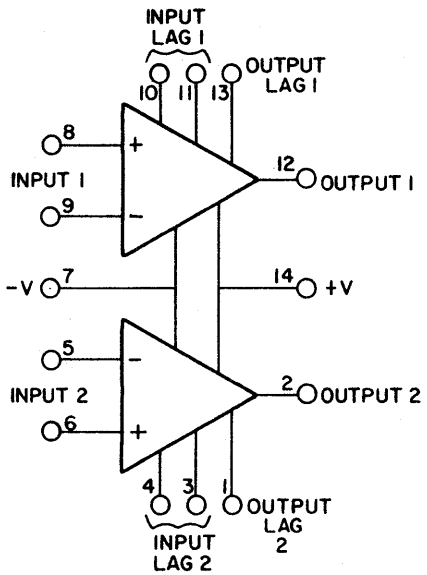
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: MC1437
3. Package pin configuration:



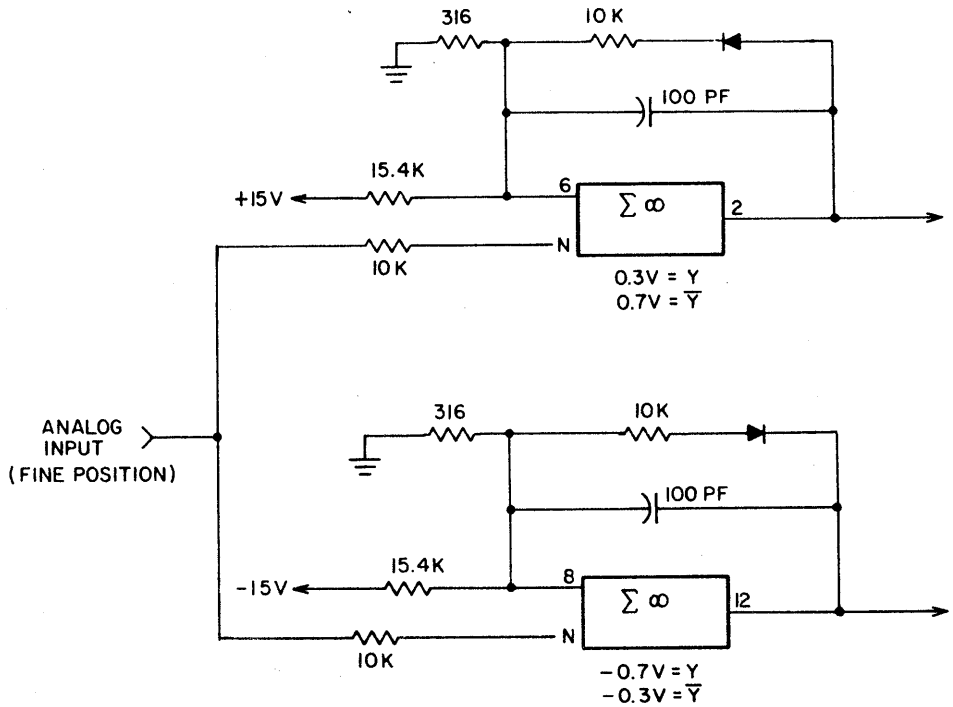


LOGIC SYMBOL



EQUIVALENT CIRCUIT

338
Rev K
Sheet 1 of 2



TYPICAL APPLICATION

338
Rev J
Sheet 2 of 2

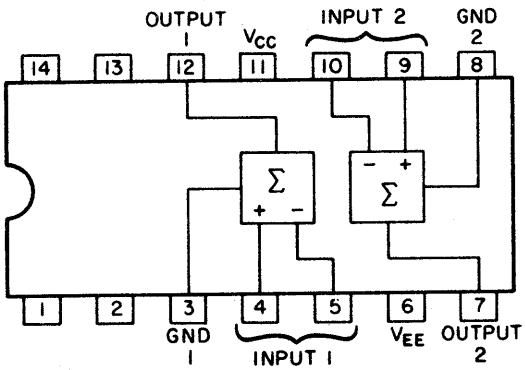
DESCRIPTION

Element 339 consists of two high-speed voltage comparators in one package. Each section provides an open-collector output capable of driving lamps or relays requiring up to 25 mA. Inputs and outputs can be isolated from system ground.

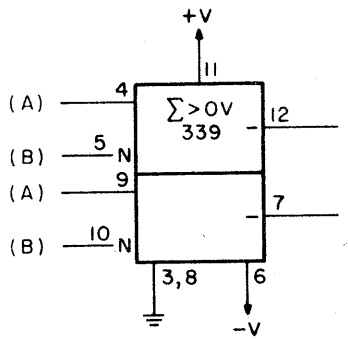
The 339 can operate from a single +5 V supply, or from ± supplies with a total potential difference of up to 36 V. Maximum differential input voltage is ±5 V.

NOTES

1. If sections appear separately, the supply-voltage pins are repeated as needed and only the applicable ground pin is shown for each section.
2. Vendor identification: LM319
3. Package pin configuration and functional diagram:



339



LOGIC SYMBOL

A more positive than B: output open.

A equal to or less positive than B: output grounded.

339
Rev J
Sheet 1 of 1

DESCRIPTION

Element 340 is a high-performance operational amplifier with high open-loop gain, high common-mode range, internal frequency compensation, and exceptional temperature stability. Internal short-circuit protection allows for nulling of the offset voltage.

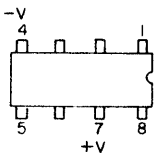
NOTES:

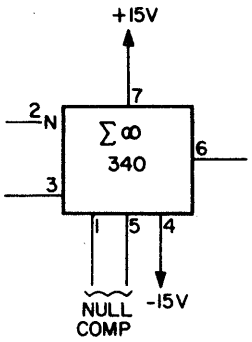
1. Vendor identification:

Element	Vendor Number
340	741C
340A	741S

2. Package pin configuration:

(pin 8 not connected)





LOGIC SYMBOL

340
Rev J
Sheet 1 of 1

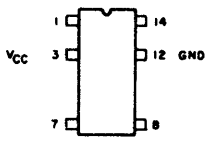
DESCRIPTION

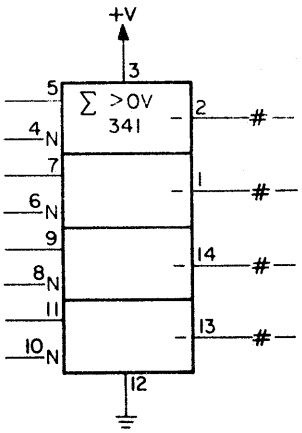
Element 341 consists of four independent precision voltage comparators, each having an offset voltage specification as low as 2 mV, maximum. The 341 interfaces directly with TTL and CMOS. Operating range is +2 V dc to +36 V dc, or ±1 V dc to ±18 V dc. Current drain (0.8 mA) is independent of supply voltage.

The input common-mode voltage range includes ground, even when operating from a single po power supply.

NOTES:

1. Sections may appear separately (V_{CC} and GND connections repeated).
2. Vendor identification: LM339
3. Package pin configuration:



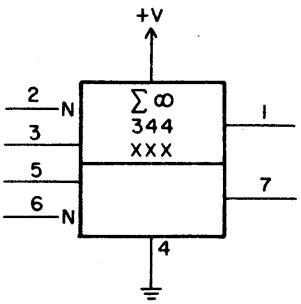


LOGIC SYMBOL

341
Rev J
Sheet 1 of 1

DESCRIPTION:

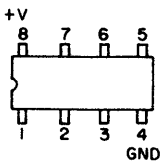
Element 344 consists of two independent, high-gain, internally frequency-compensated operational amplifiers in one 8-pin package. The 344 is designated to operate from one +5 V power supply, rather than the separate + and - supplies normally required for op amps.



LOGIC SYMBOL

NOTES:

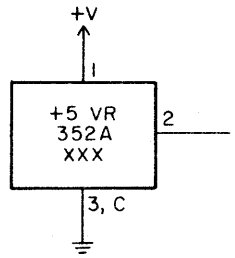
1. Vendor identification: 358N
2. Package pin configuration:



344
Rev. J
Sheet 1 of 1

DESCRIPTION:

Elements 352 and 352A are 5-volt regulators with internal current limiting and thermal shutdown. The 352 comes in a TO-3 package capable of delivering output currents up to 1A. The 352A uses a TO-5 package, and can deliver up to 200 mA.



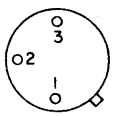
LOGIC SYMBOL

NOTES:

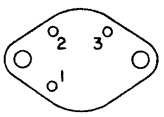
1. Vendor identification:

Element	Vendor Number
352	309K
352A	309H

2. Package pin configuration:



BOTTOM VIEW
352A



BOTTOM VIEW
352

DESCRIPTION

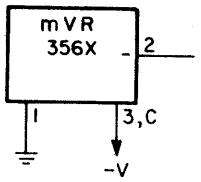
Element 356 is a negative-voltage regulator. Output currents in excess of 1A can be delivered with adequate heat sinking. Thermal overload and short circuit protection is provided internally, and "safe area" compensation at the output reduces the short-circuit as the voltage across the internal pass transistor is increased.

NOTES:

1. Vendor identification:

Element	Vendor Number
356A	MC7905C/LM320T-5
356B	MC7905.2C/LM320T-5.2
356C	MC7912C/LM320T-12
356D	MC7915C/LM320T-15

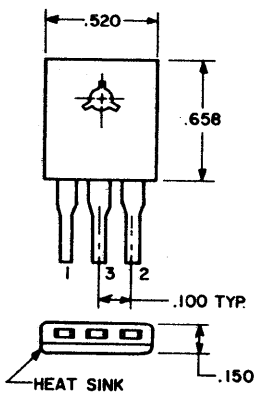
2. Package pin configuration:
   (heat sink connected to pin 3)



Replace 'm' in qualifying symbol according to the value in parentheses below for the element used:

356A (-5)
356B (-5.2)
356C (-12)
356D (-15)

LOGIC SYMBOL



TO220

356
Rev J
Sheet 1 of 1

DESCRIPTION

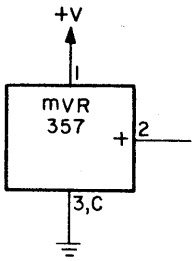
Element 357 is a positive-voltage regulator featuring internal current limiting, thermal shutdown, and safe-area compensation. Output currents in excess of 1A are possible with adequate heat sinking.

NOTES:

1. Vendor identification:

Element	Vendor Number
357A	7805C/LM340T+5
357B	7806C/LM340T+6
357C	7808C/LM340T+8
357D	7812C/LM340T+12
357E	7815C/LM340T+15
357F	7818C/LM340T+18
357E	7824C/LM340T+24

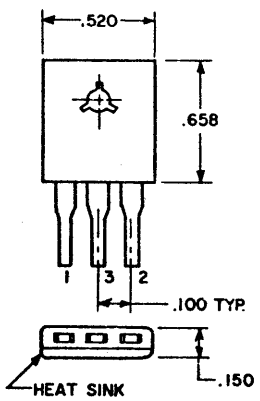
2. Package pin configuration:
   (heat sink connected to pin 3)



Replace 'm' in qualifying symbol according to the value in parentheses below for the element used:

357A (+5)
357B (+6)
357C (+8)
357D (+12)
357E (+15)
357F (+18)
357G (+24)

LOGIC SYMBOL



T0220

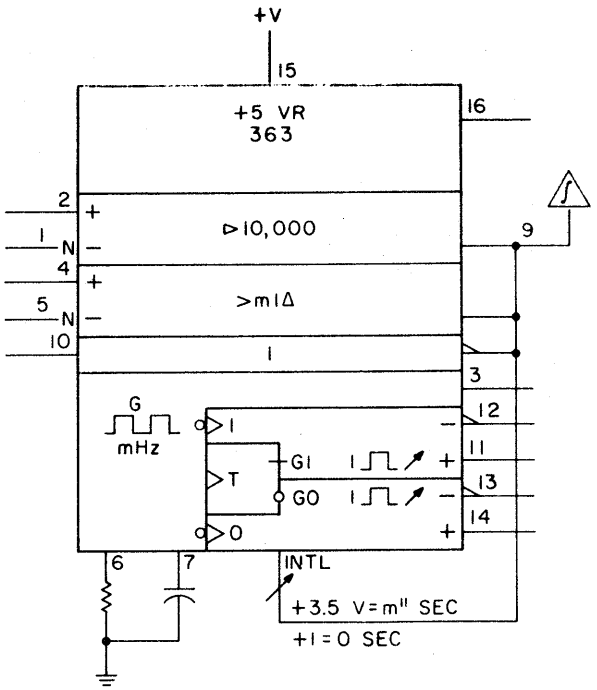
357
Rev J
Sheet 1 of 1

DESCRIPTION:

TTL element 363 is a regulating pulse-width modulator that operates with input voltages up to 40 V. Output transistors A and B (see block diagram on sheet 2) are controlled by a pulse-steering FF, which is driven by an oscillator that has a period $t = R_T C_T$, where t is in microseconds, R_T is in ohms, and C_T is in microfarads.

For single-ended operation (outputs paralleled), the duty cycle range is 0-90% and the frequency of the output is the same as that of the oscillator. For push-pull applications (a voltage doubler, for example), the duty cycle for each output has the range 0-45%, and the overall frequency of the output is one-half that of the oscillator.

Maximum current for each output is 100 mA. If the current-limiting feature is not used, pins 4 and 5 should be grounded.

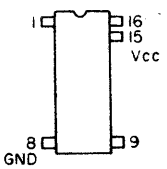


REPLACE m WITH NOMINAL FREQUENCY, m' WITH NOMINAL CURRENT LIMIT POINT, AND m" WITH NOMINAL MAXIMUM PULSE WIDTH.

LOGIC SYMBOL

NOTES:

1. Vendor identifications SG 3524
2. Package pin configuration:



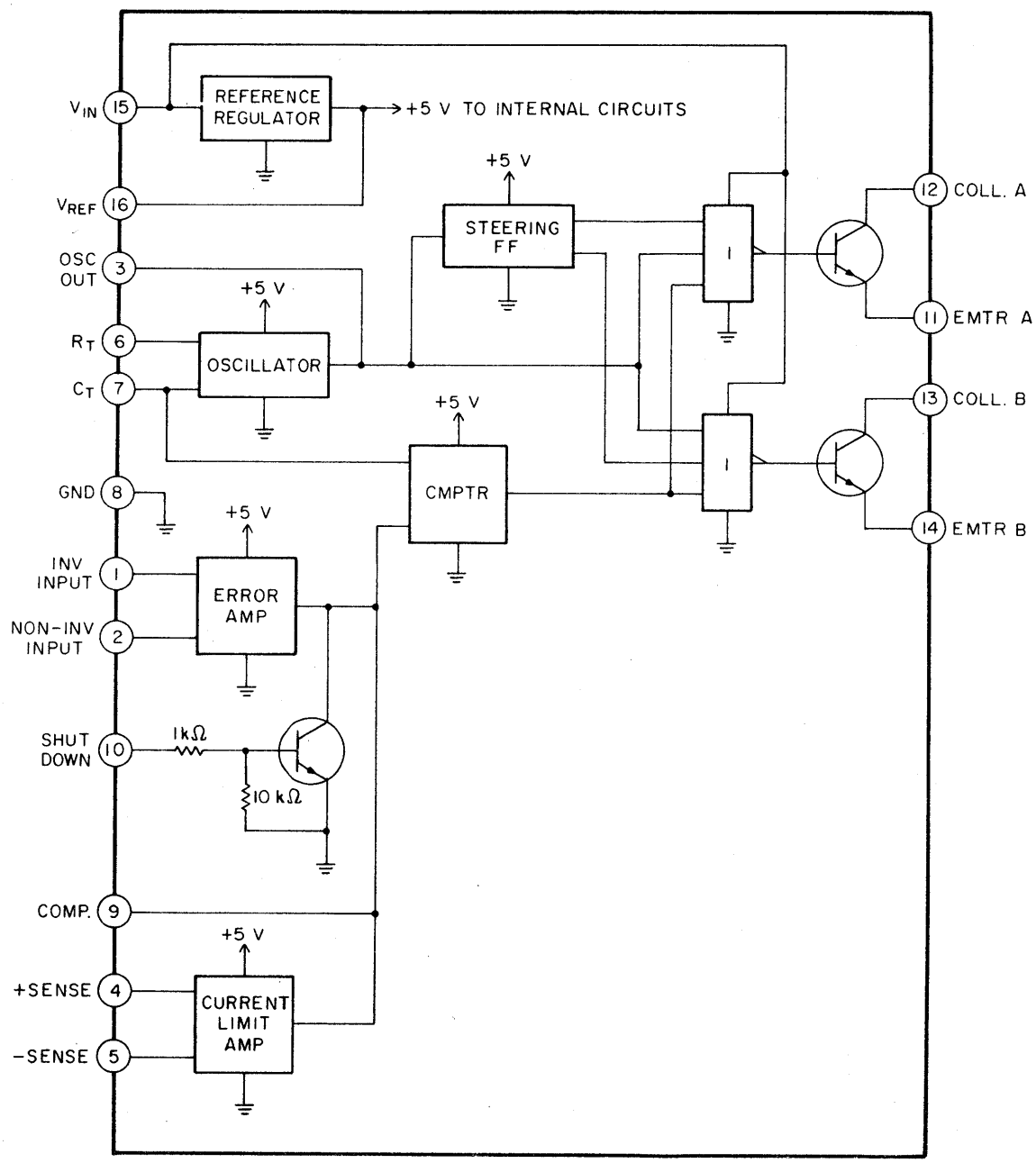


Figure 1. Functional Block Diagram, 36

363
Rev. J
Sheet 2

DESCRIPTION:

CMOS element 368 is a 3 1/2-digit A/D converter. A typical use of this chip would be to provide the BCD segment-drive input to decoders feeding a 3 1/2-digit LED or LCD digital voltmeter with two ranges:

1.999 V - 1.0 mV

199.9 mV - 0.1 mV

(The 1 in the most significant position is referred to as a half digit because it requires only two of the usual seven segments).

The 368 measures an unknown input voltage (pin 3) by comparing it, ratiometrically, against a known full-scale reference voltage; and then expressing that ratio as a BCD value. Each conversion requires 16,400 cycles of the internal clock. Two external resistors and two external capacitors are needed for operation of the chip. These are shown at the ends of the broken lines in the logic symbol, and will be discussed in the appropriate pin description that follow.

Pin 2

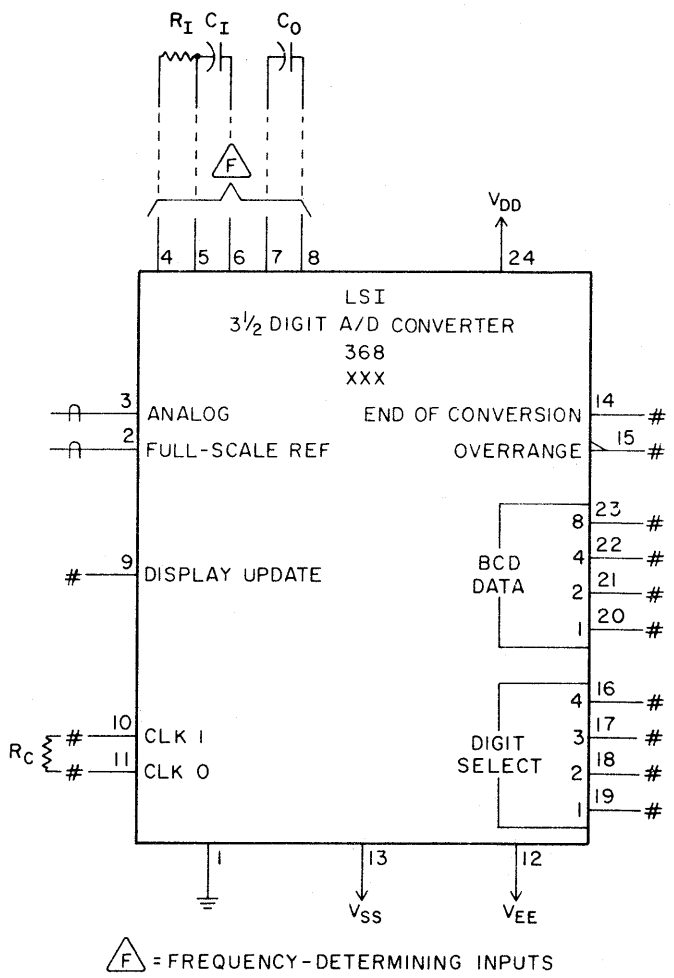
The full-scale reference voltage is applied to this pin. For a full-scale reading of 1.999 V, pin 2 = 2.0 V. For a full-scale reading of 199.9 mV, pin 2 = 200 mV. Pin 2 may also be used as a chip reset by connecting it to the most negative supply voltage, V_{EE} (pin 12).

Pins 10, 11

The time required for each conversion cycle is governed by R_C, connected between clock pins 10 and 11. For a typical conversion rate of 250 ms (66 kHz clock), R_C would be 300 kilohms. (Maximum clock frequency is 400 kHz, which represents a conversion time of about 40 ms.) For better frequency stability, these pins may be connected to an external crystal. A third method would be to use an external clock signal. This signal would connect to pin 10 and be referenced to V_{EE} (pin 12).

Pins 7,8

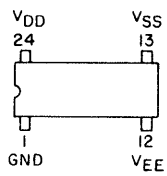
Capacitor C_O connects between these two pins and determines the Offset correction for the buffer and integrator amplifiers. Recommended value for this mylar capacitor is 0.1 µF.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 14433
2. Package configuration:



368
REV L
Sheet 1 of 3

Pins 4,5,6

C_I and R_I are part of the integrator network. The recommended value for C_I is 0.1 µF. The value of R_I depends upon the voltage range (see above). For a maximum of 1.999 V, use 470 kilohms; for the 199.9 mV range, use 27 kikohms.

Pins 9,14

For most applications, pin 9 (Display Update) is connected to pin 14 (End of Conversion) to provide a continuous readout. If pin 9 is to be controlled externally, it will become active on the positive-going edge of the signal, which should be referenced to V_{SS} (pin 13), rather than V_{EE} or ground.

Pins 16-19

These digit select pins sequentially enable the four displays, starting with the most significant 1/2 digit (pin 19), immediately following the fall of the End of Conversion pulse on pin 14. One complete display cycle (four digits plus the polarity indicator) requires 80 clock cycles. As each conversion takes 16,400 clock cycles, this means that the display cycle is repeated 200 times during each converion cycle. For a clock frequency of 66 kHz, then, the display would be repeated about every 1.20 ms. As shown in figure 1, there is a gap of two clockcycles between each digit enable. This allows for the stabilization of the BCD data, which is multiplexed at the same rate.

Pins 20-23

These BCD outputs contain three full digits of information during digit-select times 2,3, and 4. During digit-select time 1, the half digit, overrange, underrange, and polarity codes are available. Table 1 shows the format of the BCD information during the times when Digit Select 1 (pin 19) is enabled.

Pin 15

This Overrange pin is normally high. It goes low when the unknown input voltage exceeds the full-scale reference voltage.

Pin 17

This pin connects to the most negative power supply, V_{EE}. Note that the output drive current does not return through this pin, but rather through pin 13.

Pin 13

This pin, V_{SS}, is the negative return for the output drivers (BCD, Digit Select, End of Conversion, Overrange). When this pin is connected to analog ground (pin 1), the output voltage swings from ground to V_{DD}. When connected to V_{EE}, the swing is from V_{EE} to V_{DD}. The allowable range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.

Pin 24

This pin connects to the most positive power supply, V_{DD}.

368
REV L
Sheet 2

TABLE 1. INFORMATION FORMAT FOR DIGIT SELECT 1

Coded Condition of MSD	BCD Outputs				BCD to Seven-Segment Decoding
	8 (pin 23)	4 (pin 22)	2 (pin 21)	1 (pin 20)	
+0	1	1	1	0	Blank
-0	1	0	1	0	
+0 UNDR	1	1	1	1	
-0 UNDR	1	0	1	1	
+1	0	1	0	0	4 → 1
-1	0	0	0	0	0 → 1
+1 OVR	0	1	1	1	7 → 1
-1 OVR	0	0	1	1	3 → 1

Hook up only segments "b" and "c" to MSD display

NOTES:

BCD8 = Display half digit: High for 0, Low for 1.

BDC4 = Display Polarity: High for +, Low for -.

BCD1 = Out of Range condition when High (1).
Used with BCD8 to show Underrange (BDC8 = 1) or Overrange (BCD8 = 0).

BCD2: Used to establish unique hex codes for a "1" display when decoder is connected to a full-digit display in the MSD position. Has no meaning for a half-digit display.

UNDR = Underrange: Occurs when count is less than 180 (e.g., ≤ 180 mV on 2- V scale).

OVR = Overrange: Occurs when count is 1999 (e.g., 199.9 mV on 200 mV scale).

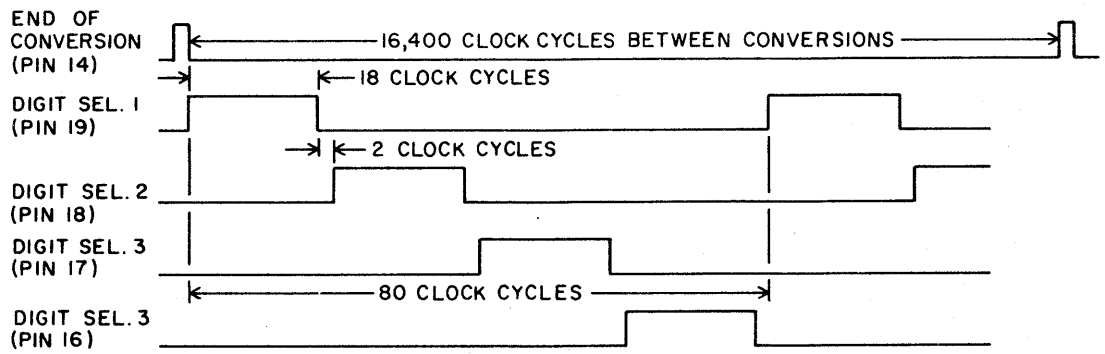
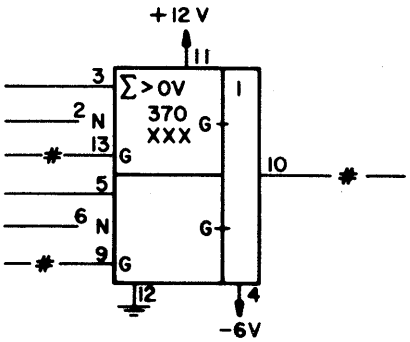


Figure 1. Digit Select Timing

368
Rev K
Sheet 3

DESCRIPTION

The 370 circuit consists of two high-gain voltage comparators with separate differential inputs and a common output. Individual strobes (G) allow independent gating of the inputs to each section. The circuit has a voltage gain of 500.

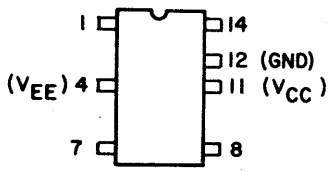


(# IDENTIFIES BINARY LOGIC SIGNAL)

LOGIC SYMBOL

NOTES:

1. Vendor identification: 711C
2. Package pin configuration.

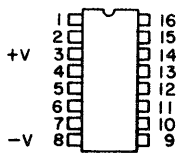


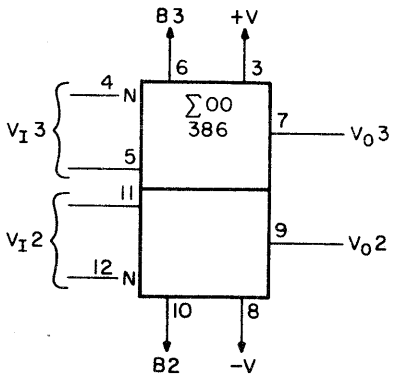
DESCRIPTION

Element 386 consists of three independent operational transconductance amplifiers and an independent bias regulator. Maximum potential between +V and -V pins is 14 volts. Typical common-mode input voltage range is +4.6 to -5.2 volts.

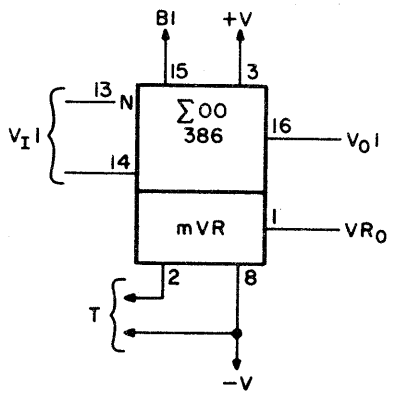
NOTES

1. Vendor identification: CA3060AD
2. Package pin configuration:





AND



B=BIAS COMPONENTS
T=TERMINATION COMPONENTS
m=-V + 7 V

LOGIC SYMBOL

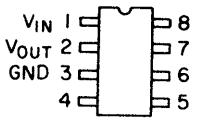
386
Rev M
Sheet 1 of 1

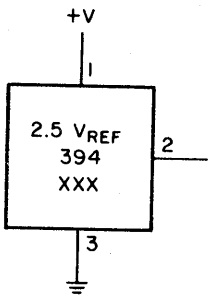
DESCRIPTION

Element 394 is a precision, band-gap, low-voltage reference that maintains a uniform output of 2.5 V (±25 mV) over an input-voltage range from 4.5 V to 35 V. Output current is 10 mA. It is designed for critical instrumentation and D/A converter applications.

NOTES:

1. Vendor identification: 1403U
2. Package pin configuration:



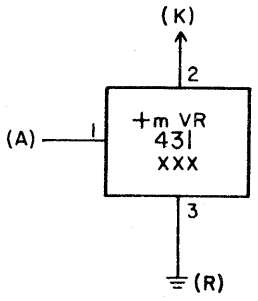


LOGIC SYMBOL

394
Rev. J
Sheet 1 of 1

DESCRIPTION:

Element 431 is an adjustable shunt regulator. Output voltages may be regulated between 2.5 V and supply voltage (max = 36 V) by connecting two external resistors between the anode (A) and cathode (K), and using them as a voltage-divider to provide a reference-voltage input to pin (R). The device has sharp turn-on characteristics that make it highly suitable for Zener diode applications.

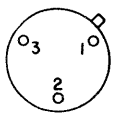


REPLACE m WITH NOMINAL VOLTAGE DETERMINED BY VOLTAGE DIVIDER INPUT TO PIN 3

LOGIC SYMBOL
UA431C

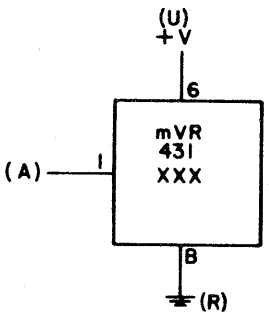
NOTES:

1. Vendor identification: μA431C, TL431C
2. Package pin configuration



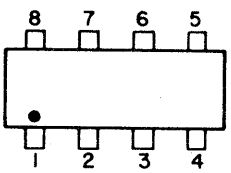
BOTTOM VIEW
UA431C

OR



REPLACE m WITH NOMINAL VOLTAGE DETERMINED BY VOLTAGE DIVIDER INPUT TO PIN 8

LOGIC SYMBOL
TL431C



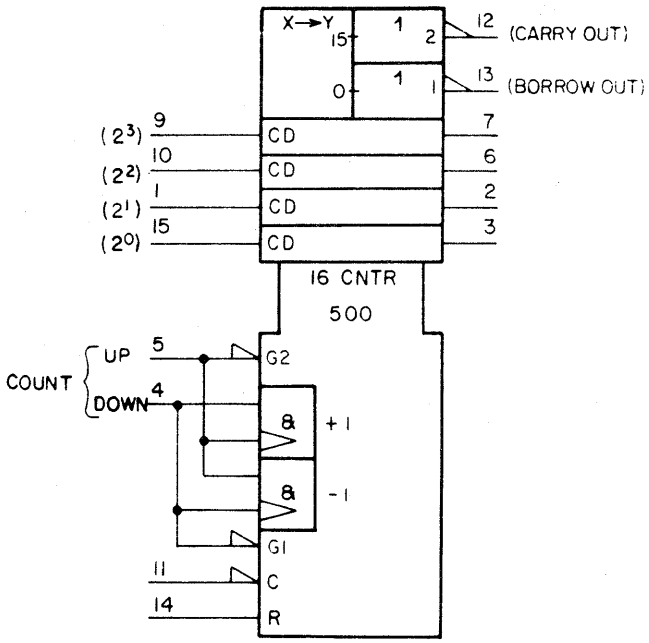
TOP VIEW
TL431C

431
Rev M
Sheet 1 of 1

DESCRIPTION

The 500 circuit is a synchronous 4-bit up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable; that is, the counter may be preset to any state by entering the desired data at the data inputs while the load input (pin 11) is low. The output will then change to agree with the data inputs independently of the count pulses. A high level applied to the clear input forces all outputs to the low level. The clear function is independent of the count and load inputs.



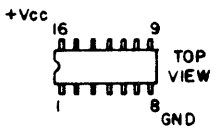
LOGIC SYMBOL

NOTES:

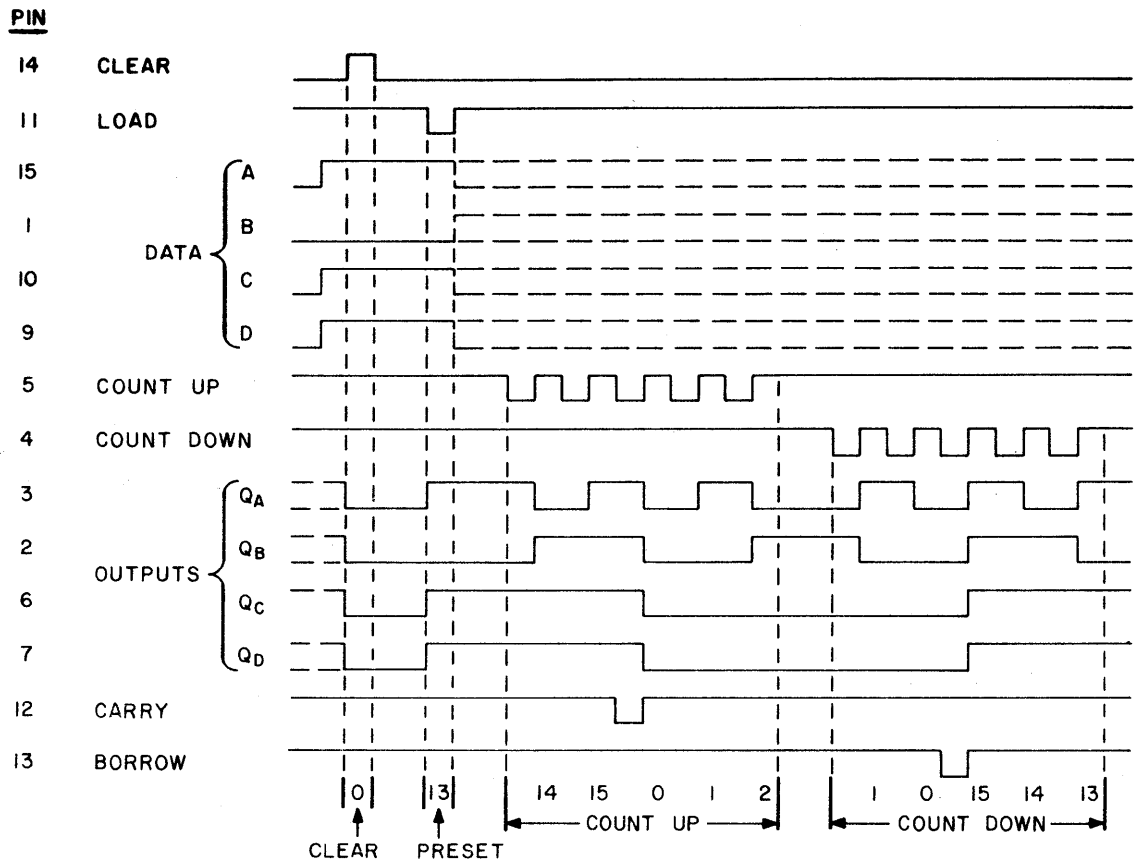
1. Input/Output identifiers are not part of the symbol.
2. Vendor identification:

Element	Vendor Number
500	74193,9366
500LS	74LS193

3. Package pin configuration.



500
Rev J
Sheet 1 of 3

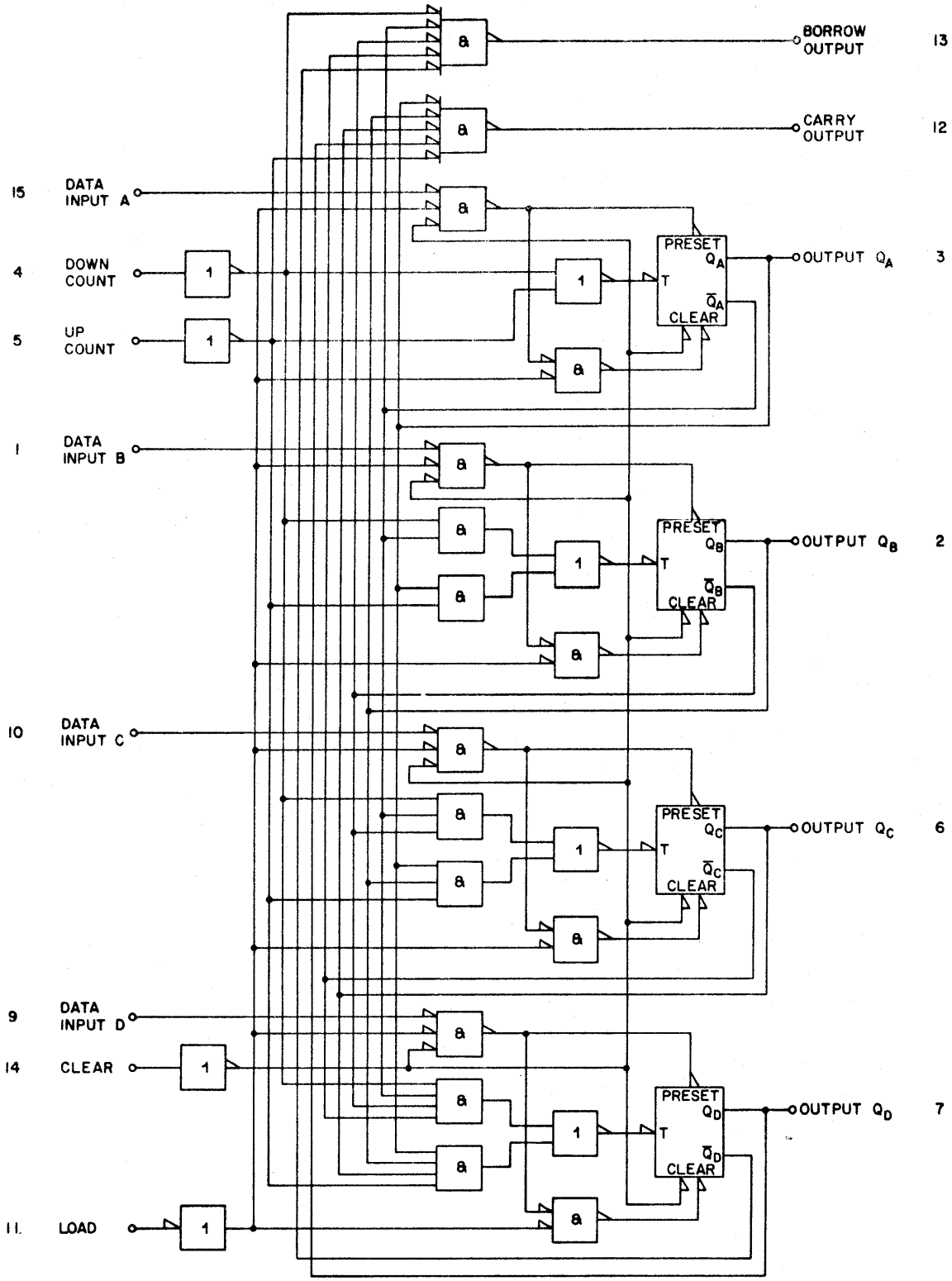


NOTE:

ILLUSTRATED ABOVE IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUTS TO ZERO.
2. LOAD (PRESET) TO BCD THIRTEEN.
3. COUNT UP TO FOURTEEN, FIFTEEN, CARRY, ZERO, ONE AND TWO.
4. COUNT DOWN TO ONE, ZERO, BORROW, FIFTEEN, FOURTEEN AND THIRTEEN.

COUNTING SEQUENCE



FUNCTION DIAGRAM

500
Rev J
Sheet 3 of 3

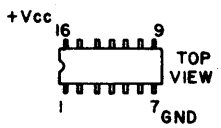
DESCRIPTION

The 501 circuit is a 5-bit comparator that provides comparison between two 5-bit words and gives three outputs: "less than", "greater than", and "equal to". A high level on the active low enable (pin 1) forces all three outputs low.

NOTES:

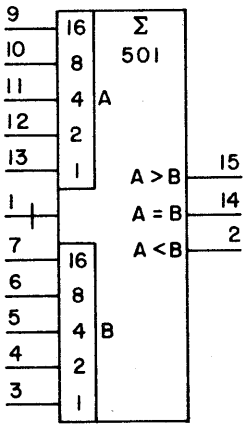
1. Vendor identification: 9324

2. Package pin configuration.



3. Pin names:

Pin	Function
1	Enable (active low) input
9,10,11,12,13	Word A parallel inputs
3,4,5,6,7	Word B parallel inputs
2	A Less Than B (A < B) output
14	A Equal to B (A=B) output
15	A Greater Than B (A > B) output



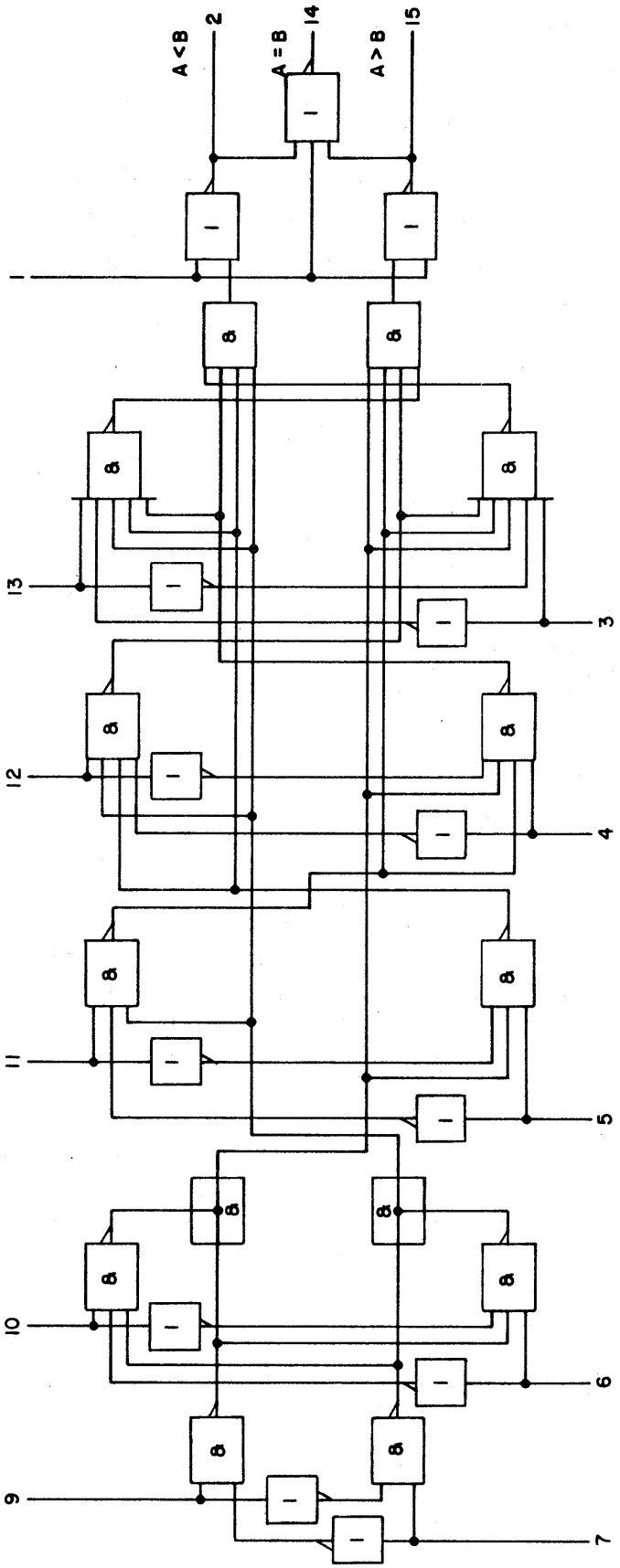
LOGIC SYMBOL

	INPUT		OUTPUT		
I	A	B	A < B	A > B	A = B
H	X		L	L	L
L	WORD A = WORD B		L	L	H
L	WORD A > WORD B		L	H	L
L	WORD A < WORD B		H	L	L

H = HIGH LEVEL
L = LOW LEVEL
X = EITHER HIGH OR LOW LEVEL

TRUTH TABLE

501
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

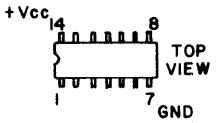
501
Rev J
Sheet 2 of 2

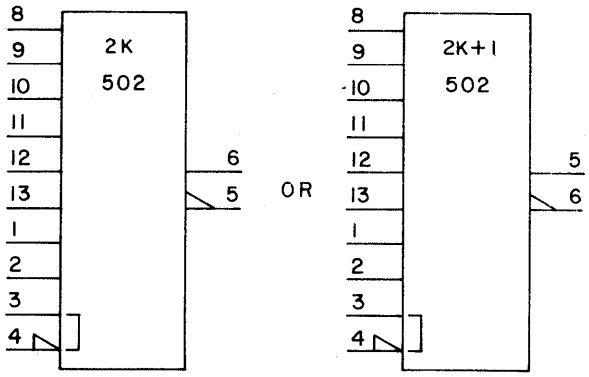
DESCRIPTION

The 502 circuit is an 8-bit parity generator/checker with complementry outputs and control inputs to facilitate operation in either odd-or even-parity applications.

NOTES:

1. Vendor identification: 74180
2. Package pin configuration.



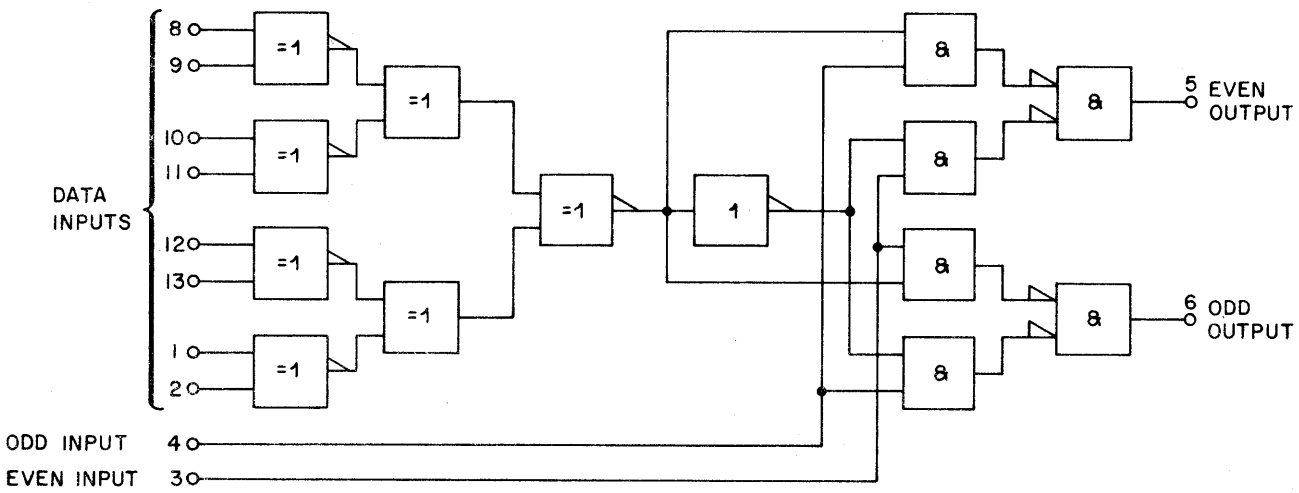


LOGIC SYMBOL

INPUTS			OUTPUTS	
Σ OF 1's AT PINS 1, 2, 8 THRU 13	PIN 3	PIN 4	PIN 5	PIN 6
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0.	1	1

X = IRRELEVANT

TRUTH TABLE

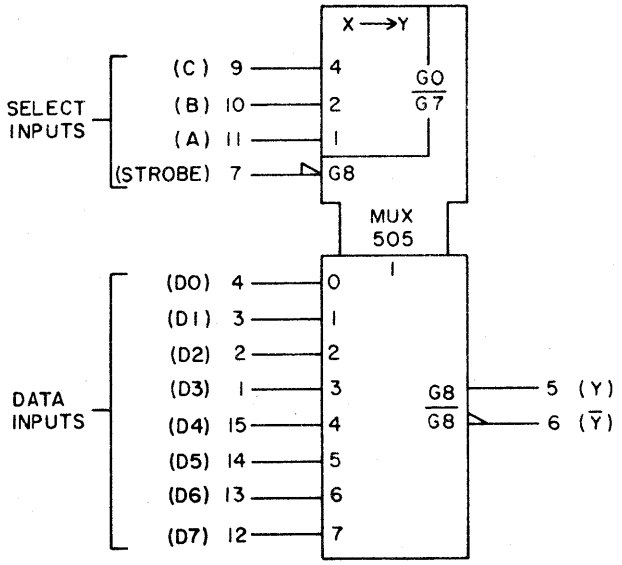


FUNCTION DIAGRAM

502
Rev J
Sheet 1 of 1

DESCRIPTION

Element 505 is a 1-of-8 multiplexer/selector that takes data from one of eight data inputs, depending upon the state of the select inputs, and gates it to pin 5 when G8 (strobe input) goes low. When the strobe input is high,pin 5 will be low. Pin 6 is the complement of pin 5.



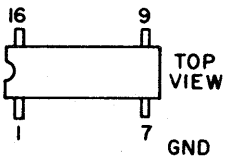
LOGIC SYMBOL

NOTES:

1. Vendor identification:

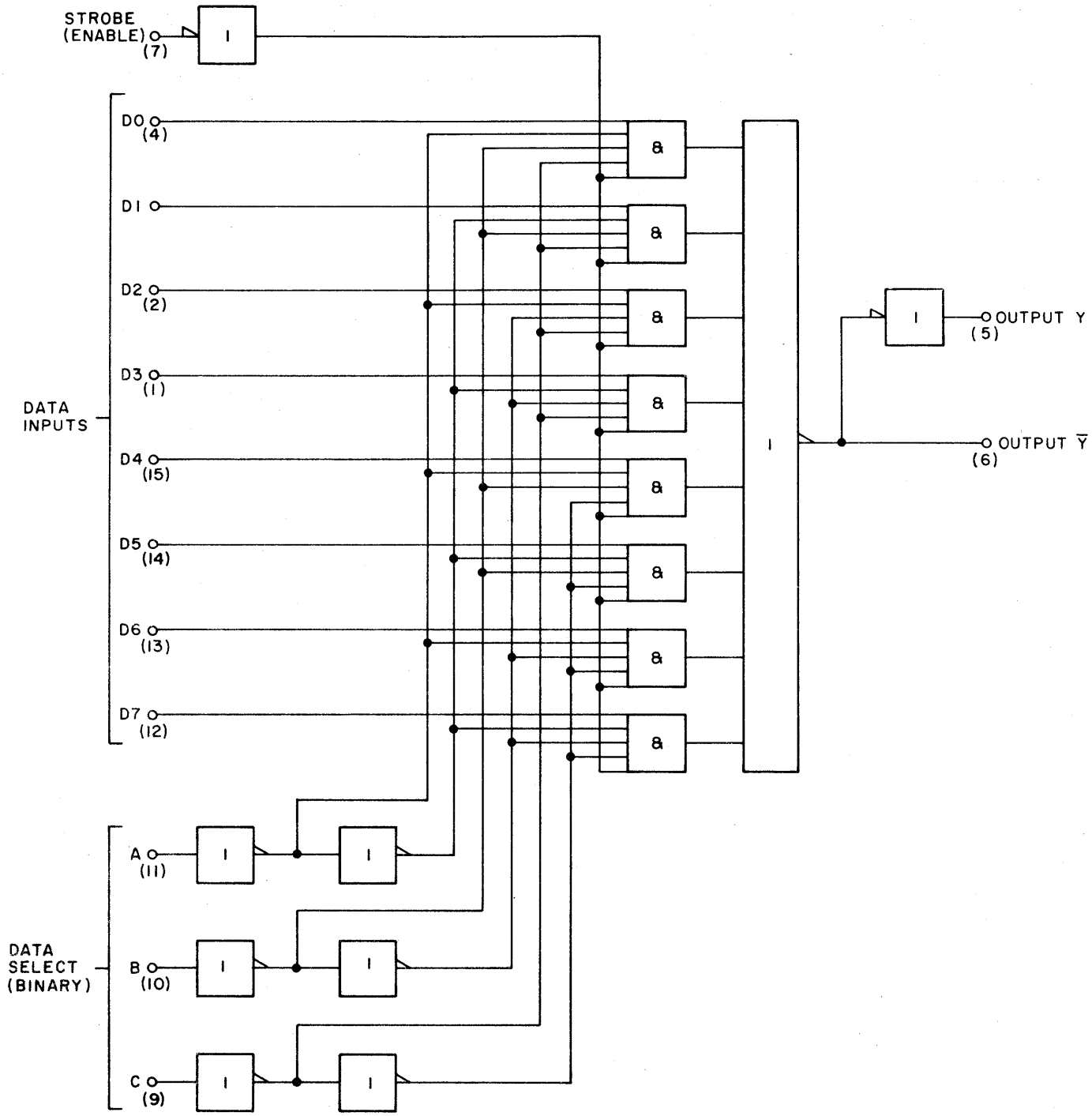
Element	Vendor Number
505	74151
505S	74S151

2. **Package pin configuration.** +Vcc



INPUTS												OUTPUTS	
C	B	A	STROBE	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	0	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

TRUTH TABLE



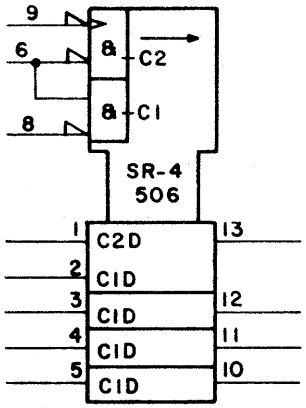
FUNCTIONAL DIAGRAM

505
Rev J
Sheet 2 of 2

DESCRIPTION

The 506 circuit is a 4-bit shift register capable of shifting right, shifting left, or parallel-in, parallel-out operations. When the mode input (pin 6) is low, the parallel inputs (pins 2 through 5) and clock 2 input (pin 8) are disabled. Serial data may then be entered at pin 1 and shifted right from pin 10 toward pin 13 under control of the right shift clock (pin 9). When the clock input is high, the serial input is enabled. When the clock goes low, the serial input is disabled, and the data is transferred to output pin 13. The right shift of data at the outputs also occurs at this time.

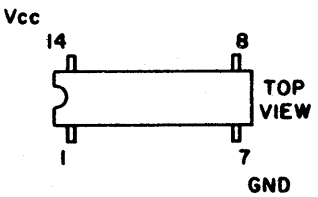
When the mode input is high, the serial input and right shift clock are disabled and the circuit now functions as four R-S master-slave FF's with a common clock input, clock 2 (pin 8). By connecting pin 10 to pin 4, pin 11 to pin 3, and pin 12 to pin 2, a left-shift register is formed with input pin 5 as the serial input and pin 8 as the left shift clock. Thus, the circuit can shift left or right at independent clock rates by controlling the mode input.



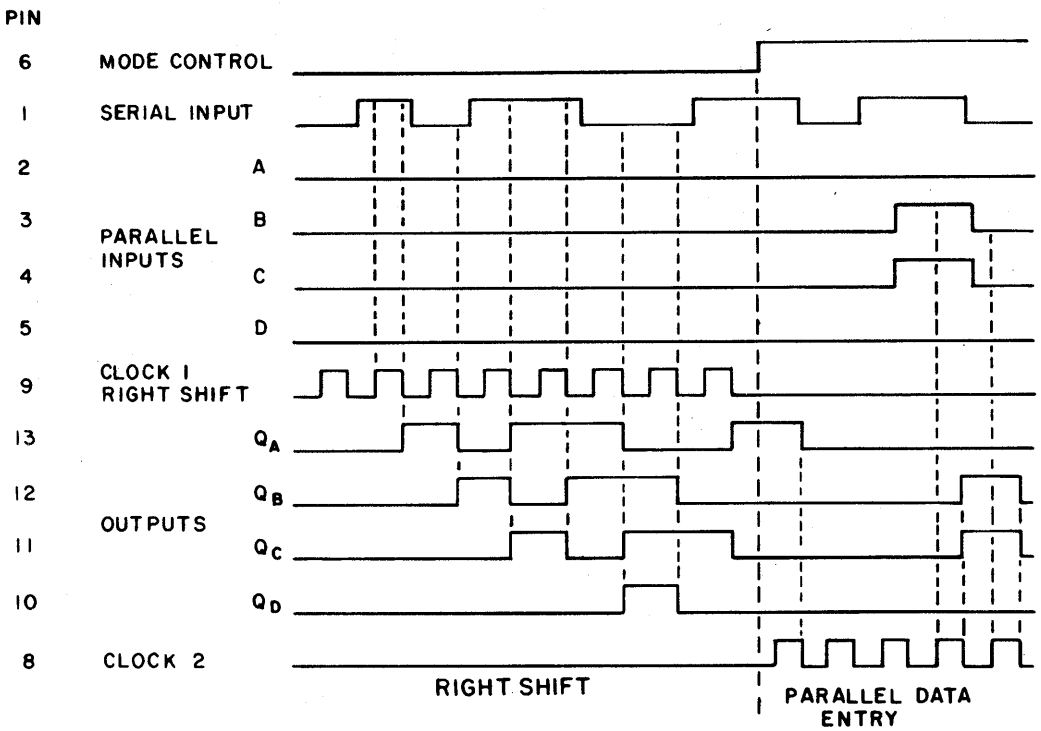
LOGIC SYMBOL

NOTES:

1. **Vendor identification: 7495A**
2. **Package pin configuration:**

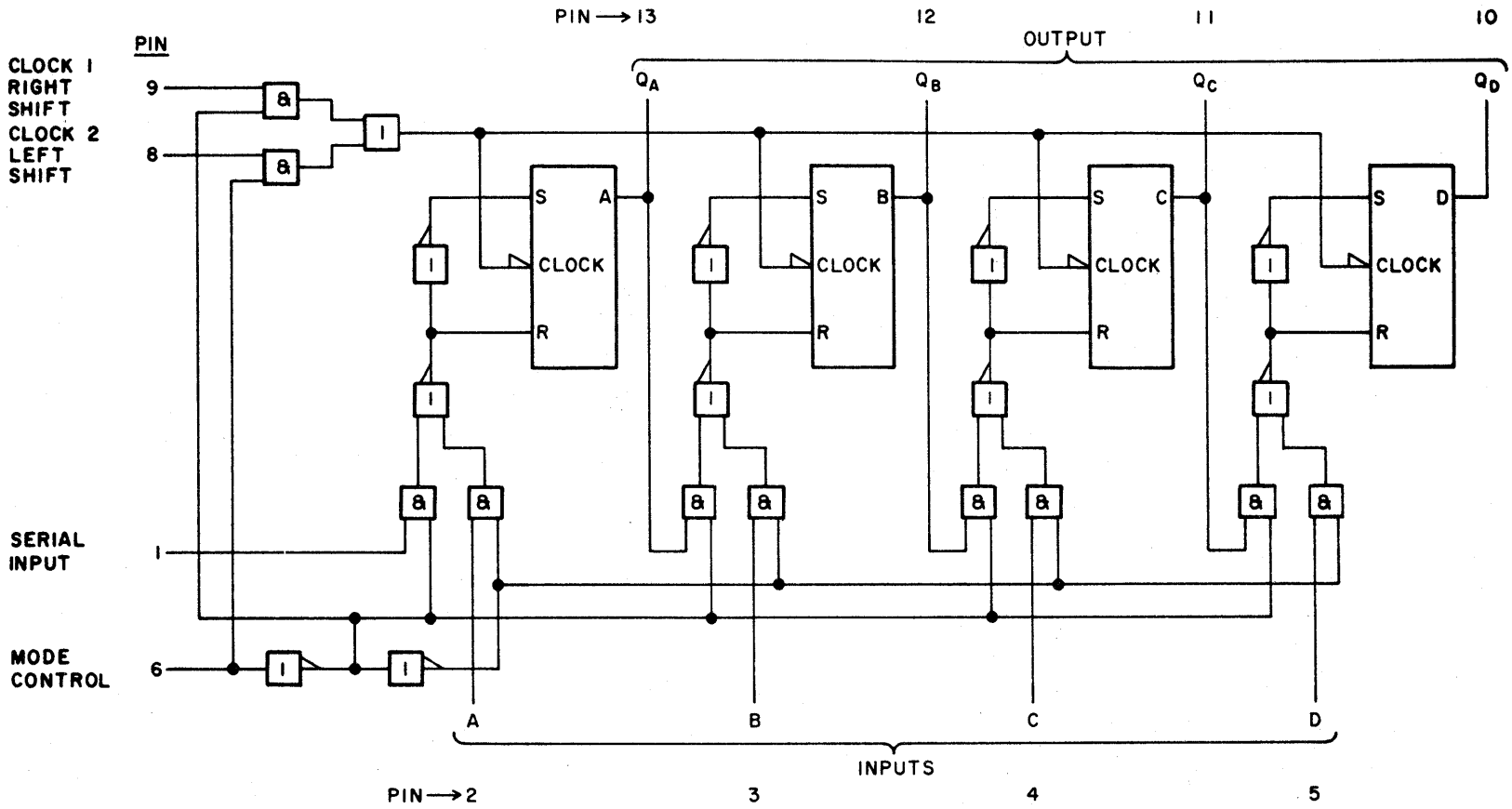


506
Rev J
Sheet 1 of 3



FUNCTION SEQUENCE

506
Rev J
Sheet 2 of 3

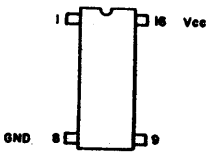

PIN → 13
12
11
10
OUTPUT
PIN
CLOCK 1
RIGHT
SHIFT
CLOCK 2
LEFT
SHIFT
9
8
Q_A
Q_B
Q_C
Q_D
S A
S B
S C
S D
CLOCK
R
SERIAL
INPUT
1
MODE
CONTROL
6
A
B
C
D
INPUTS
PIN → 2
3
4
5

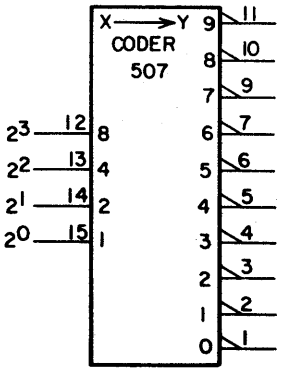
DESCRIPTION

The 507 circuit is a 4-line-to-10-line (BCD-to-decimal) decoder. For encoded input counts of 0 through 9 (0000-1001), the appropriate decimal output goes low. For other input states (1010-1111), all outputs are high.

NOTES:

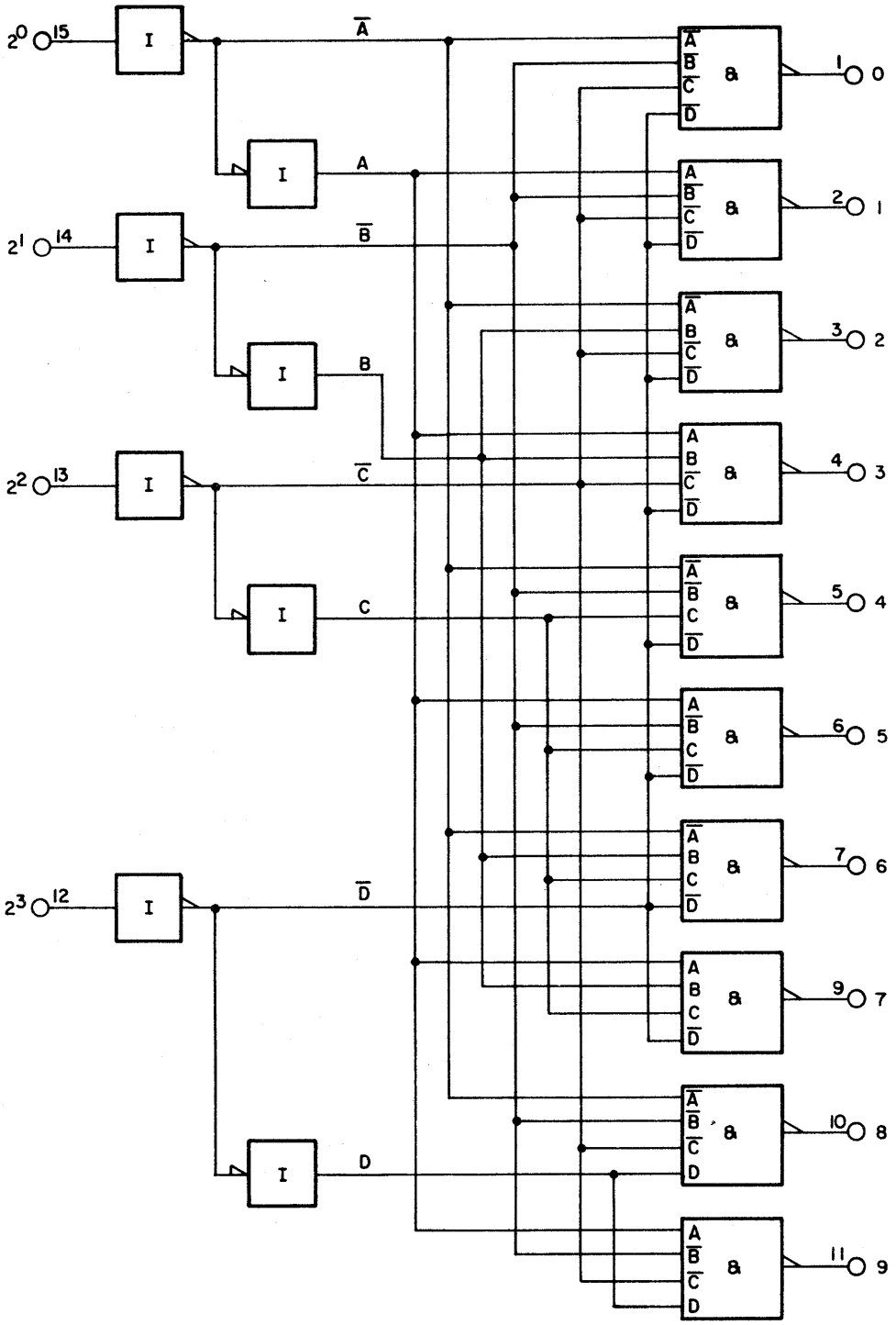
1. Vendor identification: 7442/9352
2. Package pin configuration:





LOGIC SYMBOL

507
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

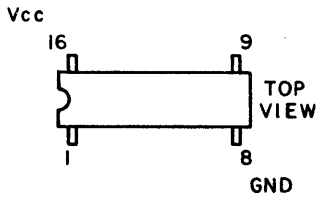
507
Rev J
Sheet 2 of 2

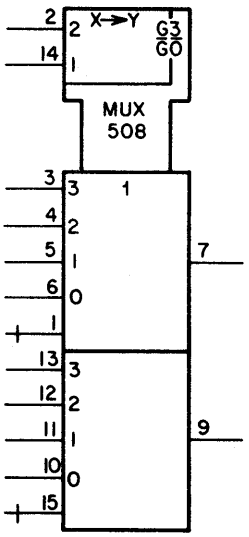
DESCRIPTION

Element 508 consists of two 4-line-to-1-line multiplexers with common select inputs and a separate low-active enable (high-active inhibit) input for each section. When either inhibit/enable input (pins 1, 15) is high, the output from that section will be low, regardless of which data input has been selected. When inhibit/enable is low, the output follows that of the selected data input.

NOTES:

1. Vendor Identification: 74153
2. Package pin configuration.





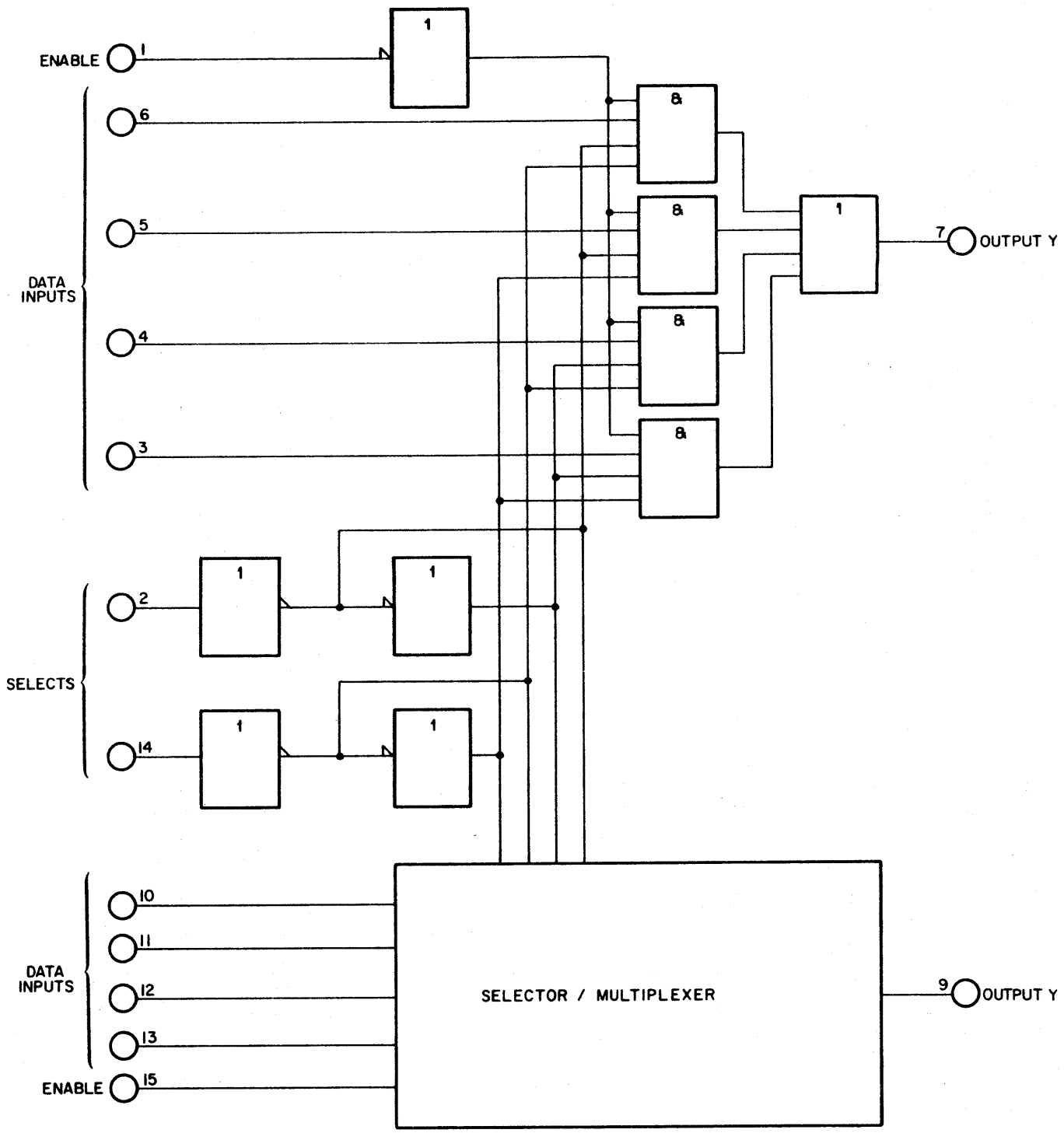
LOGIC SYMBOL

SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
2	14	6	5	4	3	1	7
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH
L = LOW
X = EITHER HIGH OR LOW

TRUTH TABLE

508
Rev. J
Sheet 1 of 2



LOGIC DIAGRAM

508
Rev. J
Sheet 2 of 2

DESCRIPTION

The 509 circuit is a 4-bit, high-speed, parallel arithmetic logic unit (ALU). It can perform 16 different arithmetic operations or 16 different logic operations on active high or active low data. The function table on page 509-2 lists these operations.

Placing a high on the mode control input (M) causes the 509 circuit to perform logic operations on the individual bits as listed. When the mode control input is low, the device performs arithmetic operations on the two 4-bit words. The carry out Cn+4 signal provides for ripple carry between devices, or for carry look-ahead between packages using the carry propagate (P) and carry generate (G) signals. In slower circuits, the 509 circuit may be used in a ripple carry mode by connecting the $\overline{Cn+4}$ signal to the carry input ($\overline{Cn}$) of the next unit. Using the 509 circuit in conjunction with the 510 circuit, carry look-ahead circuit makes possible high speed operation. Each group of four 509's requires one 510.

The 509 circuit subtracts by 1's complement addition and generates the 1's complement of the subtrahend internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

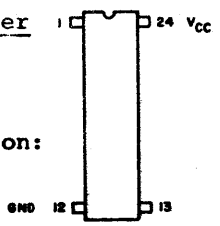
Logic equivalence between the four bits of A and the four bits of B is indicated by the A = B output being high when the unit is in the subtract mode. The open-collector A = B output can be wire-AND connected to other A = B outputs to give a comparison for more than four bits. Used with the carry out signal, the A = B signal can indicate A > B and A < B. The A = B output must connect to a pull-up resistor tied to Vcc.

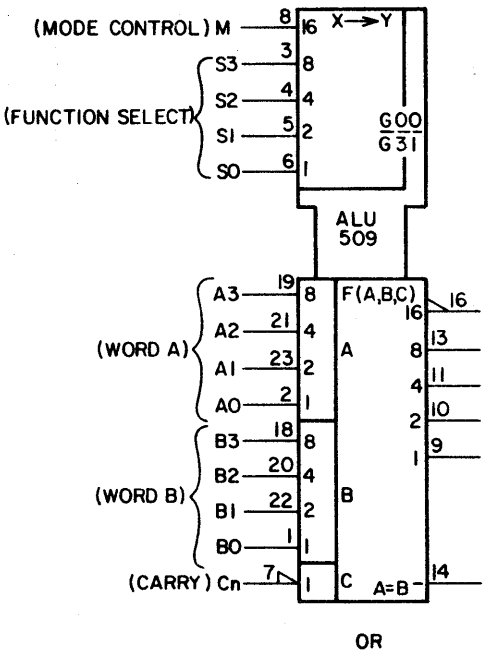
NOTES:

1. Vendor identification:

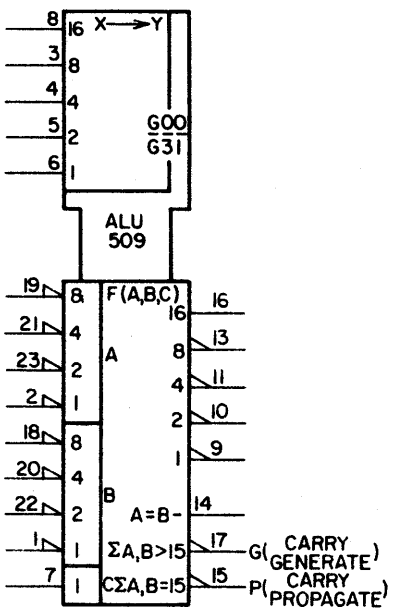
Element	Vendor Number
509	74181
509S	74S181

2. Package pin configuration:





OR



LOGIC SYMBOL

509
Rev J
Sheet 1 of 3

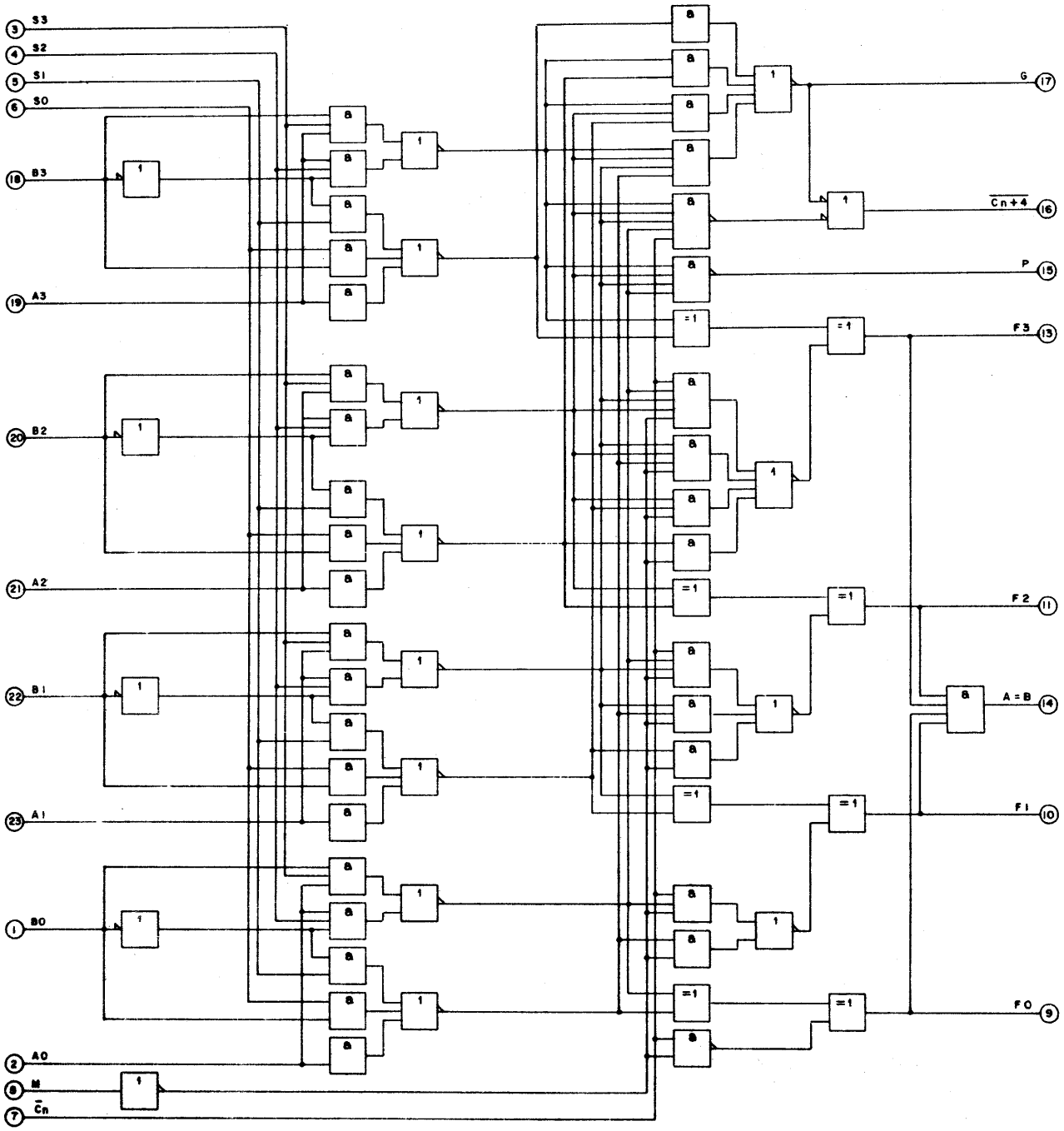
MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS		ACTIVE HIGH INPUTS AND OUTPUTS	
S3	S2	S1	S0	LOGIC (M=H)	ARITHMETIC (M=L)(Cn=L) (1)	LOGIC (M=H)	ARITHMETIC (M=L)(Cn=H) (1)
L	L	L	L	$\overline{A}$	A MINUS 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB MINUS 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	$A\overline{B}$ MINUS 1	$\overline{A}B$	$A+\overline{B}$
L	L	H	H	LOGICAL 1	MINUS 1	LOGICAL 0	MINUS 1
L	H	L	L	$\overline{A+B}$	A PLUS $(A+\overline{B})$	$\overline{AB}$	A PLUS $A\overline{B}$
L	H	L	H	$\overline{B}$	AB PLUS $(A+\overline{B})$	$\overline{B}$	$(A+B)$ PLUS $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A MINUS B MINUS 1	$A \oplus B$	A MINUS B MINUS 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ MINUS 1
H	L	L	L	$\overline{A}B$	A PLUS $(A+B)$	$\overline{A+B}$	A PLUS AB
H	L	L	H	$A \oplus B$	A PLUS B	$\overline{A \oplus B}$	A PLUS B
H	L	H	L	B	$A\overline{B}$ PLUS $(A+B)$	B	$(A+\overline{B})$ PLUS AB
H	L	H	H	A + B	$A+\overline{B}$	AB	AB MINUS 1
H	H	L	L	LOGICAL 0	A PLUS A (2)	LOGICAL 1	A PLUS A (2)
H	H	L	H	$A\overline{B}$	AB PLUS A	$A+\overline{B}$	$(A+B)$ PLUS A
H	H	H	L	AB	$A\overline{B}$ PLUS A	A + B	$(A+\overline{B})$ PLUS A
H	H	H	H	A	A	A	A MINUS 1

(1) Add "plus 1" to arithmetic operation when Cn is active.

(2) Each bit is shifted to the next more significant position.

FUNCTION TABLE

509
Rev J
Sheet 2 of 2



FUNCTIONAL DIAGRAM

509
Rev J
Sheet 3 of 3

DESCRIPTION:

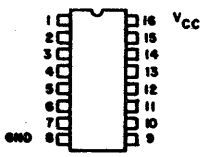
The 510 circuit is a look-ahead carry generator. It is generally used with the type 509 arithmetic logic unit circuit to provide carry look-ahead capability. Each 510 circuit accepts up to four pairs of active-low carry propagate (P_0, P_1, P_2, P_3) and carry generate (G_0, G_1, G_2, G_3) signals and an active-high carry input (Cn). The 510 circuit can anticipate a carry across four adders or groups of adders, and provides the anticipated active-high carries (C_{n+X}, C_{n+Y}, C_{n+Z}). The 510 circuit also has active-low carry propagate (P) and carry generate (G) outputs for cascading. Cascaded 510 circuits can provide look-ahead across N-bit adders.

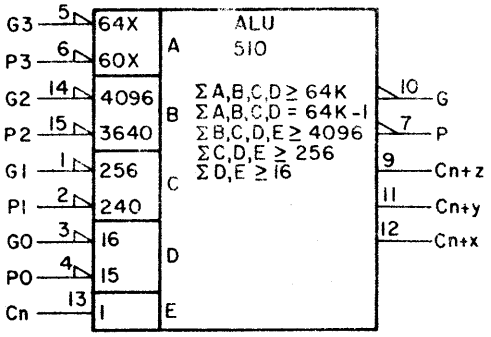
NOTES

1. Vendor identification:

Element	Vendor Number
510	74182
510S	74S182

2. Package pin configuration:





G0, G1, G2 AND G3 — CARRY GENERATE INPUTS

P0, P1, P2 AND P3 — CARRY PROPAGATE INPUTS

C - CARRY INPUT

Cn+x, Cn+y, AND Cn+z — CARRY OUTPUTS

G - CARRY GENERATE OUTPUT

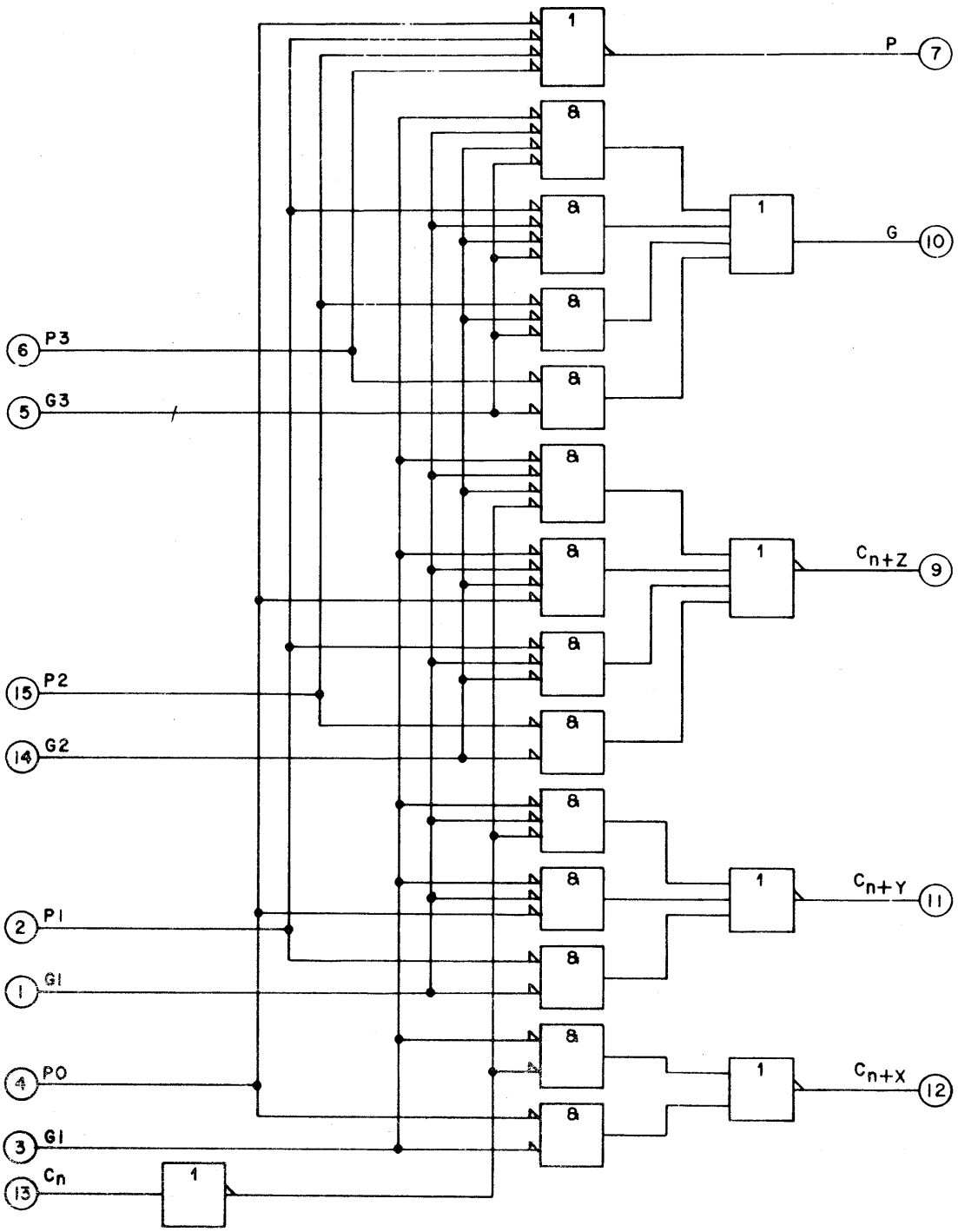
P - CARRY PROPAGATE OUTPUT

LOGIC SYMBOL

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+X}	C_{n+Y}	C_{n+Z}	G	P
X	H	H									L		
L	H	X									L		
X	L	X									H		
H	X	L									H		
X	X	X	H	H							L		
X	H	H	H	X							L		
L	H	X	H	X							L		
X	X	X	L	X							H		
X	L	X	X	L							H		
H	X	L	X	L							H		
X	X	X	X	X	H	H						L	
X	X	X	H	H	H	X						L	
X	H	H	H	X	H	X						L	
L	H	X	H	X	H	X						L	
X	X	X	X	X	L	X						H	
X	X	X	L	X	X	L						H	
X	L	X	X	L	X	L						H	
H	X	L	X	L	X	L						H	
	X		X	X	X	X	H	H					H
	X		X	X	H	H	H	X					H
	X		H	H	H	X	H	X					H
	H		H	X	H	X	H	X					H
	X		X	X	X	X	L	X					L
	X		X	X	L	X	X	L					L
	X		L	X	X	L	X	L					L
	L		X	L	X	L	X	L					L
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

TRUTH TABLE

510
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

510
Rev J
Sheet 2 of 2

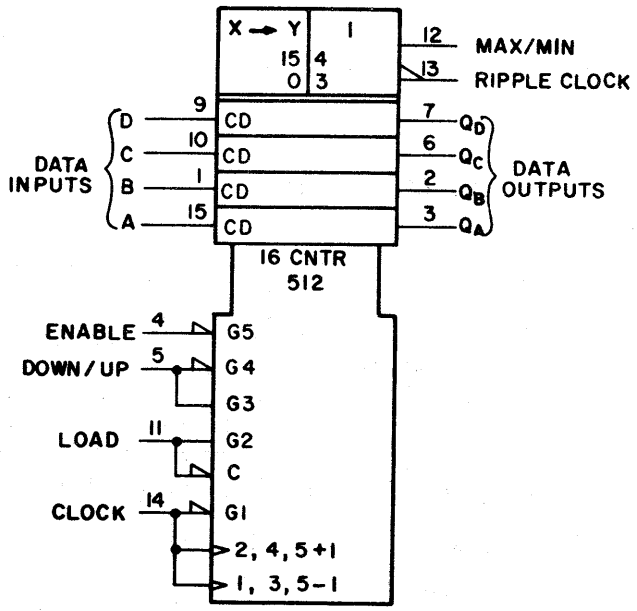
DESCRIPTION

The 512 circuit is a 4-bit binary, synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

The counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will then change to agree with the data inputs independently of the state of the clock input.

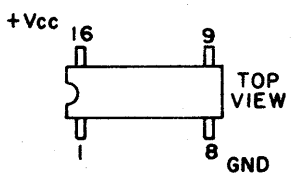
Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.



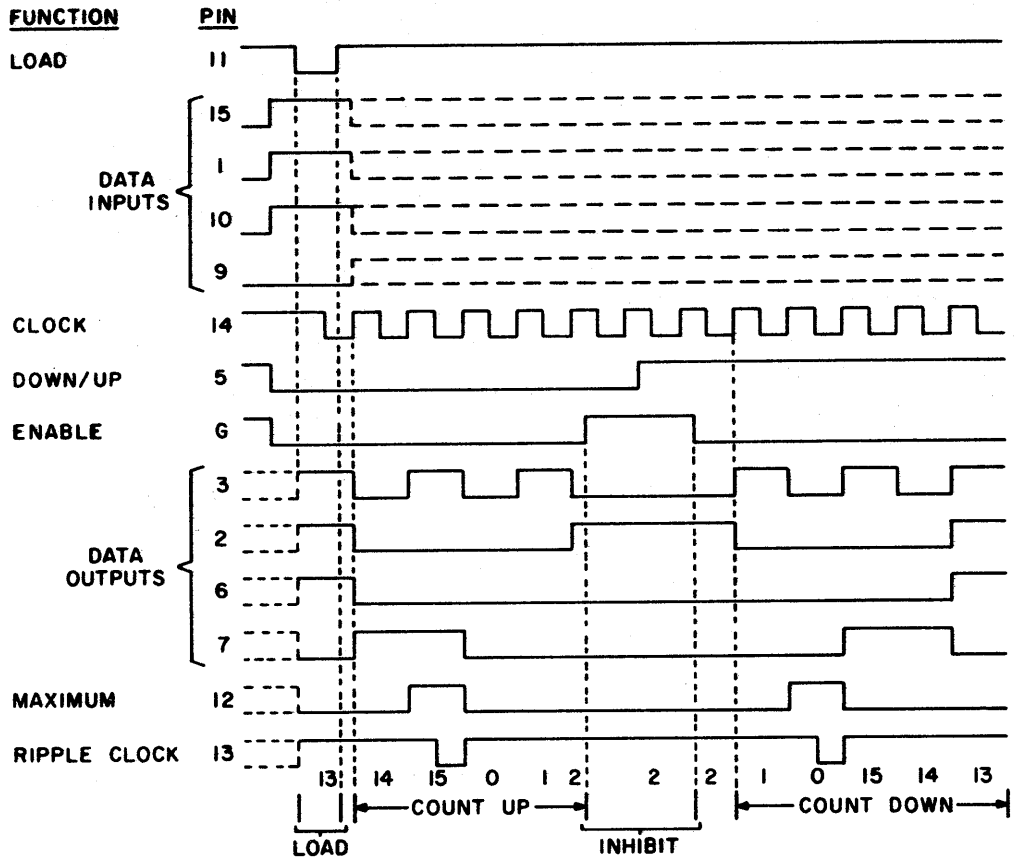
LOGIC SYMBOL

NOTES:

1. Vendor identification: 74191, 9336
2. Package pin configuration:



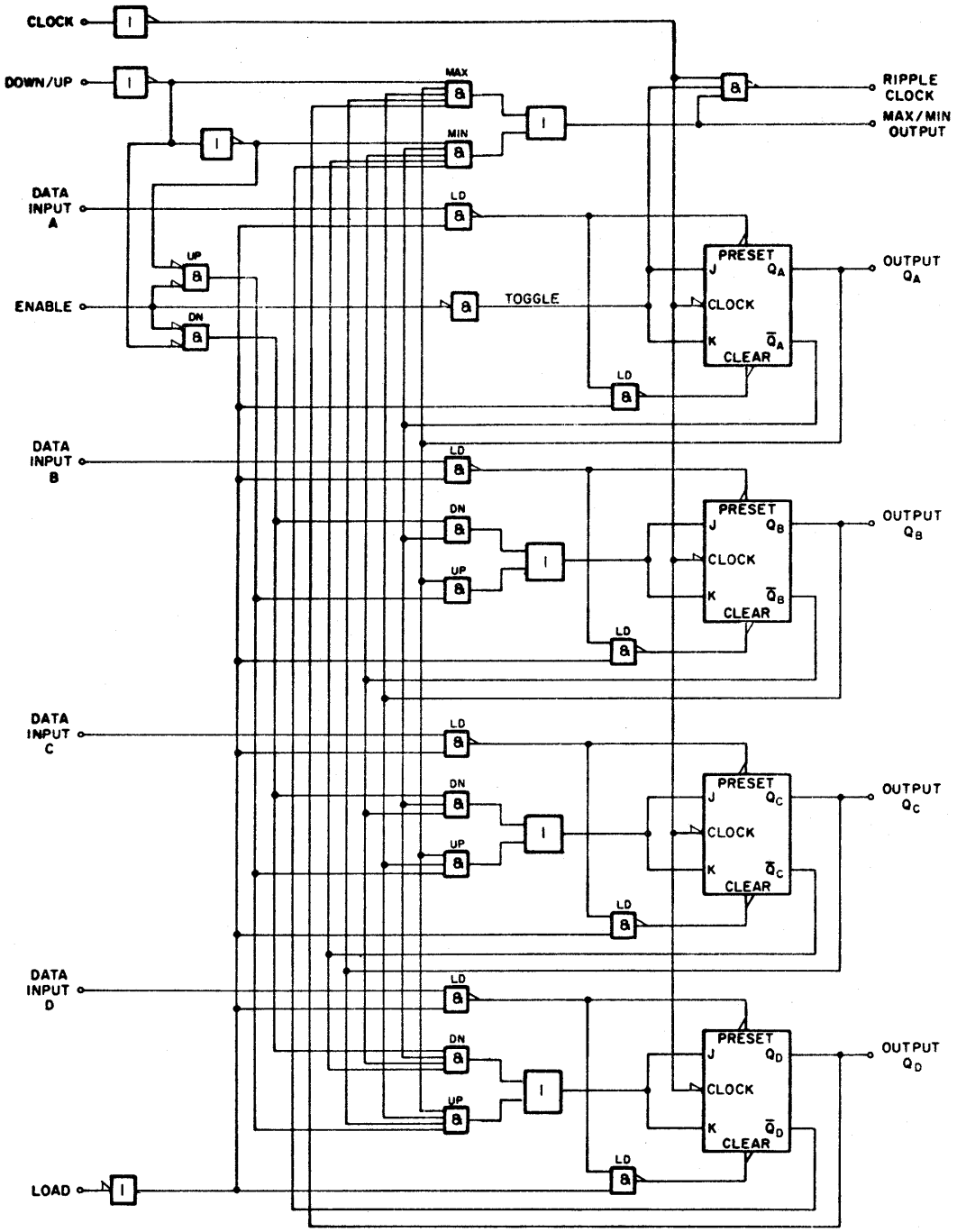
512
Rev J
Sheet 1 of 3



1. LOAD (PRESET) TO BINARY THIRTEEN.
2. COUNT UP TO FOURTEEN, FIFTEEN (MAXIMUM) ZERO, ONE, AND TWO.
3. INHIBIT.
4. COUNT DOWN TO ONE, ZERO (MINIMUM), FIFTEEN, FOURTEEN, AND THIRTEEN.

TYPICAL, LOAD, COUNT, AND INHIBIT SEQUENCES

512
Rev J
Sheet 2 of 3



FUNCTION DIAGRAM

512
Rev J
Sheet 3 of 3

DESCRIPTION

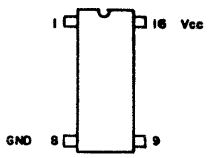
Element 514 is a 16-bit (4x4) random-access register file/memory with open-collector outputs and non-destructive readout. Separate Read/Write addressing permits reading from one 4-bit word location while simultaneously writing into another location.

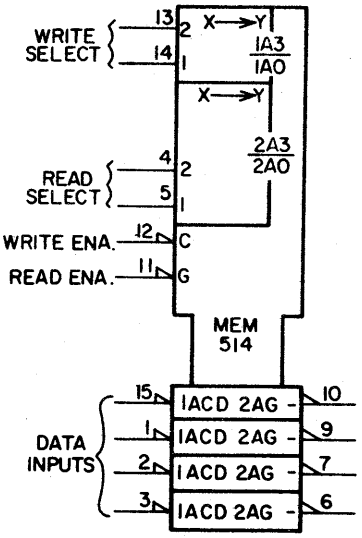
Writing or reading is accomplished when the corresponding enable signal is low. When the Read enable is high, all outputs will be high (see function tables).

Maximum read and write times are 35 and 45 ns, respectively.

NOTES:

1. Vendor identification 74170
2. Package pin configuration:





LOGIC SYMBOL

READ FUNCTION

INPUTS			OUTPUT PINS			
2	1	G	10	9	7	6
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

WRITE FUNCTION

INPUTS			WORD			
2	1	C	0	1	2	3
L	L	L	Q=D	Qn	Qn	Qn
L	H	L	Qn	Q=D	Qn	Qn
H	L	L	Qn	Qn	Q=D	Qn
H	H	L	Qn	Qn	Qn	Q=D
X	X	H	Qn	Qn	Qn	Qn

1. L = LOW, H = HIGH, X = DON'T CARE
2. W0B1: WORD 0, BIT 1, ETC.
3. Q=D: THE FOUR STORED BITS WILL ASSUME THE BINARY VALUE OF THE FOUR DATA INPUT BITS.
4. Qn: NO CHANGE

514
Rev J
Sheet 1 of 1

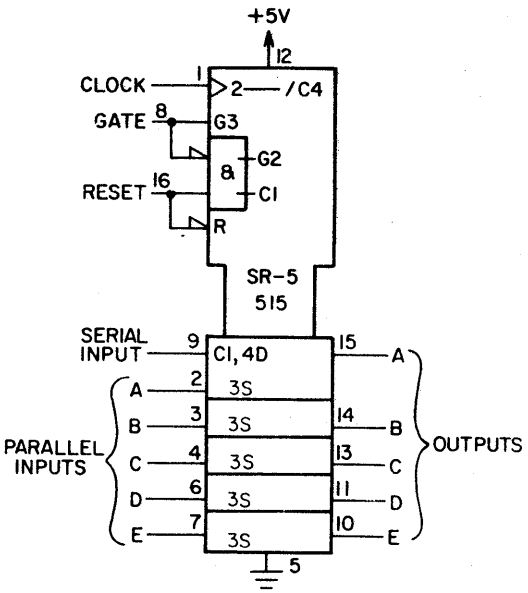
DESCRIPTION

The 515 shift resister consists of five set-reset, master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both the inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the low state by applying a low voltage to the reset input (pin 16). This condition may be applied independent of the clock input (pin 1).

The flip-flops may be independently set to the high state by applying a high to both the set input of the specific flip-flop and the common Gate input G3 (pin 8). Input G3 is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. G3 is also independent of the clock input or clear input.

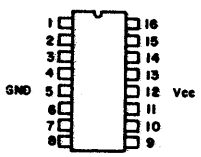
Transfer of information to the output pins occurs when the clock input goes from a low to a high. Since the flip-flops are J-K master-slave circuits, the proper information must appear at the two inputs of each flip-flop prior to the rising edge of the clock. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining flip-flop inputs. The reset input (pin 16) must be at a high and the gate G3 input must be at a low when clocking occurs.



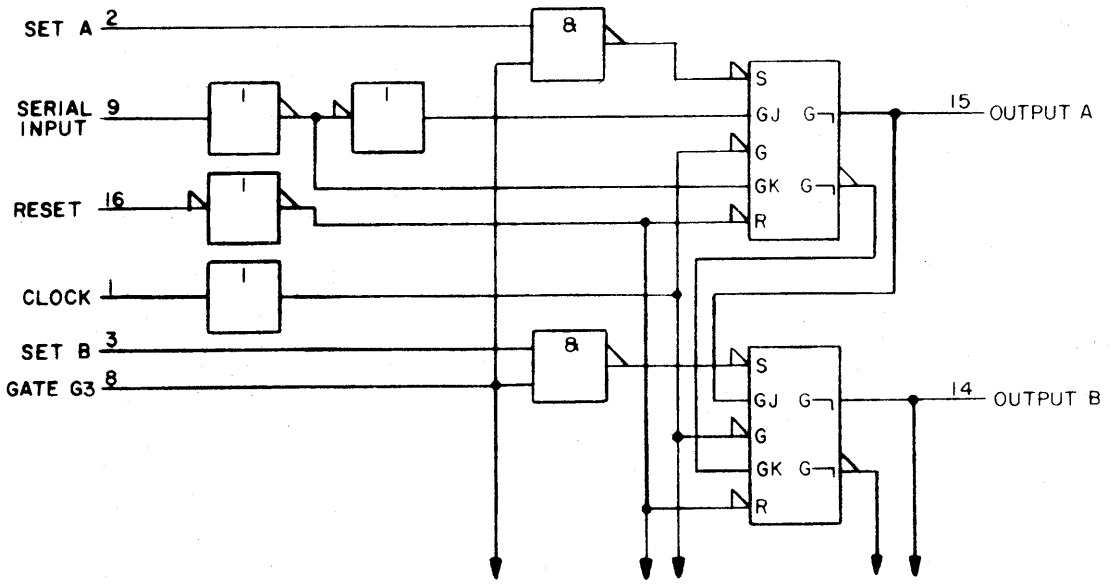
LOGIC SYMBOL

NOTES:

1. Vendor identification: 7496/9396
2. Package pin configuration:

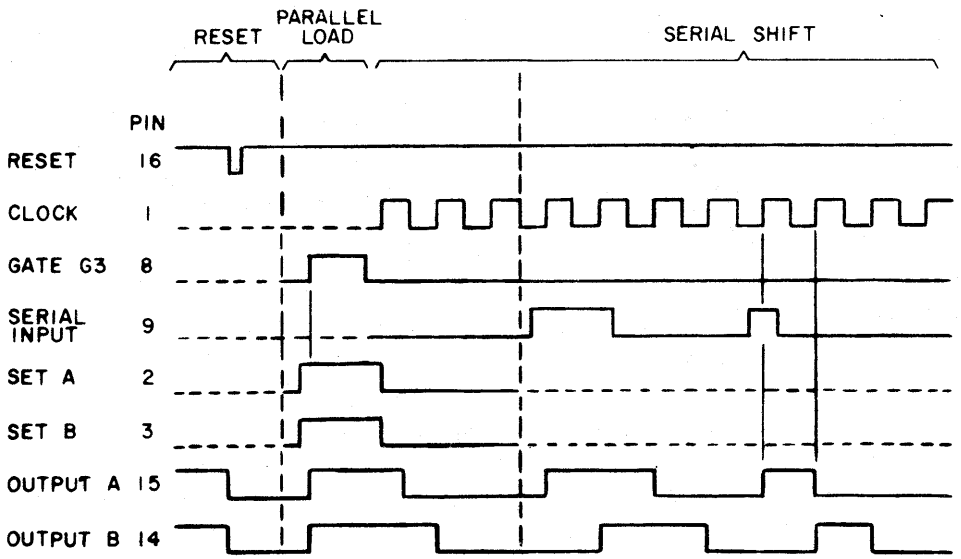


515
Rev J
Sheet 1 of 2



NOTE: FLIP-FLOPS C, D, AND E NOT SHOWN. THEY ARE IDENTICAL TO A AND B.

FUNCTIONAL DIAGRAM



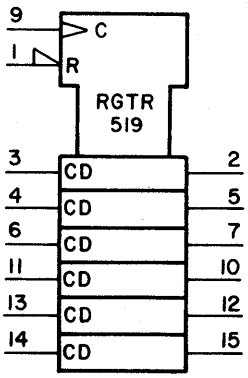
____ = LEVEL HAS NO EFFECT

TIMING DIAGRAM

515
Rev J
Sheet 2 of 2

DESCRIPTION

The 519 circuit is a register made up of six D-type flip-flops with common clock and clear inputs.



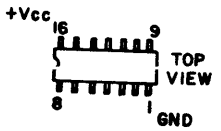
LOGIC SYMBOL

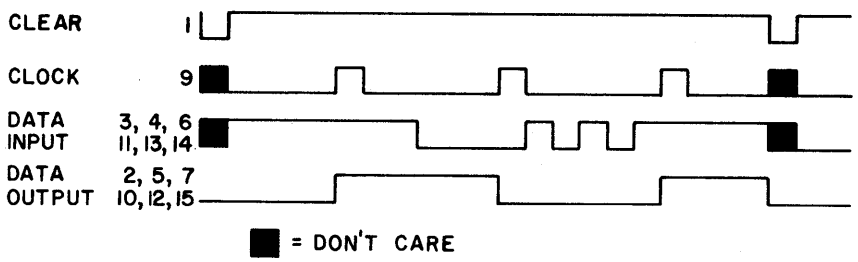
NOTES:

1. Vendor identification:

Element	Vendor Number
519	74174
519S	74S174

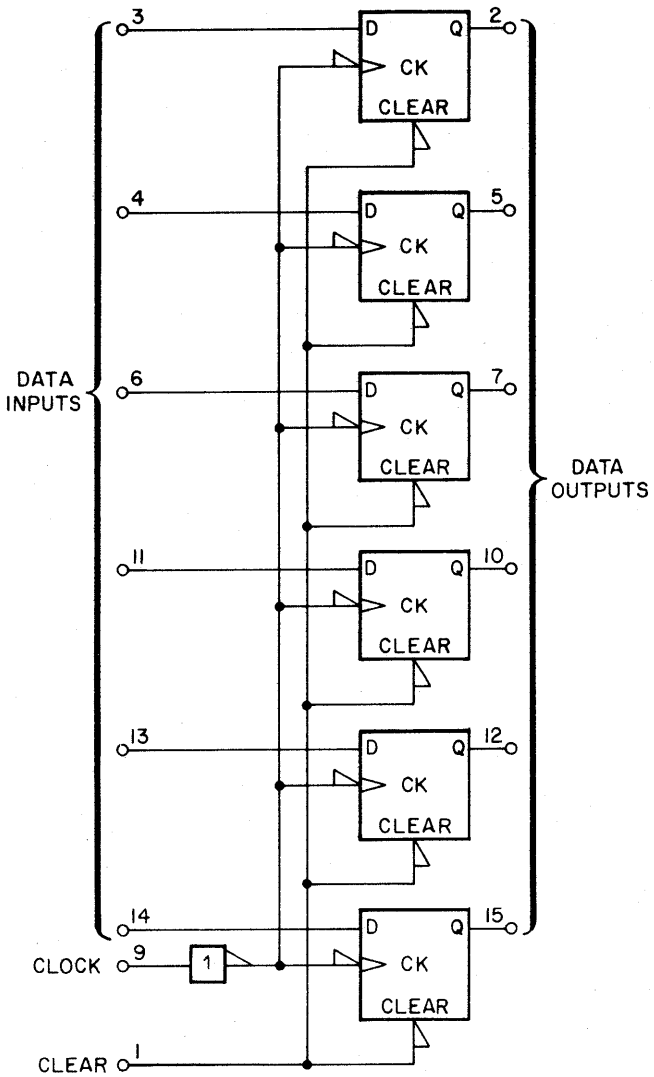
2. Package pin configuration.





FUNCTION SEQUENCE

519
Rev J
Sheet 1 of 2

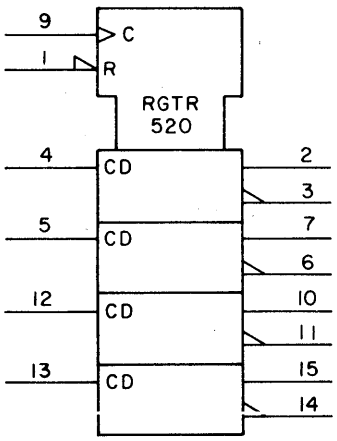


FUNCTION DIAGRAM

519
Rev K
Sheet 2 of 2

DESCRIPTION

Element 520 contains four positive-edge-triggered D-type flip-flops with common clock and reset (clear) inputs. Each FF has complementary outputs. Information at the input is transferred to the output on the positive-going transition of the clock pulse. When the clock is either high or low, input data has no effect on the outputs.



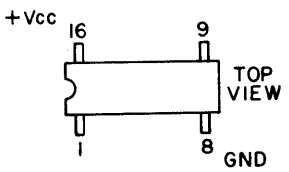
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
520	74175
520LS	74LS175
520S	74S175

2. Package pin configuration:



INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	NC	NC

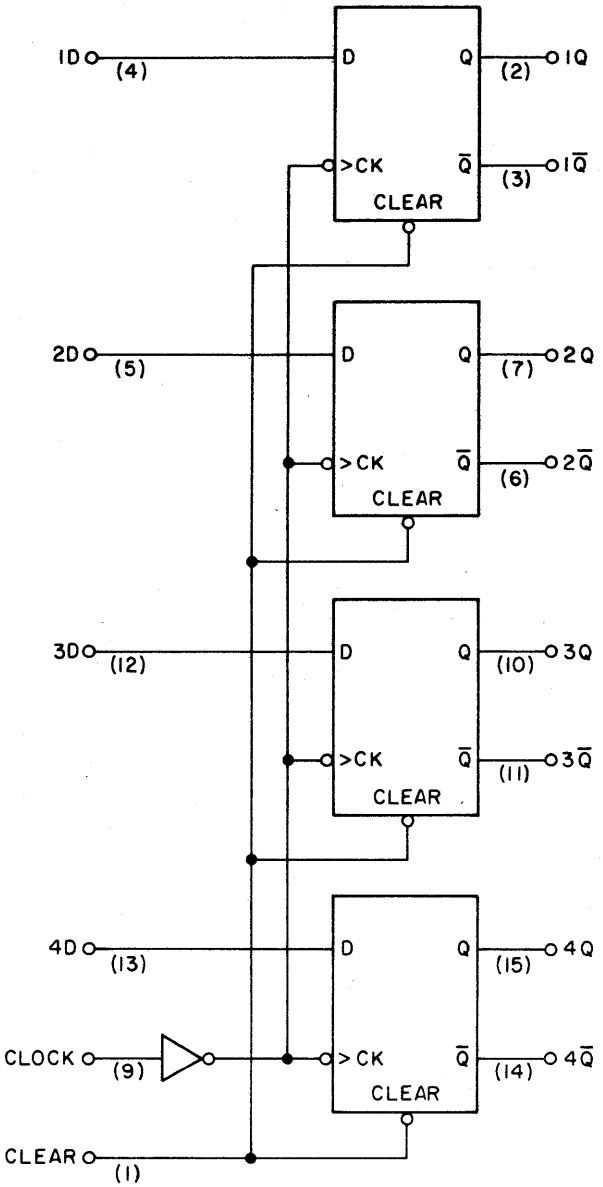
↑ = TRANSITION FROM LOW TO HIGH LEVEL

X = DON'T CARE

NC = SAME AS BEFORE INDICATED INPUT CONDITIONS WERE ESTABLISHED

TRUTH TABLE

520
Rev J
Sheet 1 of 2



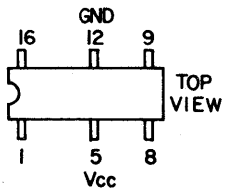
FUNCTIONAL DIAGRAM

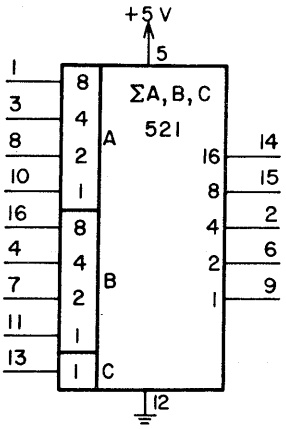
DESCRIPTION

The 521 circuit performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

NOTES:

1. Vendor identification: 7483
2. Package pin configuration.



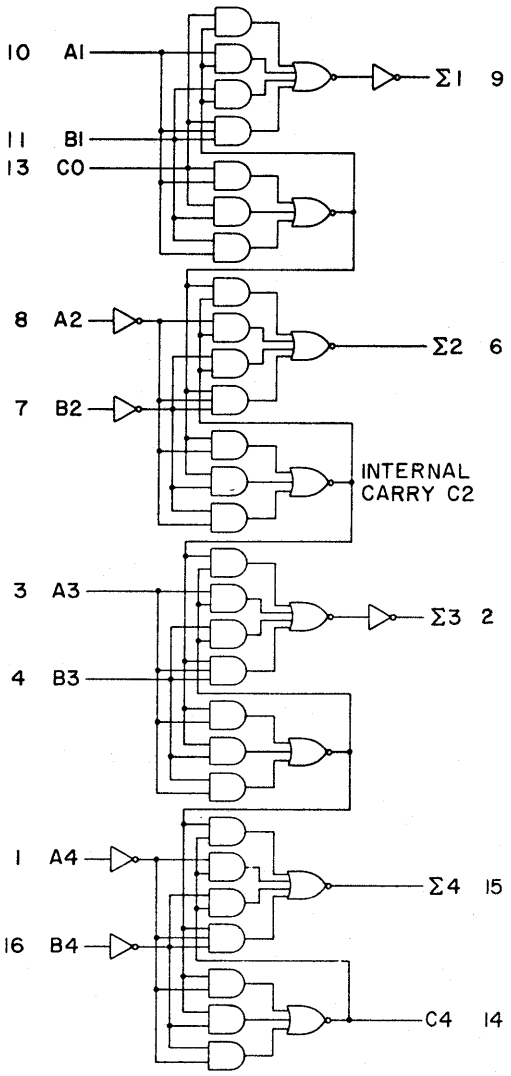


LOGIC SYMBOL

INPUT				OUTPUT					
				WHEN CO=L			WHEN CO=H		
				WHEN C2=L			WHEN C2=H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: INPUT CONDITIONS AT A1, A2, B1, B2, AND CO ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4, ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.

TRUTH TABLE



FUNCTION DIAGRAM

521
Rev J
Sheet 1 of 1

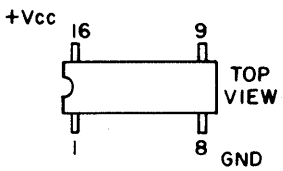
DESCRIPTION

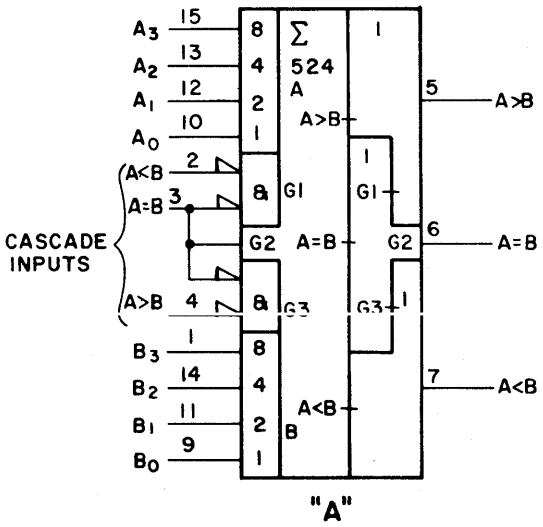
Element 524 performs a magnitude comparison of two 4-bit words (word A and word B). One of three conditions will exist and the output corresponding to that condition will be high (the other two will be low). For words greater than 4 bits, two or more circuits are cascaded using the cascade input (pins 2, 3 and 4).

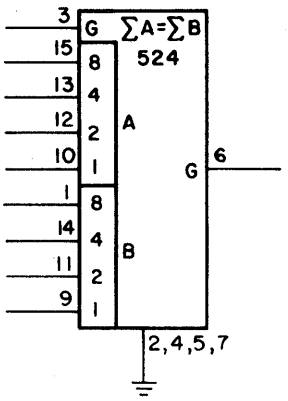
For applications requiring only an equality indication, the logic symbol may appear as in "B". In this usage, the grounded pins may not always be shown.

NOTES:

1. Vendor identification: 7485
2. Package pin configuration.





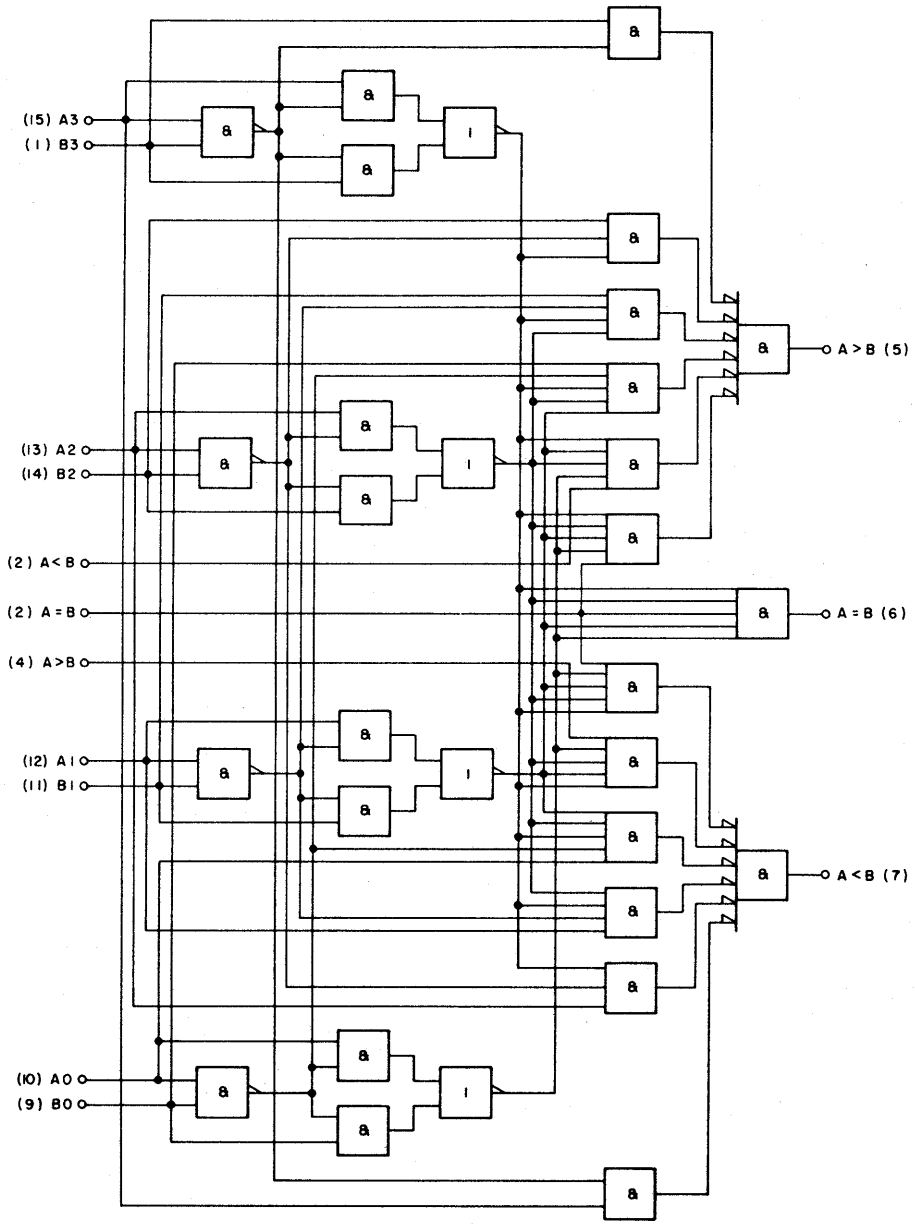


LOGIC SYMBOLS

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3 B3	A2 B2	A1 B1	A0 B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H

TRUTH TABLE

524
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

524
Rev J
Sheet 2 of 2

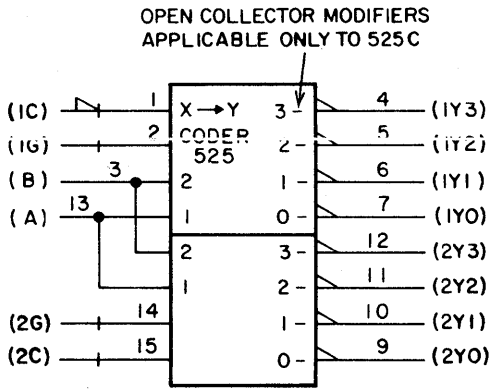
DESCRIPTION

General

Element 525* consists of two separate sections that are used as either 2-to-4 decoders or 1-to-4 demultiplexers. Each section has individual strobes and data inputs; however, they have common code inputs (select A and B). These circuits may also be used in combination to form either a 3-to-8 decoder or a 1-to-8 demultiplexer circuit. Figure 1 shows the functional diagram for this chip, with pin numbers in parentheses. The following paragraphs discuss each of the possible applications.

Dual Two-Line to Four-Line Decoder

When used in this manner (refer to Figure 2), the two-line code is applied to the common select inputs, A and B. The two output sections are then enabled individually via their strobe and data inputs. Outputs 1Y0-1Y3 are enabled when strobe input 1G is low and data input 1C is high. The other four-line output section (2Y0-2Y3) is enabled when both strobe 2G and data 2C are low.



LOGIC SYMBOL

*Element 525C is identical in pin configuration and function to 525, but provides open-collector outputs.

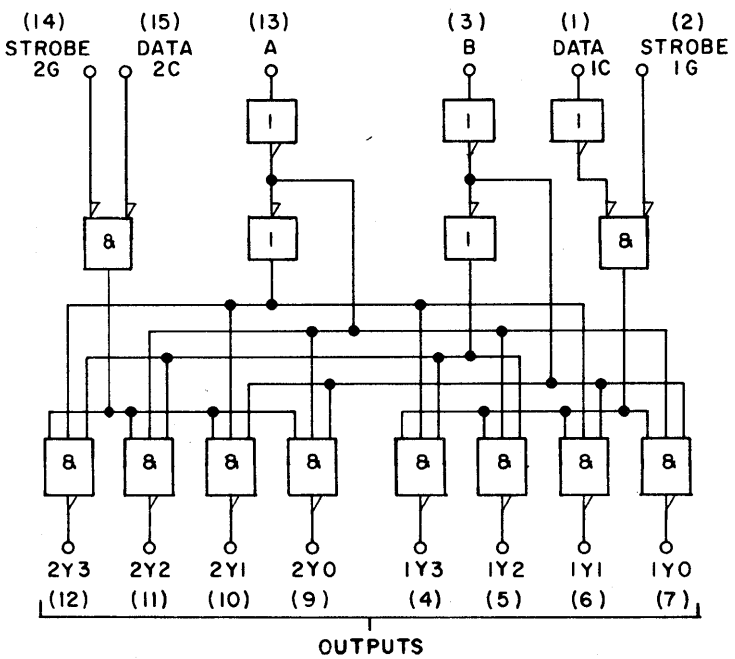


Figure 1. FUNCTIONAL DIAGRAM

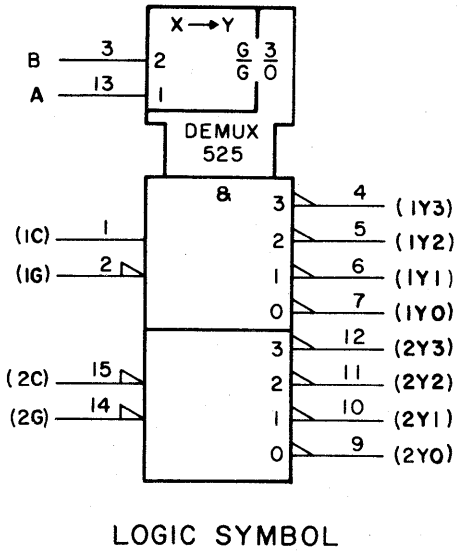
525
Rev J
Sheet 1 of 3

Dual One-Line to Four-Line Demultiplexer

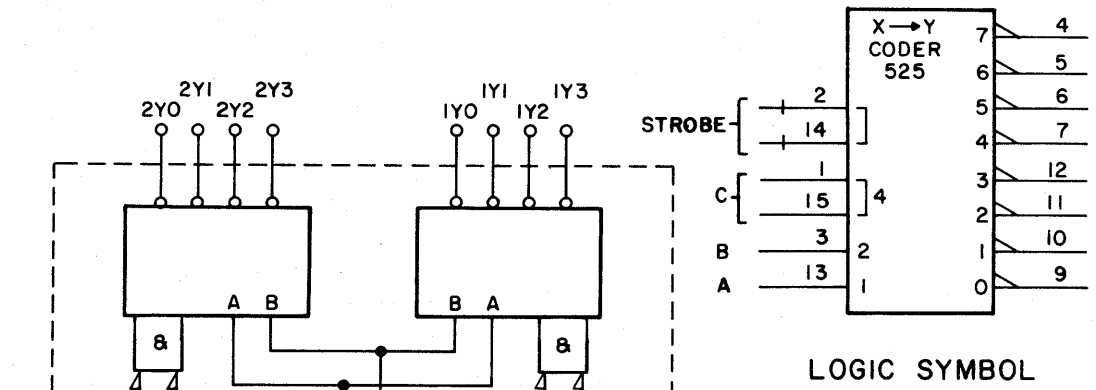
When used as a demultiplexer (refer to Figure 2), the serial input data is applied to each section via the data inputs 1C or 2C and what appears at the outputs is controlled by the A and B select lines. The two sections are enabled individually by their strobe inputs 1G or 2G.

Three-Line to Eight-Line Decoder

When used as a 3-to-8 decoder (Figure 3), the data inputs 1C and 2C are connected together and serve as a third select line (C). The strobes 1G and 2G are also connected together forming a common strobe. The code is then applied to the select inputs and the outputs are enabled when the strobe is low.



LOGIC SYMBOL



LOGIC SYMBOL

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Figure 2. Two Line to Four Line Decoder/ One Line to Four Line Demultiplexer

One-Line to Eight-Line Demultiplexer

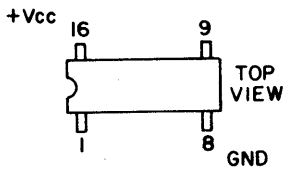
This application uses the same configuration as the 3-to-8 decoder; however, the common strobe line now serves as the data input and the outputs are controlled by the select lines (A, B and C). Refer to Figure 3.

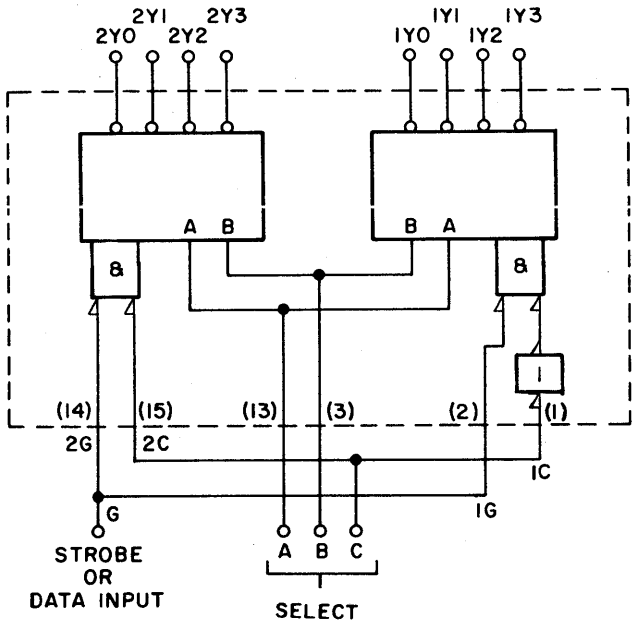
NOTES:

1. Vendor identification:

Element	Vendor Number
525	74155
525C	74156

2. Package pin configuration.



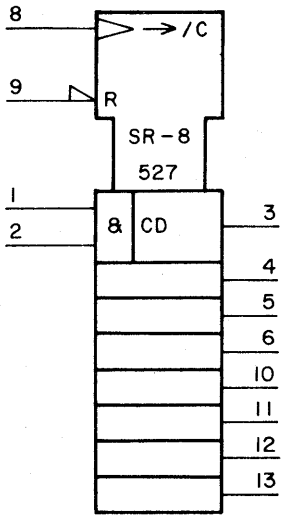


INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Figure 3. Three Line to Eight Line Decoder/ One Line to Eight Line Demultiplexer

DESCRIPTION

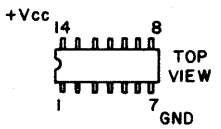
The 527 circuit is an 8-bit shift register with gated serial inputs and an asychronous clear. The gated serial inputs (pins 1 and 2) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requrements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

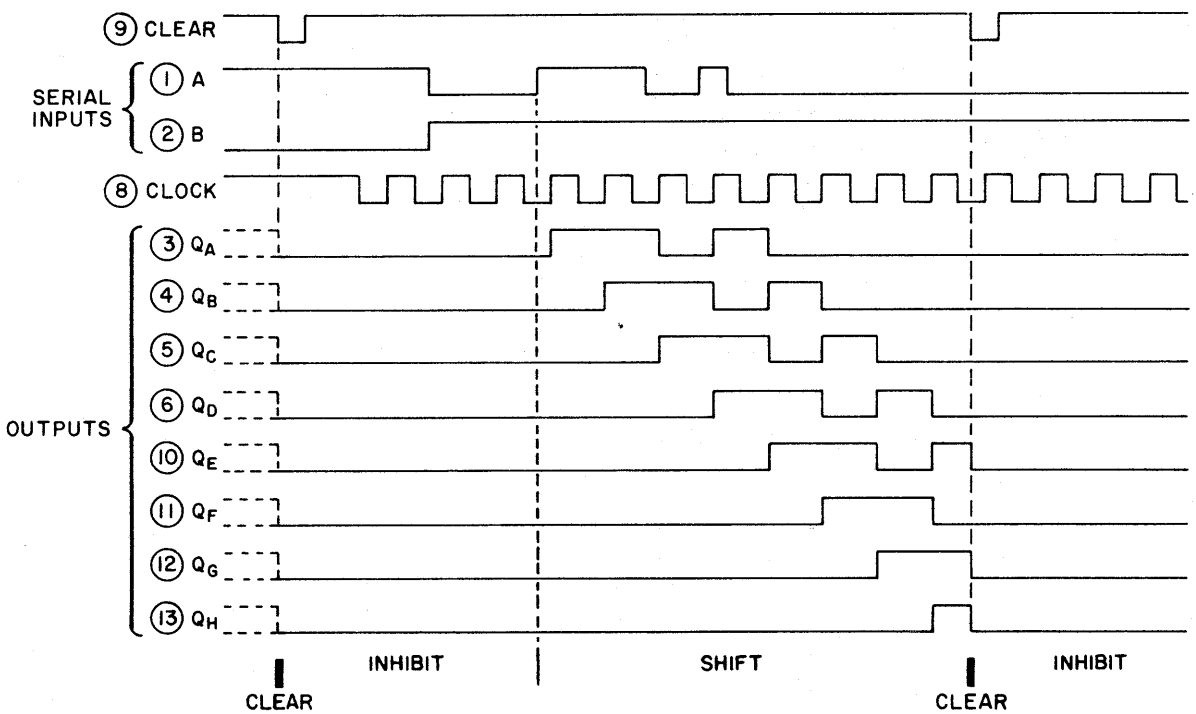


LOGIC SYMBOL

NOTES:

1. Vendor identification: 74164,8570
2. Package pin configuration.

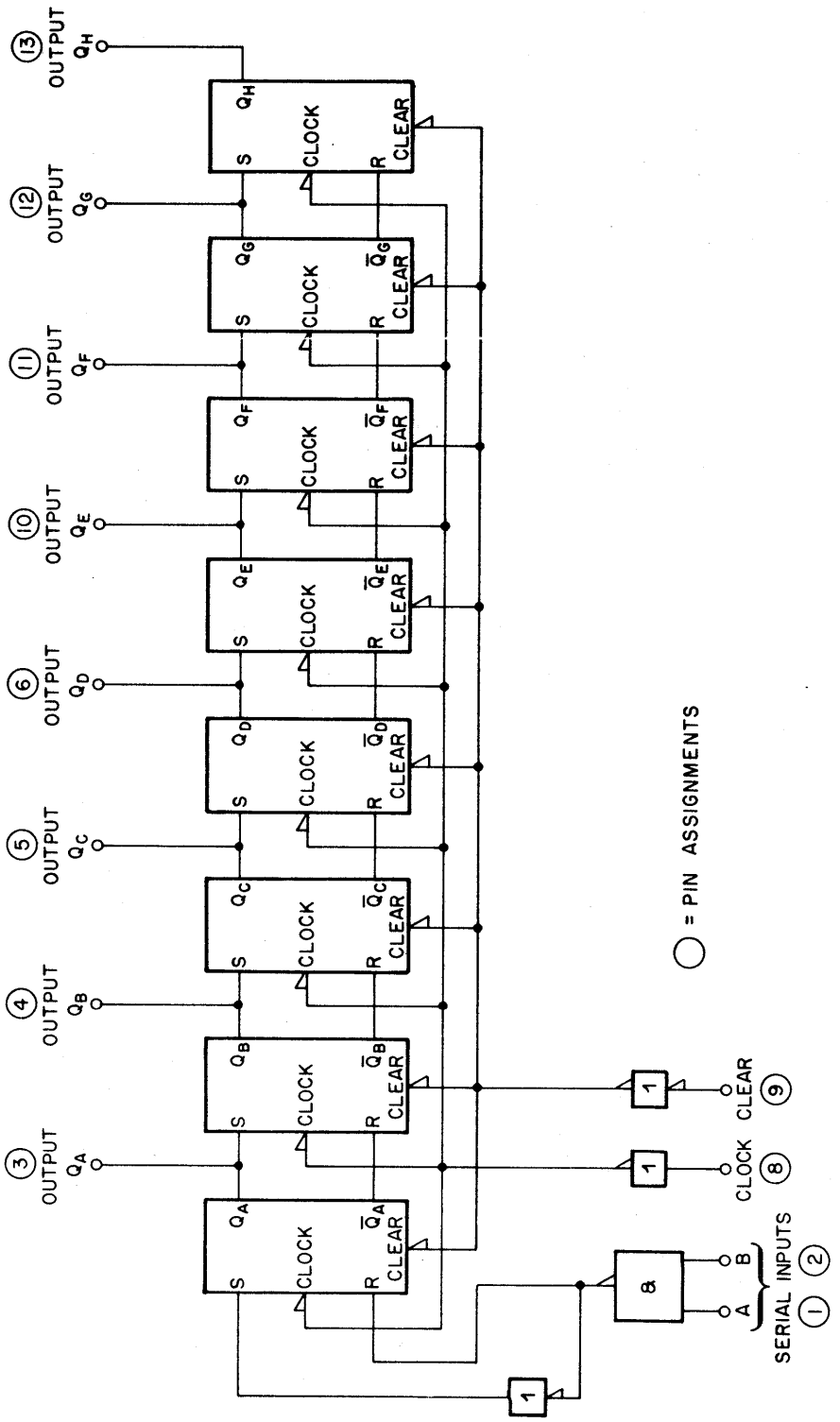




NOTES: 1. TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES.
2. ◯ = PIN ASSIGNMENTS.

FUNCTION SEQUENCE

527
Rev J
Sheet 1 of 2



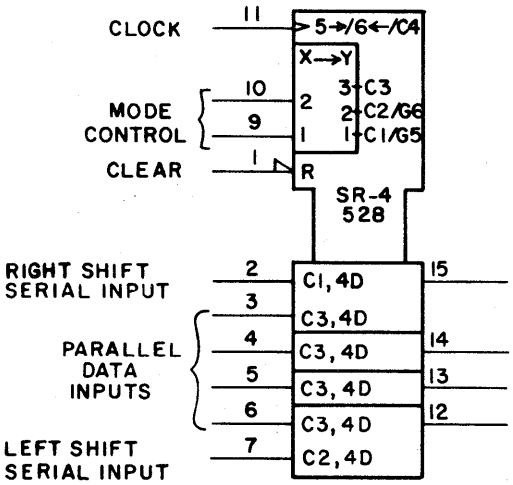
527
Rev J
Sheet 2 of 2

DESCRIPTION

The 528 is a bidirectional shift register that has 4 distinct modes of operation.

	Mode Control	
	Pin 10	Pin 9
Parallel (Broadside) Load (Pins 2-7)	H	H
Shift Right (Pin 15 Towards Pin 12)	L	H
Shift Left (Pin 12 Towards Pin 15)	H	L
Inhibit Clock (Do nothing)	L	L

In the parallel load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when pin 9 is high and pin 10 is low. Serial data for this mode is entered at the shift right data input. When pin 9 is low and pin 10 is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking (and hence data entry) is inhibited when both mode control inputs are low. The mode controls should be changed only when the clock is high.



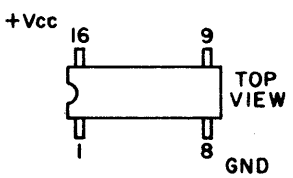
LOGIC SYMBOL

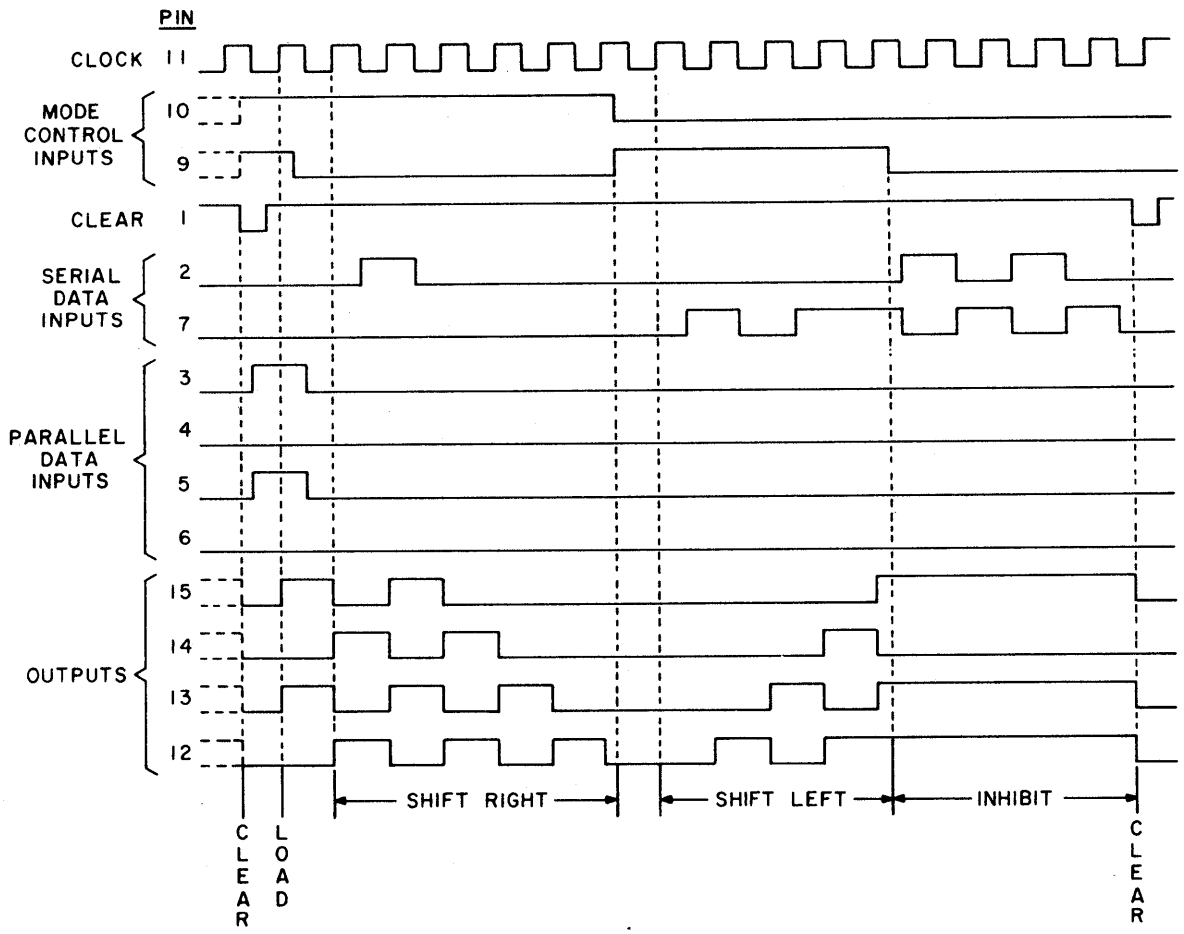
NOTES:

1. Vendor identification:

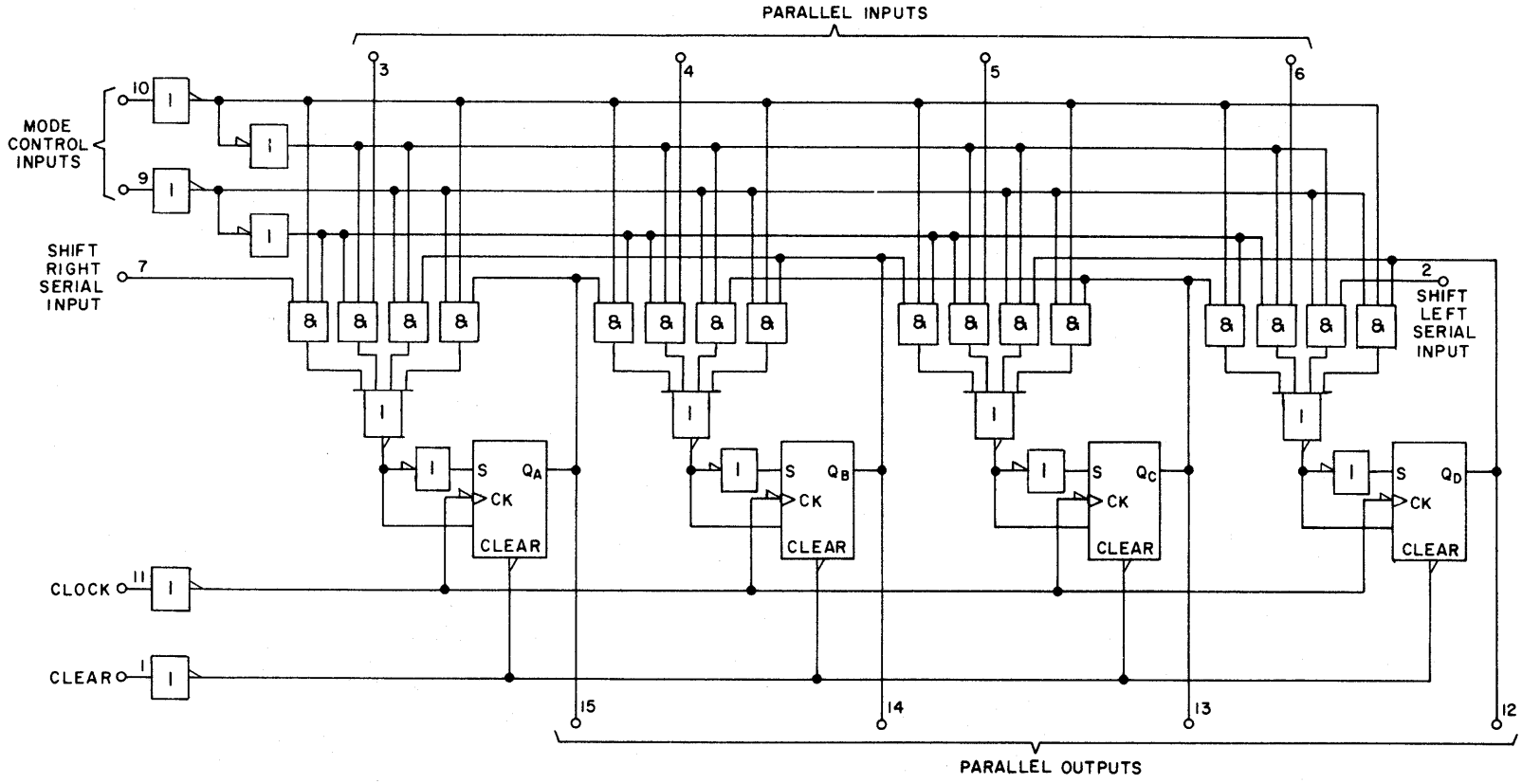
Element	Vendor Number
528	74194
528S	74S194

2. Package pin configuration.





TYPICAL CLEAR, LOAD, SHIFT RIGHT, SHIFT LEFT, INHIBIT AND CLEAR SEQUENCES



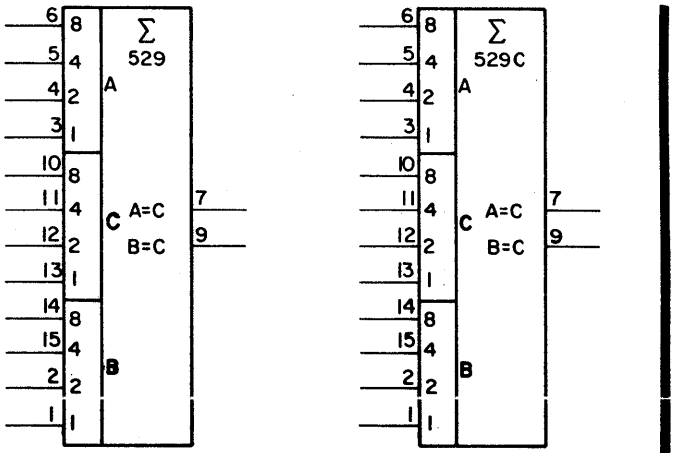
FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION

Element 529 simultaneously and independently compares two 4-bit inputs, A and B, against a 4-bit reference input, C.

Output pin 7 (A=C) will go high when all four A inputs equal the respective reference inputs; output pin 9 (B=C) will go high when all four B inputs equal the respective reference inputs.

Element 529C is logically similar, but provides open-collector outputs that require external pull-up resistors to attain the high-active state.



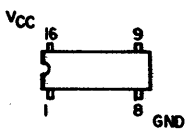
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
529	MC 4022
529C	MC 4021

2. Package pin configuration:



NOTE

The MC 4021 and MC 4022 are unique to this vendor (Motorola). The 4021 and 4022 (no MC prefix) are CMOS circuits and may be found elsewhere in this manual. Motorola identifies these CMOS circuits as MC 14021 and MC 14022, which we have shortened to 4021 and 4022 in keeping with the numbers given them by other vendors.

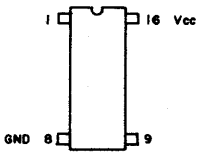
529
REV L
Sheet 1 of 1

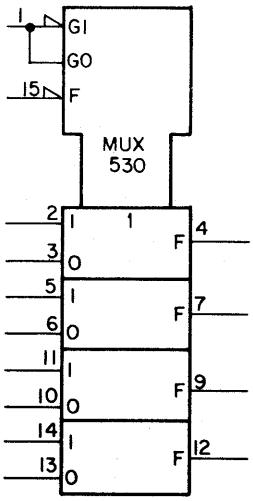
DESCRIPTION

Element 530 is a quad 2-input multiplexer with three-state outputs. The input select and strobe (output enable) lines are common to all four sections. A high on the strobe input (F) puts all outputs in the Hi-Z state, regardless of the state of the select (G) or data inputs.

NOTES

1. Vendor identification: 8123
2. Package pin configuration:





LOGIC SYMBOL

INPUTS				OUT-PUT
CONTROL		DATA		
F	G	0	I	F
H	X	X	X	HI-Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

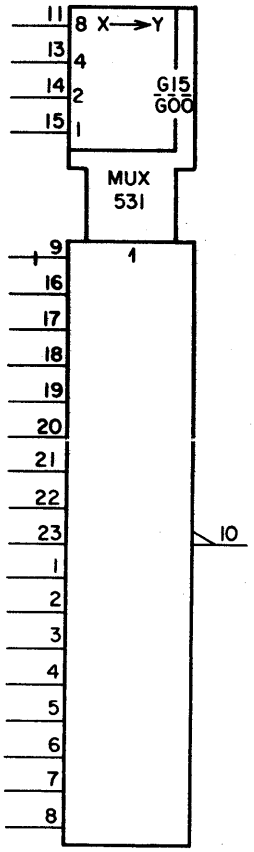
TRUTH TABLE

530
Rev M
Sheet 1 of 1

DESCRIPTION

The type 531 is a 16-bit multiplexer. It selects one of sixteen data sources. The output is determined by the encoded BCD gating on pins 11, 13, 14, and 15. The output is inverted from the input. The multiplexer is inhibited by a logic high on pin 9.

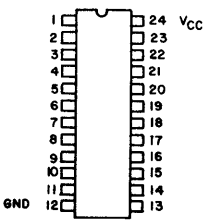
INPUT PINS																				OUTPUT PIN
GATING				I	DATA INPUTS															
11	13	14	15	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	10
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L



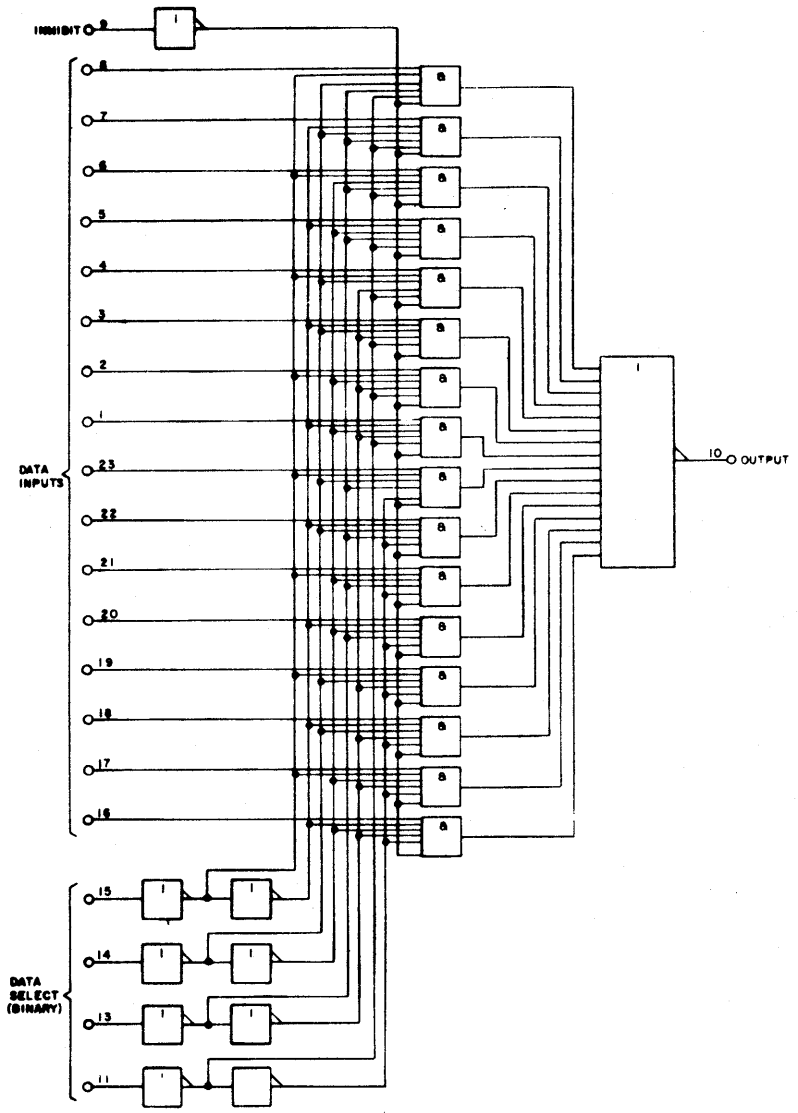
LOGIC SYMBOL

NOTES:

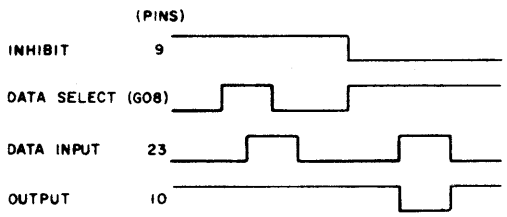
1. Vendor identification: 74150
2. Package pin configuration:



531
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM



TIMING DIAGRAM

531
Rev J
Sheet 2 of 2

DESCRIPTION

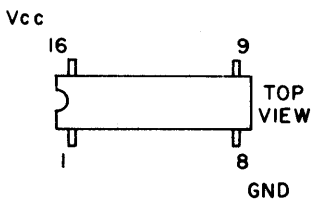
The 532 circuit is a priority encoder that accepts eight active-low inputs and produces a binary weighted output code reflecting the highest-order input. A weight is assigned to each active-low input so that when two or more inputs are simultaneously active, only the input with the highest weight is represented on the output. Weight priorities are in descending order with input 7 having the highest weight. An active-low input enable (pin 5) and an active-low output enable (pin 15) are provided to expand priority encoding to more inputs.

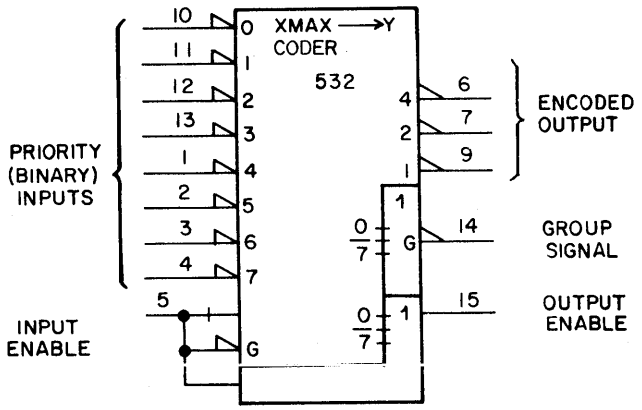
A group signal output (pin 14) will be low if any input is low. This active-low output differentiates between a case where there is no active input and the case where only the lowest-priority input (pin 10) is active, since both of these cases cause the three encoded output pins to go high.

Pin 15 is low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both pin 15 and pin 14 are inactive (high) when the input enable is high.

NOTES:

1. Vendor identification: 9318
2. Package pin configuration.





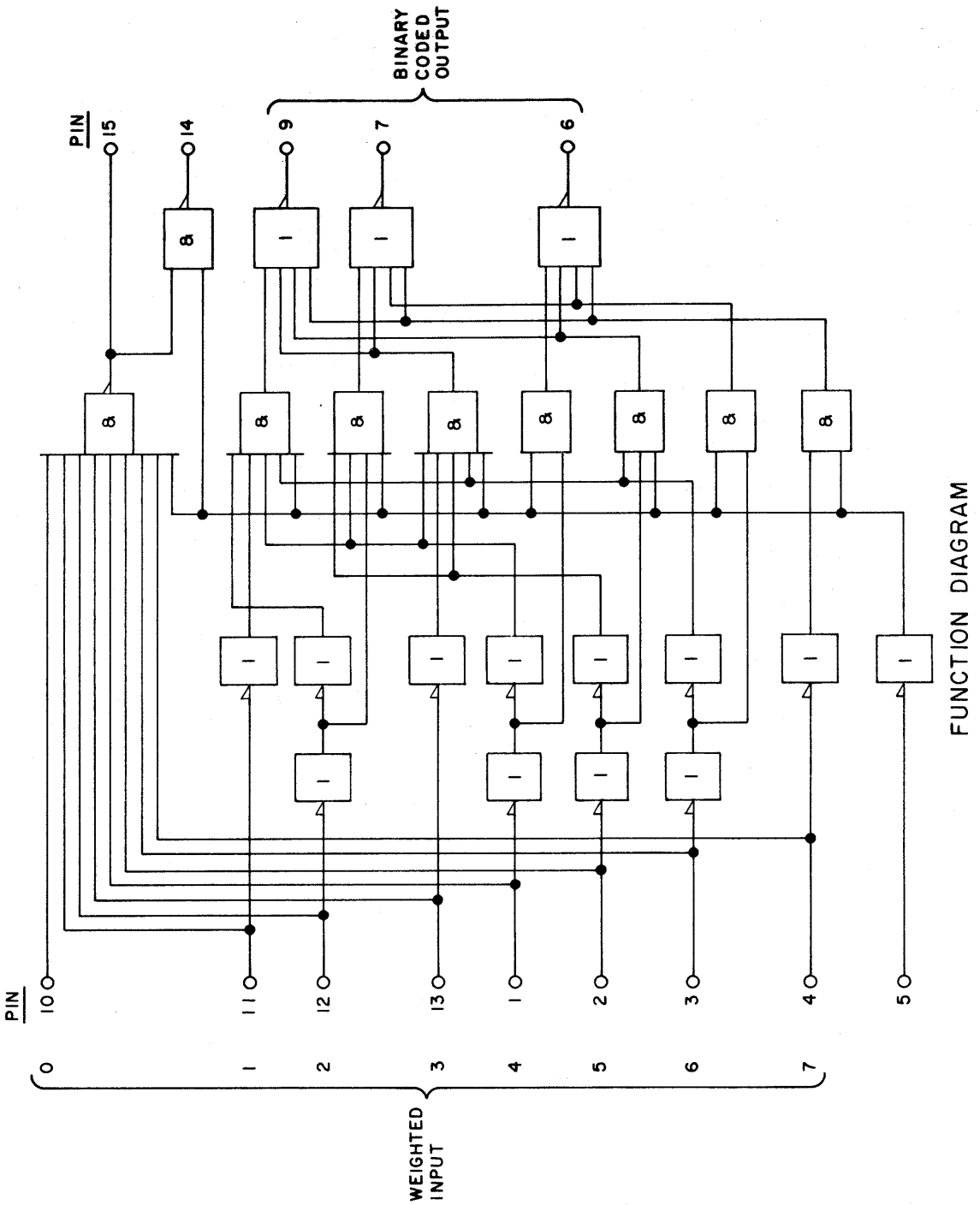
LOGIC SYMBOL

INPUT									OUTPUT				
5	10	11	12	13	1	2	3	4	14	9	7	6	15
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = EITHER HIGH OR LOW VOLTAGE LEVEL

TRUTH TABLE

532
Rev J
Sheet 1 of 2



532
Rev J
Sheet 2 of 2

DESCRIPTION

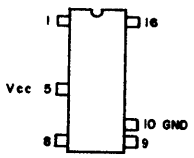
The 537 circuit is a binary counter capable of either 4-bit or 3-bit operation. (See functional diagram and truth tables on sheet 2.) As a 4-bit counter, pin 12 is connected to pin 1, and pin 14 is used as the count-pulse input. For 3-bit operation, pins 12 and 14 are not used, the count pulse being brought in on pin 1.

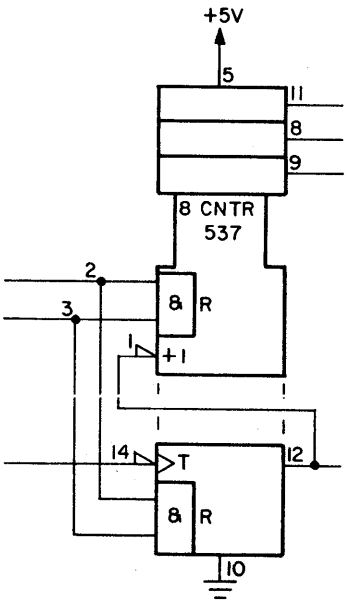
The count advances on the negative-going edge of the input pulse,,provided that the counter is enabled by a low level or either of the Reset inputs, pins 2 and 3.

During 3-bit operation, the toggle-input FF may be used independently, provided that its Reset function coincides with that of the octal counter.

NOTES:

1. Vendor identification: 7493
2. Package pin configuration:



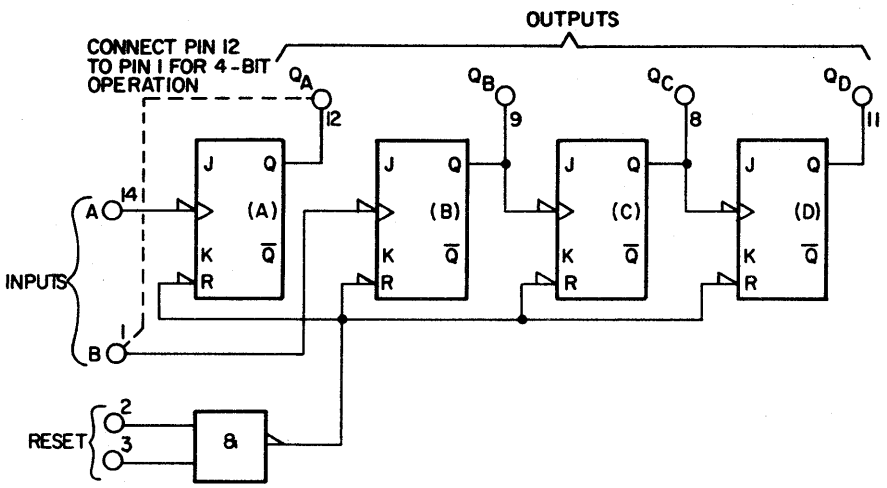


LOGIC SYMBOL

NOTE

If the toggle-input FF is used independently, the Element Identifier is repeated within the FF symbol.

537
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

4-BIT OPERATION, INPUT A
(CONNECT Q_A TO INPUT B)

COUNT	OUTPUTS		
	Q_D	Q_C	Q_B
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

3-BIT OPERATION, INPUT B
(INPUT A AND OUTPUT Q_A UNUSED)

TRUTH TABLES

DESCRIPTION

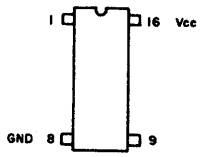
Element 538 is a dual 1-of-4 decoder with low-active outputs.

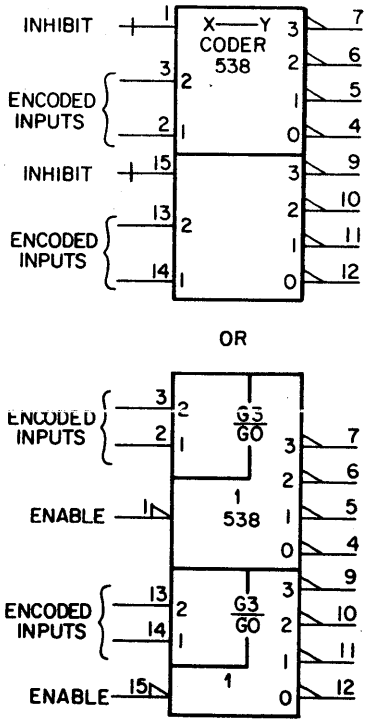
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
538	9321
538S	74S139
538LS	74LS139

3. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUTS			
INH/ ENA	1	2	0	1	2	3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

TRUTH TABLE

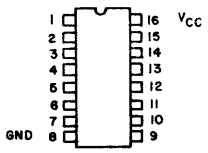
538
Rev J
Sheet 1 of 1

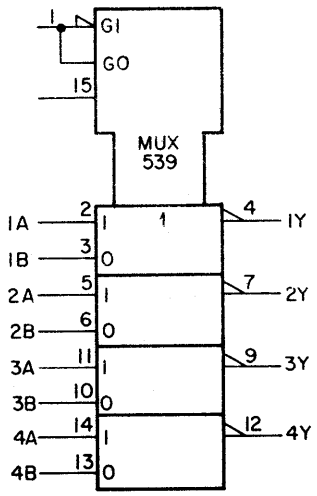
DESCRIPTION

The 539S circuit is a quad, 2-to-1 selector/ multiplexer with inverting outputs that act in accordance with the truth table at the right.

NOTES:

1. Vendor identification: 74S158
2. Package pin configuration:



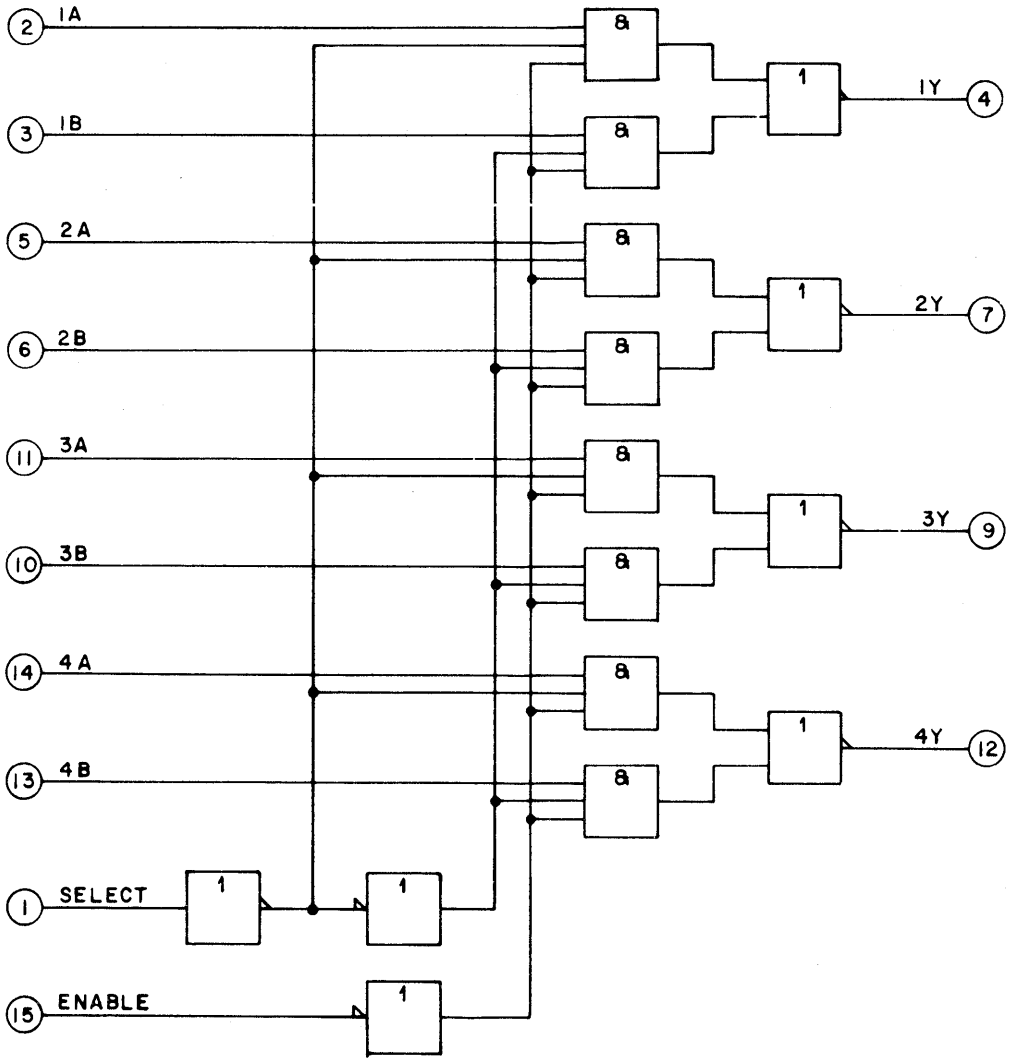


LOGIC SYMBOL

INPUTS				OUTPUT
ENABLE	SELECT	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

TRUTH TABLE

539
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

539
Rev J
Sheet 2 of 2

DESCRIPTION

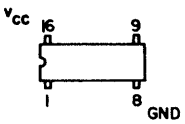
The 542 circuit is a three-state, dual 4-to-1 multiplexer. The two binary select inputs are common to both sections. A separate strobe line for each section holds the output of that section in the Hi-Z state when the strobe input is high.

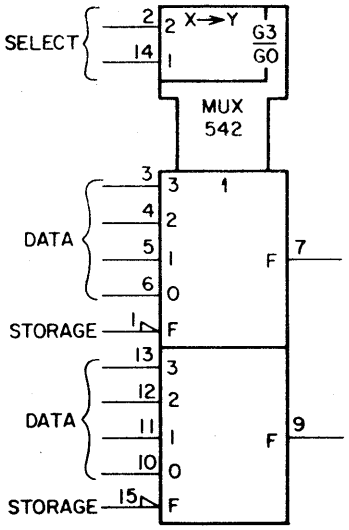
The three-state feature allows the outputs from as many as 128 sections to be connected, providing a 512-line-to-1-line multiplexing function. Appropriate control of the select and strobe inputs then converts the data from parallel-in to serial-out.

Figure 1 shows two 542 ICs connected in this manner to serialize 16 data input bits.

NOTES:

1. Vendor identification: DM8214
2. Package pin configuration:





LOGIC SYMBOL

INPUTS							OUTPUT
DATA				SELECT		STROBE	
0	1	2	3	2	1	F	
X	X	X	X	X	X	H	HI-Z
0	X	X	X	0	0	L	0
1	X	X	X	0	0	L	1
X	0	X	X	0	1	L	0
X	1	X	X	0	1	L	1
X	X	0	X	1	0	L	0
X	X	1	X	1	0	L	1
X	X	X	0	1	1	L	0
X	X	X	1	1	1	L	1

TRUTH TABLE
(ONE SECTION)

542
Rev M
Sheet 1 of 2

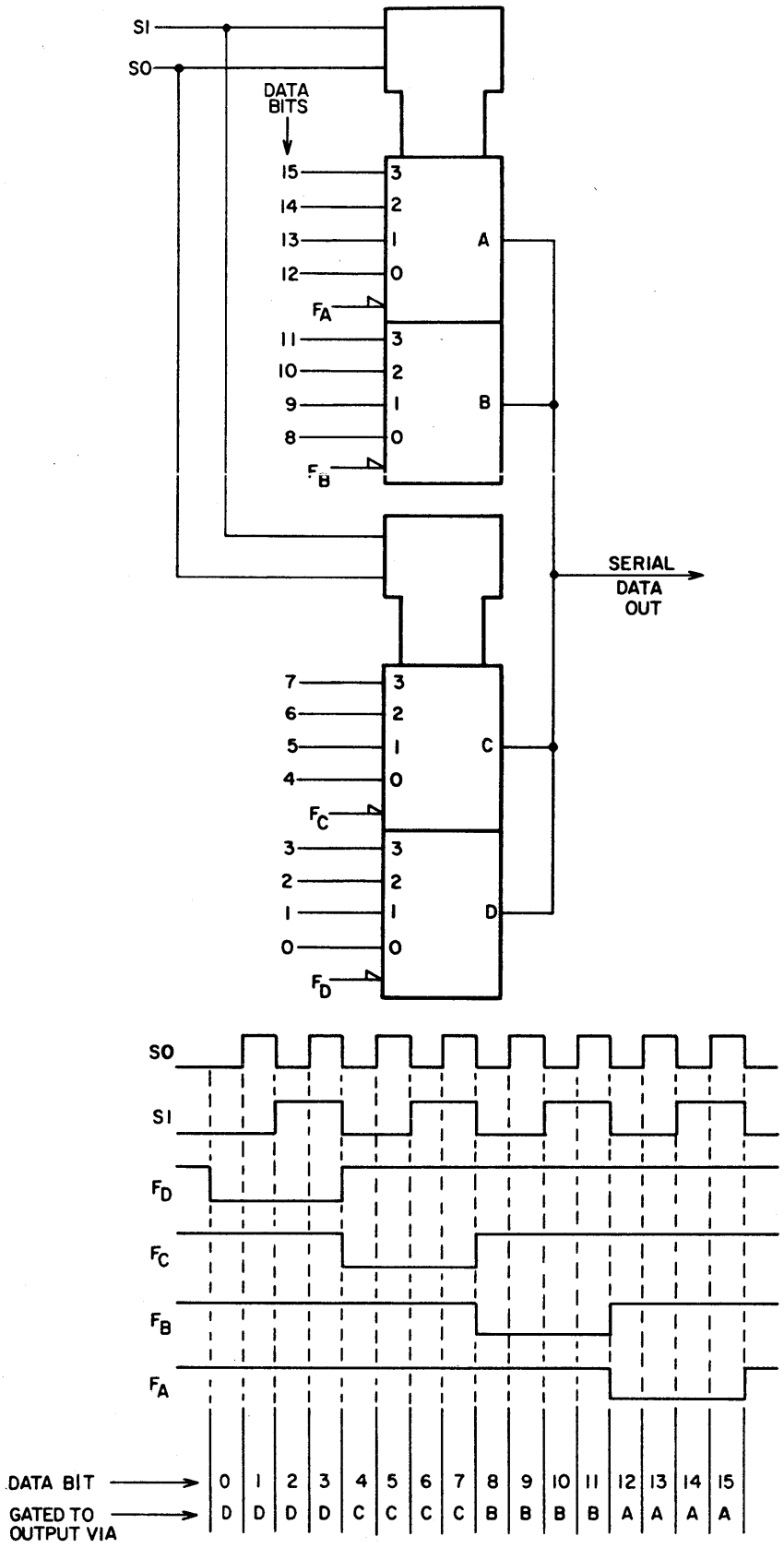


Figure 1 Serializing 16 Data Bits

542
Rev J
Sheet 2 of 2

DESCRIPTION

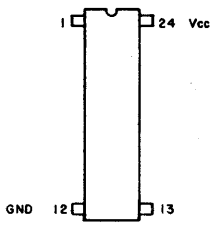
Element 543 is an 8-bit parallel/serial-in, parallel-out shift register. Loading and shifting is accomplished on the positive-going edge of the clock pusse, provided that the clock enable input is held low. Neither loading nor shifting is possible when the clock enable input is high.

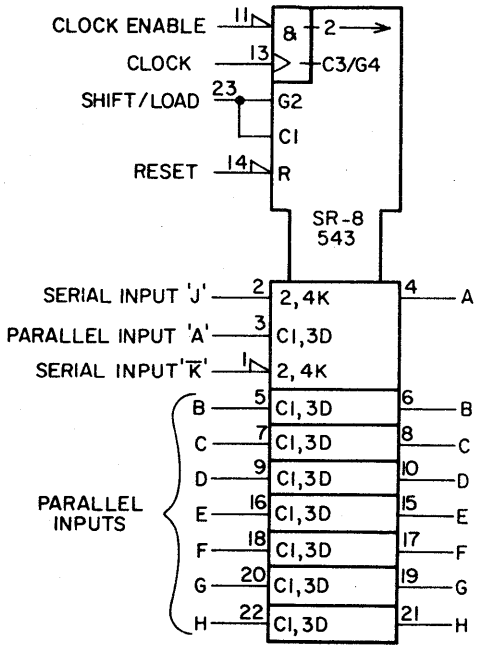
For shifting, the shift/load input must be high. During shifting, serial data is entered at the J-$\overline{K}$ inputs. See the J-$\overline{K}$ truth table for states needed to enter data into the first FF stage.

For parallel loading, the shift/load input must be low. Serial data flow is inhibited during loading.

NOTES:

1. Vendor identification: 74199
2. Package pin configuration:





LOGIC SYMBOL

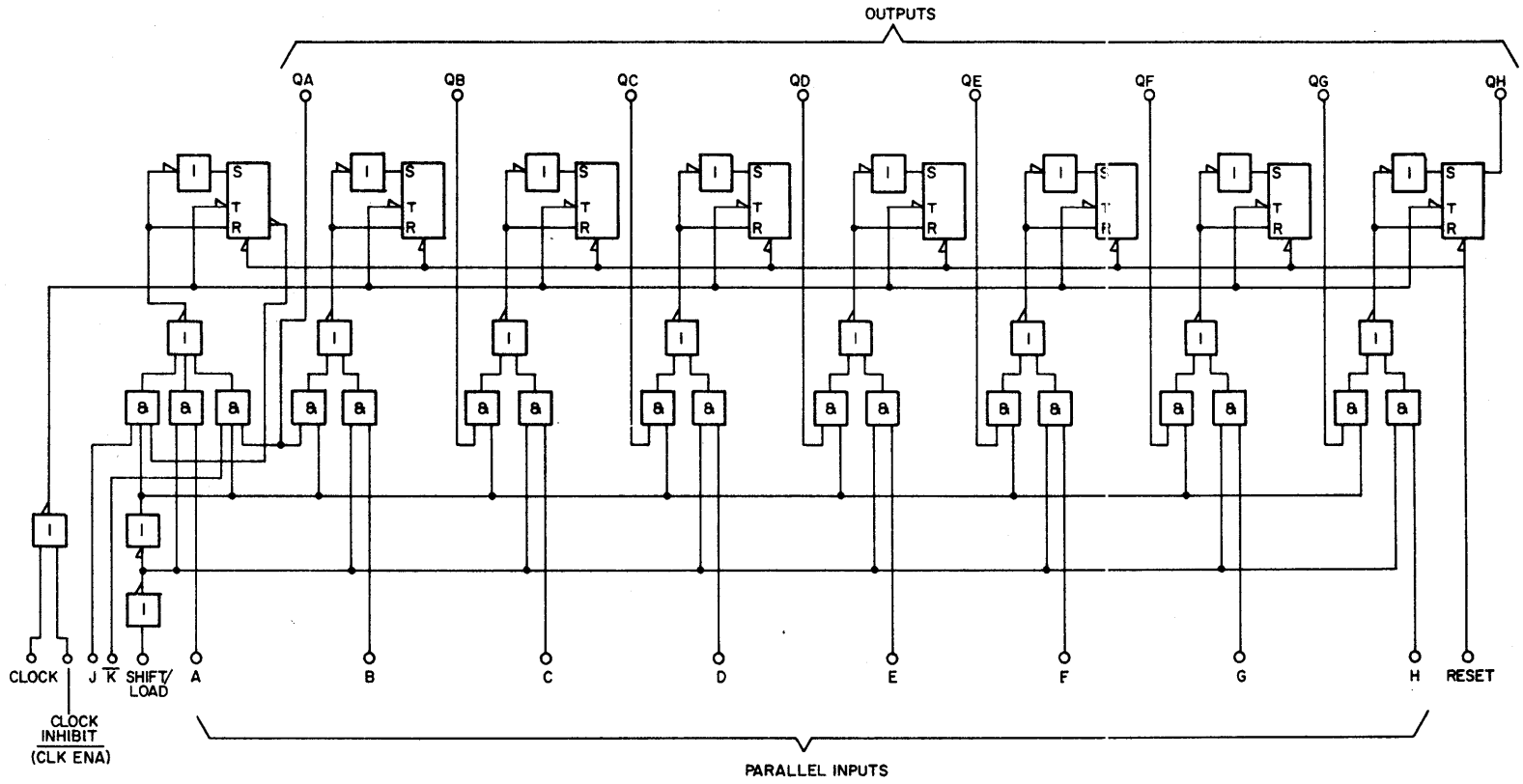
INPUTS AT tn		OUTPUT AT tn + 1
J	$\overline{K}$	QA
L	H	QAn
L	L	L
H	H	H
H	L	$\overline{QA}$n

tn = BIT TIME BEFORE CLOCK PULSE

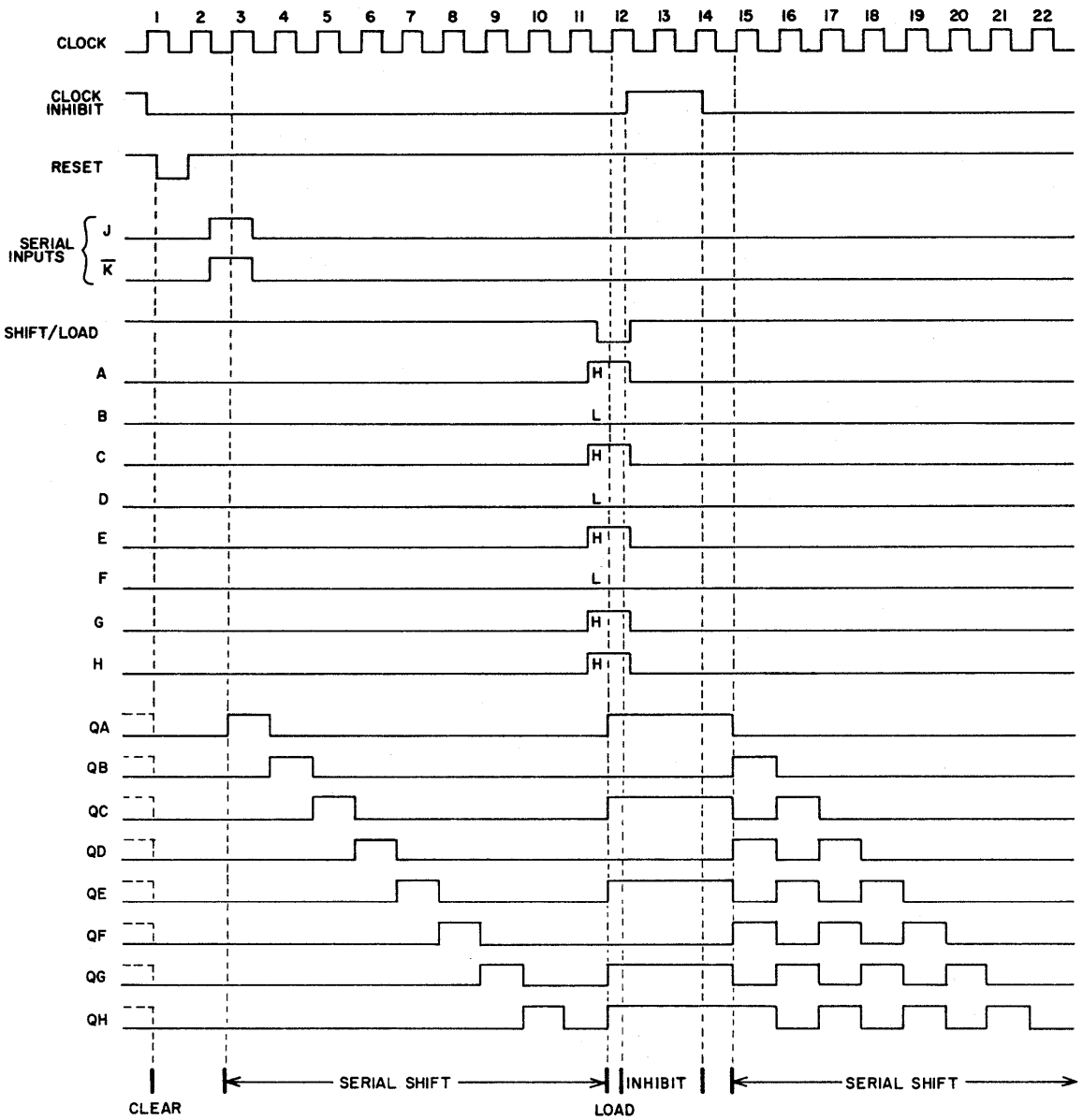
tn+1 = BIT TIME AFTER CLOCK PULSE

J-$\overline{K}$ TRUTH TABLE

543
Rev J
Sheet 1 of 3



FUNCTIONAL DIAGRAM



TIMING DIAGRAM

543
Rev J
Sheet 3 of 3

DESCRIPTION

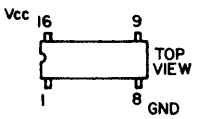
Element 544 is a quad latch featuring low-active inputs.

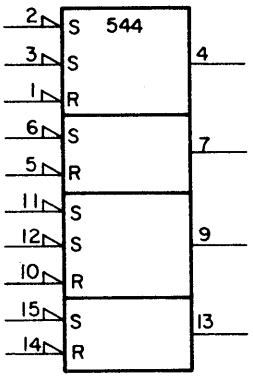
NOTES:

1. Sections may appear separately.
2. Vendor identification:

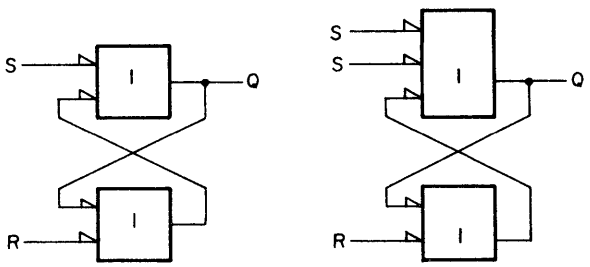
Element	Vendor Number
544	74279
544LS	74LS279

3. Package pin configuration.





LOGIC SYMBOL



FUNCTIONAL DIAGRAM

TRUTH TABLE
(EACH LATCH)

INPUTS		OUTPUT
$S_{①}$	R	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H②

Q_0 = level of Q before indicated input conditions were established.

① for latches with double S inputs:
H = both S inputs high
L = one or both S inputs low.

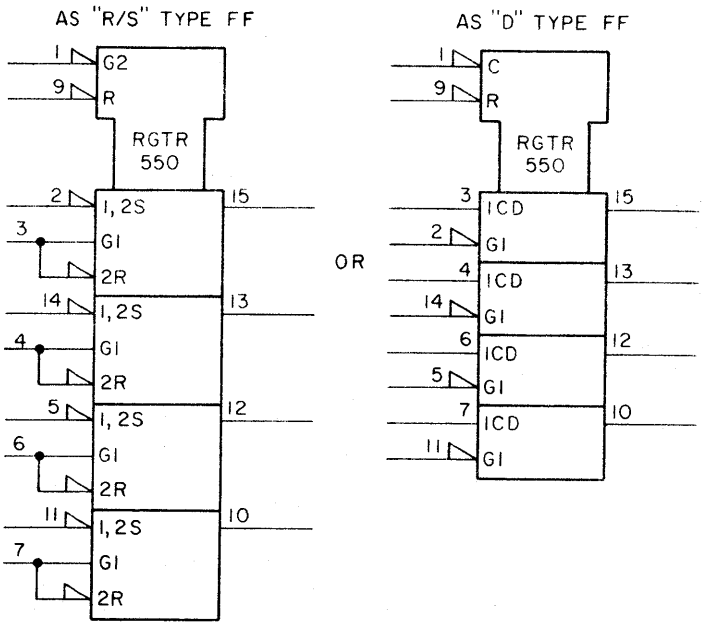
② this output level may not persist when S and R inputs return to their inactive (high) state.

544
Rev J
Sheet 1 of 1

DESCRIPTION

The 550 circuit is a 4-bit latch. It can be used as single input D latches or set/reset latches. The four latches have a common active low enable and an active low master reset. When the common enable goes high, data present in the latches is stored and the state of a latch is no longer affected by the not S and D inputs. The master reset, when activated, overrides all other input conditions forcing all latch outputs low.

Each of the four latches can be operated in one of two modes: D-type latch or set/reset latch. For D-type operation the not S input of a latch is held low. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes high. During set/reset operation, when the common enable is low, a latch is reset by a low on the D input, and can be set by a low on the not S input if the D input is high. If both not S and D inputs are low, the D input will dominate and the latch will be reset. When the enable goes high, the latch remains in the last state prior to the low to high transition.



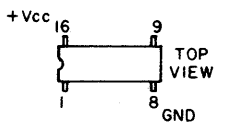
LOGIC SYMBOL

NOTES:

1. Vendor identifications:

Element	Vendor Number
550	9314

2. Package pin configuration.

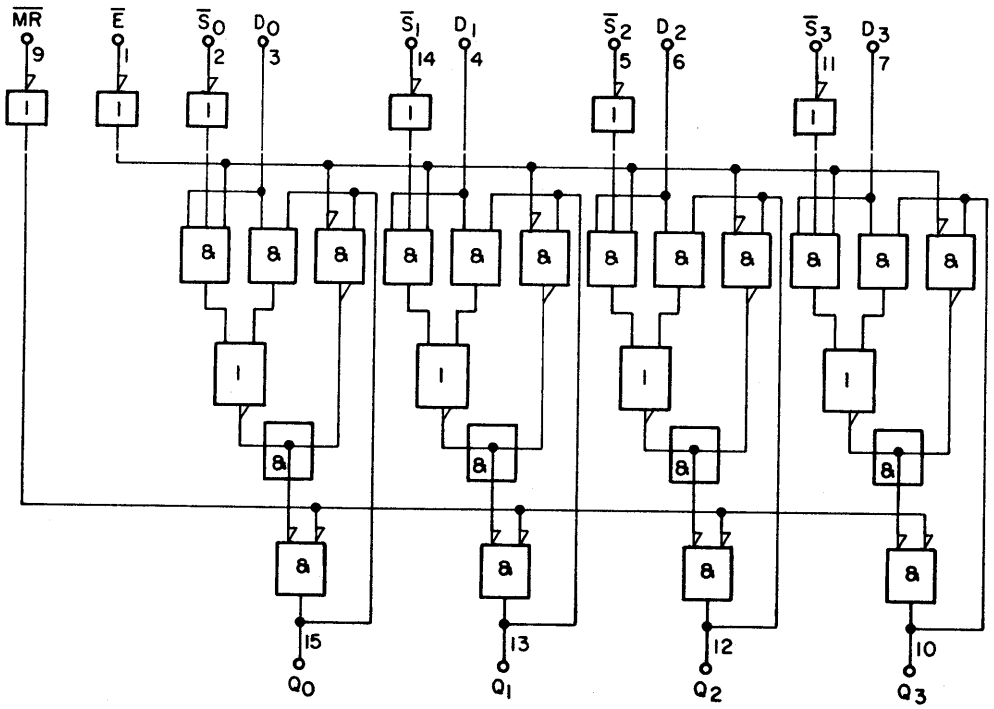


$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

X = DON'T CARE
L = LOW VOLTAGE LEVEL
H = HIGH VOLTAGE LEVEL
Q_{N-1} = PREVIOUS OUTPUT STATE
Q_N = PRESENT OUTPUT STATE

TRUTH TABLE

550
Rev J
Sheet 1 of 2



FUNCTION DIAGRAM

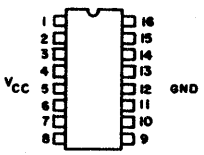
550
Rev J
Sheet 2 of 2

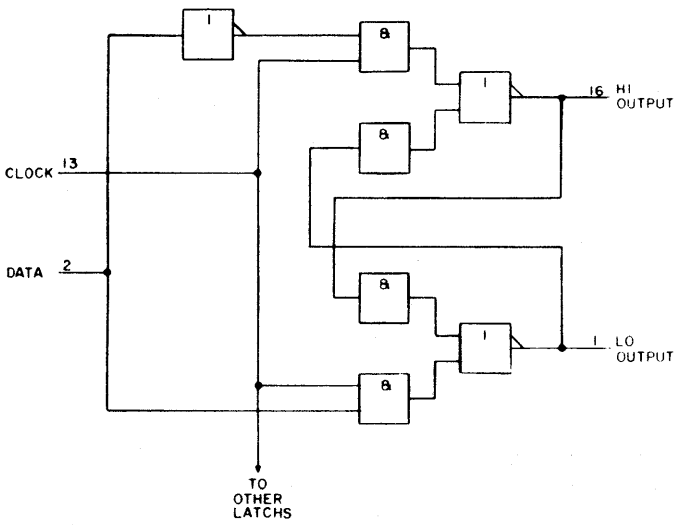
DESCRIPTION

The 551 latch may be used as a temporary storage device for binary information. Information present at a data (D) input is transferred to the high output when the clock is high. The high output follows the data input as long as the clock remains high. When the clock goes low, the information that was present at the data input at the time the transition occurred is retained at the high output until the clock goes high. The latch has complementary high and low outputs.

NOTES:

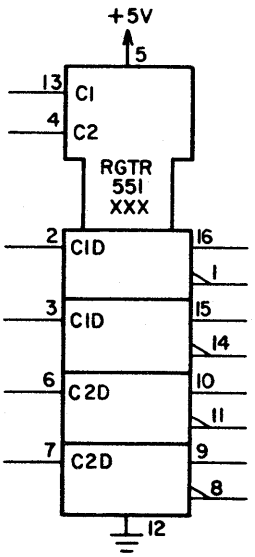
1. Vendor identification: 7475
2. Package pin configuration:





NOTE: LOGIC DIAGRAM FOR ONE LATCH ONLY

FUNCTIONAL DIAGRAM



LOGIC SYMBOL

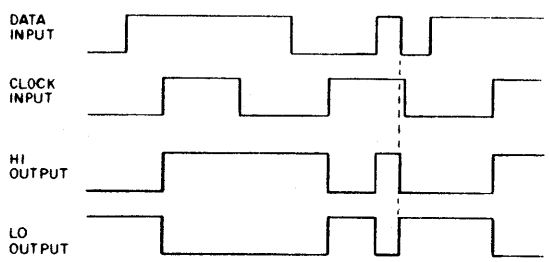
EACH LATCH

Tn	Tn + 1
DATA	HI OUTPUT
H	H
L	L

Tn = BIT TIME BEFORE NEGATIVE-GOING TRANSITION OF CLOCK

Tn + 1 = BIT TIME AFTER NEGATIVE-GOING TRANSITION OF CLOCK

TRUTH TABLE



TIMING DIAGRAM

551
Rev J
Sheet 1 of 1

DESCRIPTION:

TTL element 552 is an 8-bit addressable latch with four modes of operation, governed by inputs E (pin 14) and C (pin 15), as shown in the Mode Selection table:

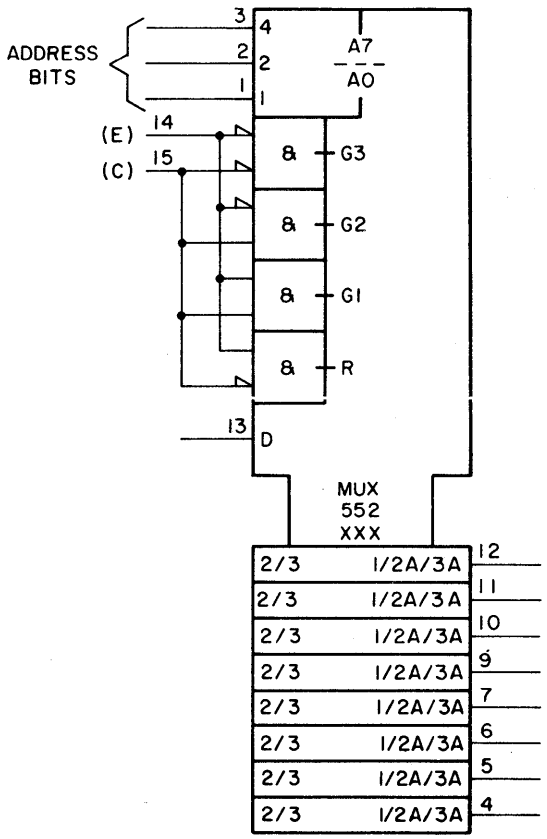
1. In the Memory mode, neither the address bits nor the data input have any effect. The existing state of each latch is available at the latch outputs.

2. In the Addressable Latch mode, the addressed output will follow the Data input (pin 13). All other outputs will remain as they were before the selection.

3. In the Demultiplex mode, the addressed output follows the state of the D input as in the Addressable Latch mode, but all other outputs will be low.

4. In the Reset mode, all outputs are low and are unaffected by the address or data inputs.

To avoid output errors in modes G2 and G3, the address and data inputs should be changed only when Mamory mode (G1) is selected.



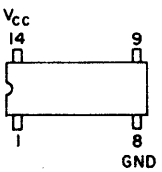
LOGIC SYMBOL

MODE SELECTION

E (Pin 14)	C (Pin 15)	Mode
L	L	Demultiplex (G3)
L	H	Addressable Latch (G2)
H	H	Memory (G1)
H	L	Reset (R)

NOTES:

1. Vendor identification: 9334
2. Package pin configuration:



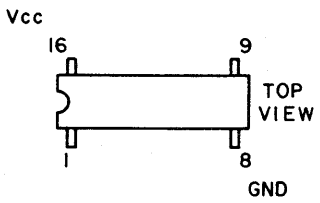
552
Rev. J
Sheet 1 of 1

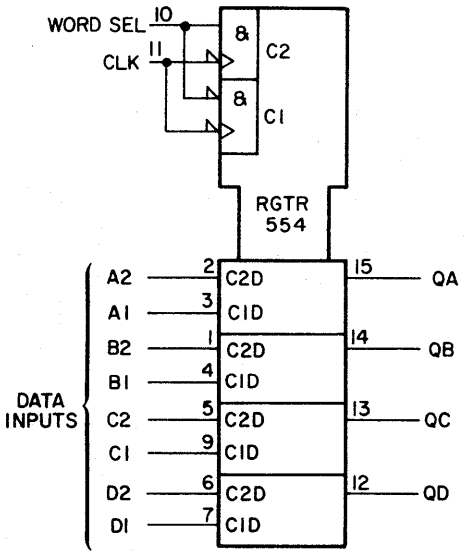
DESCRIPTION

The 554 circuit is a 1-of-2 selector/multiplexer with storage. Data is entered into the R-S flipflops on the negative-going clock transition. Data set-up time is approximately 15 nsec; word select set-up time is approximately 25 nsec. Data gated to the FF outputs by the clock signal remains there until the next clock transition. The FFs are not directly resettable.

NOTES:

1. Vendor Identification: 74298
2. Package pin configuration.





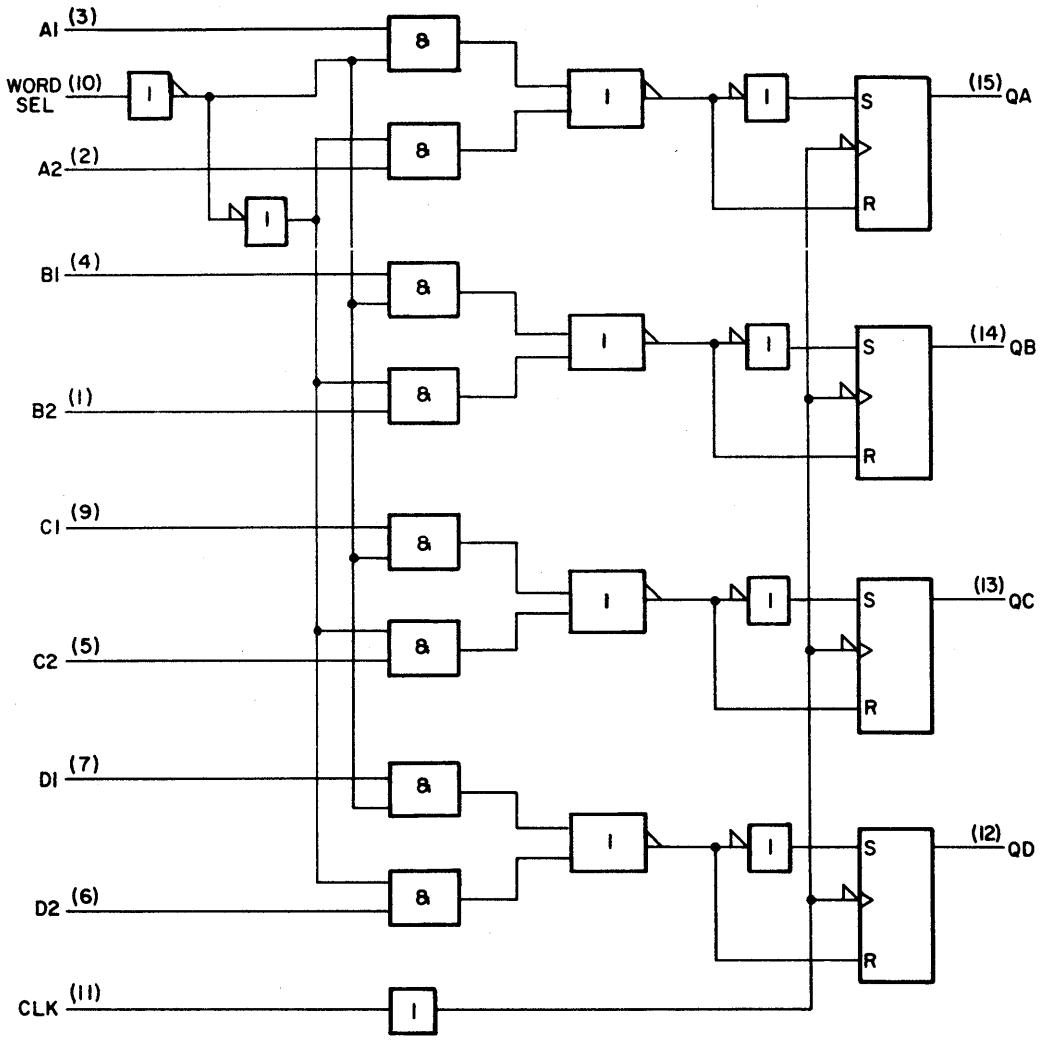
LOGIC SYMBOL

TRUTH TABLE

INPUTS		OUTPUTS			
WD SEL	CLK	QA	QB	QC	QD
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	QA0	QB0	QC0	QD0

L = low level, steady state
H = high level, steady state
↓ = transition from high to low level
X = irrelevant
A1,A2,etc. = steady-state level of data input signal
QA0,QB0,etc. = the level of QA,QB,etc. entered on last high-to-low transition of clock.

554
Rev. J
Sheet 1 of 2



PIN NUMBERS ARE IN PARENTHESES

LOGIC DIAGRAM

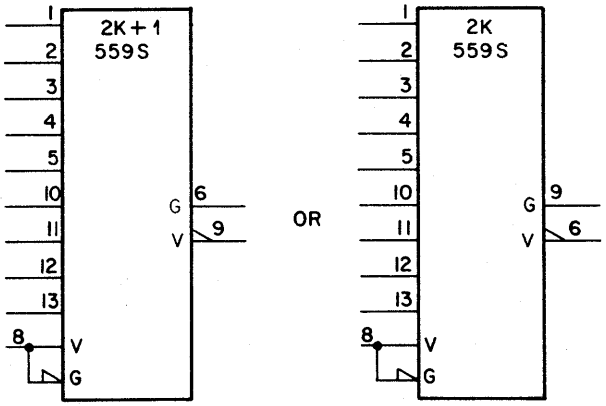
554
Rev. J
Sheet 2 of 2

DESCRIPTION

The 559S circuit is a 9-bit parity generator/ checker. This circuit is commonly used to generate a parity bit (if necessary) which is transmitted along with the associated data word. This circuit can also be used as a parity checker indicating that data has been received correctly or that an error has been detected.

Referring to the functional (logic) diagram, note that if an odd number of inputs are high, the odd output is high (the even output is low). If an even number of inputs are high, the even output is high (the odd output is low).

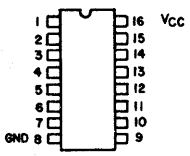
A high on the inhibit input (pin 8) forces both outputs low).

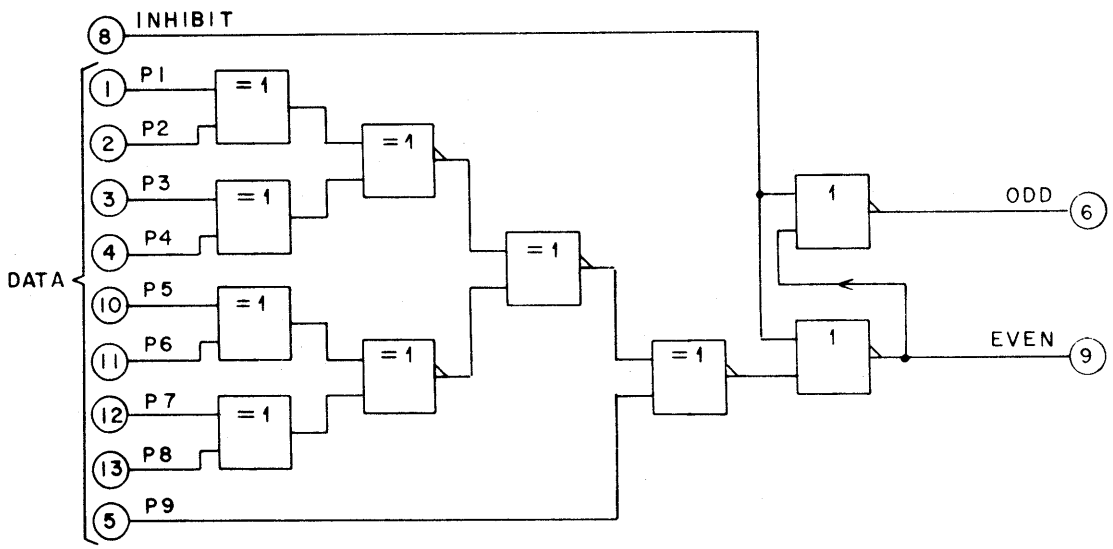


LOGIC SYMBOL

NOTES:

1. Vendor identification: 82S62
2. Package pin configuration:





FUNCTIONAL DIAGRAM

559
Rev J
Sheet 1 of 1

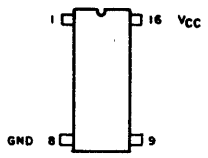
DESCRIPTION

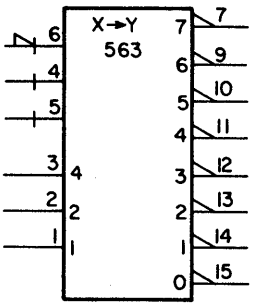
Element 563LS is a 3-to-8-line decoder that also functions as a 1-to-8-line demultiplexer. One active-high and two active-low enable inputs reduce the need for external inverters when cascading for larger words. (See example on sheet 3.)

An enable input can be used as a data input when demultiplexing.

NOTES:

1. Vendor identification: 74LS138
2. Package pin configuration:





LOGIC SYMBOL

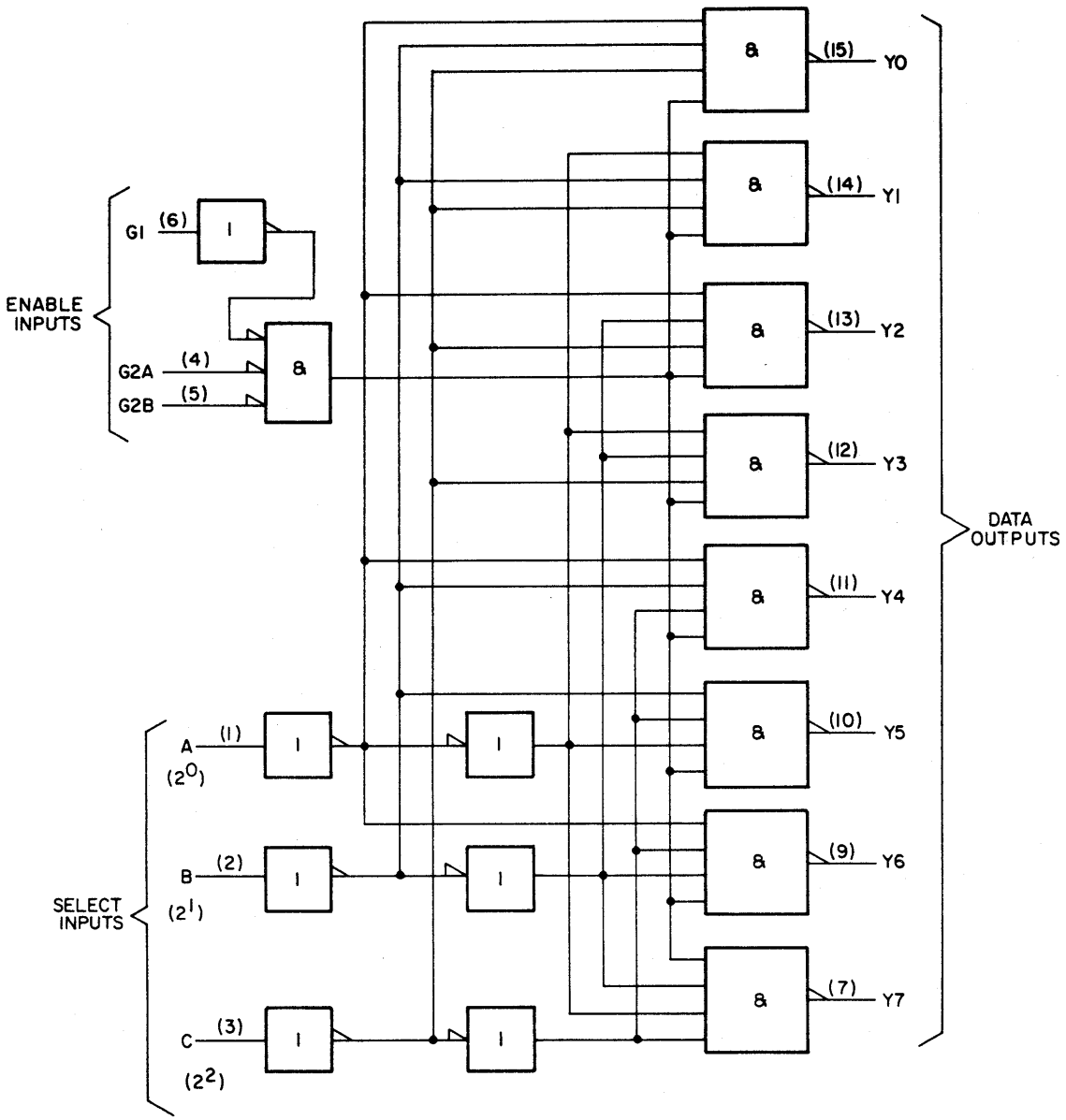
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High, L = Low, X = Irrelevant

* G2 = G2A & G2B

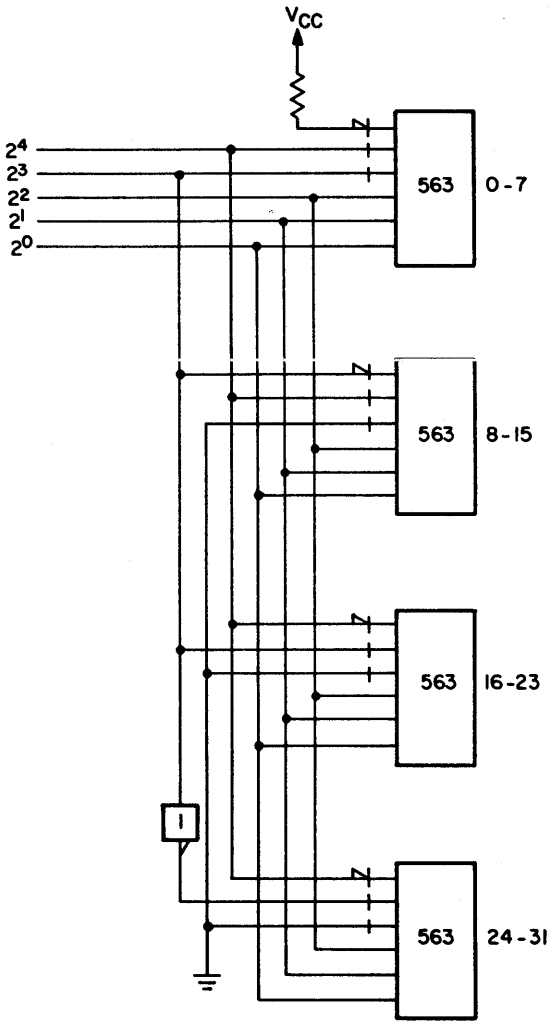
Input/output labels refer to functional diagram on sheet 2.

TRUTH TABLE



FUNCTIONAL DIAGRAM

	"ENABLE" INPUTS				
	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1



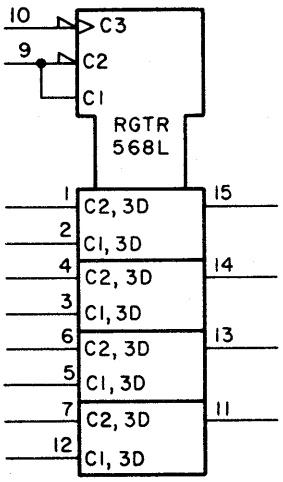
CASCADING FOR 5-TO-32-LINE DECODE

563
Rev J
Sheet 3 of

DESCRIPTION

Element 568L is a 4-bit wide, 2-word data selector with storage properties. If the Word select input (pin 9) is low, Word 1 inputs (C1, 3D) are selected. When pin 9 is high, Word 2 inputs (C2, 3D) are selected.

The selected 4-bit word is stored in four S-R masterslave FFs and passed to the outputs on the negative-going edge of the clock (pin 10). Stored data is then available until the next high-to-low transition of the clock.

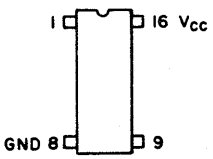


LOGIC SYMBOL

NOTES

1. Vendor identification: 74L98

2. Package pin configuration:



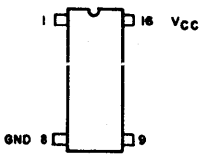
DESCRIPTION

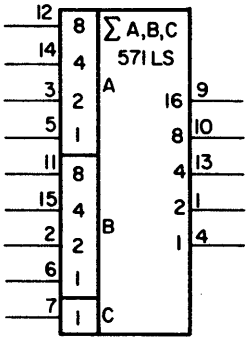
The 571LS circuit is a 4-bit binary full adder, featuring a full look-ahead that generates a fast carry in 10 ns, typically. See sheets 2 and 3 for function table and functional diagram.

NOTES:

1. Vendor identification: 75LS283

2. Package pin configuration:





LOGIC SYMBOL

571
Rev J
Sheet 1 of 3

INPUT				OUTPUT					
				WHEN CO = L			WHEN CO = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ4	Σ2 / Σ8	C2 / C4	Σ1 / Σ4	Σ2 / Σ8	C2 / C4
L	L	L	L	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High, L = Low

C0 = Carry in (pin 7)

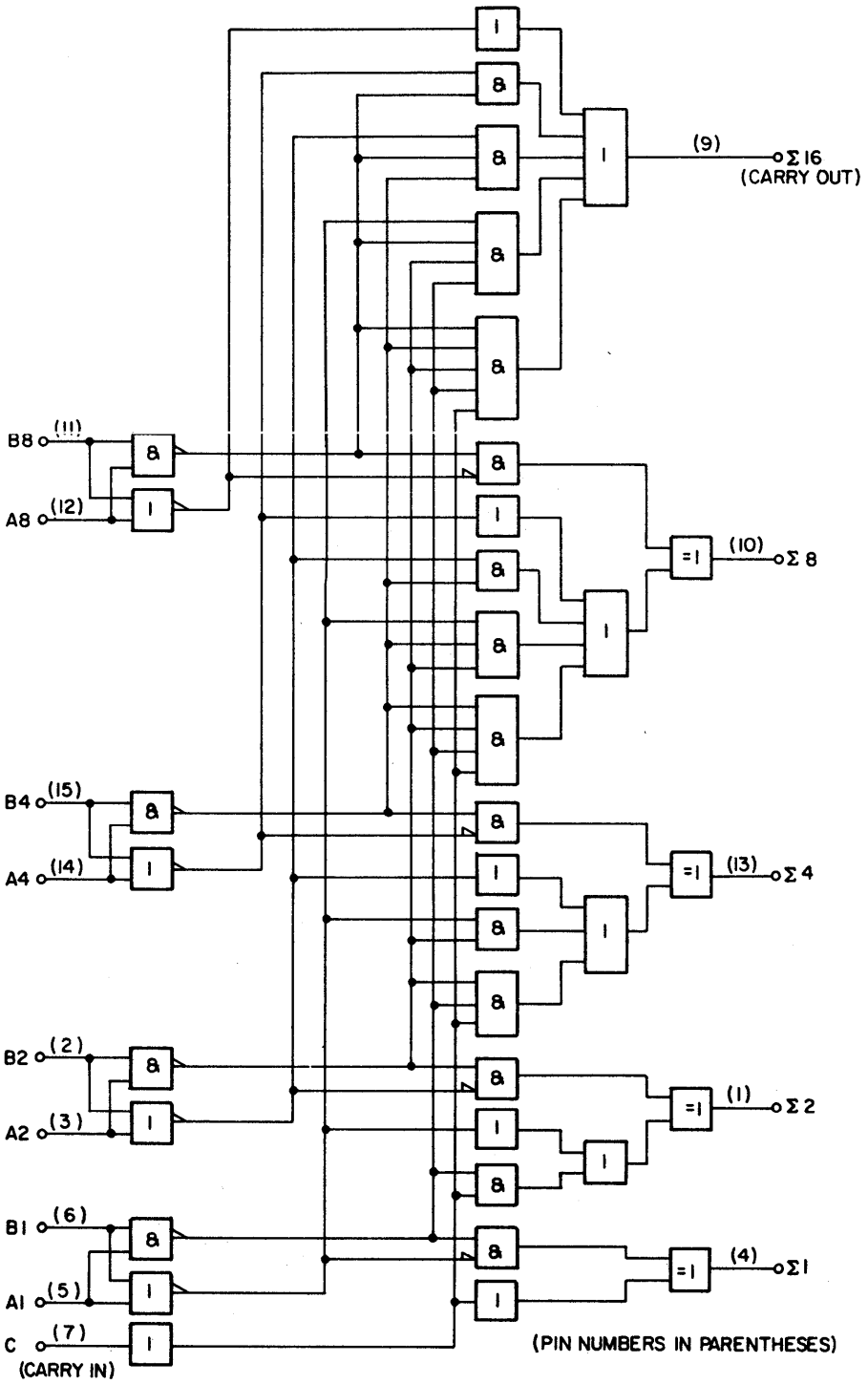
C2 = Internal carry

C4 = Carry out (E16, pin 9)

NOTE

Input conditions at A1, B1, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry, C2. The values at C2, A3, B3, A4 and B4 then determine outputs Σ4, Σ8, and C4 (Σ16).

FUNCTION TABLE



FUNCTIONAL DIAGRAM

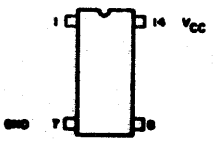
571
Rev J
Sheet 3 of 3

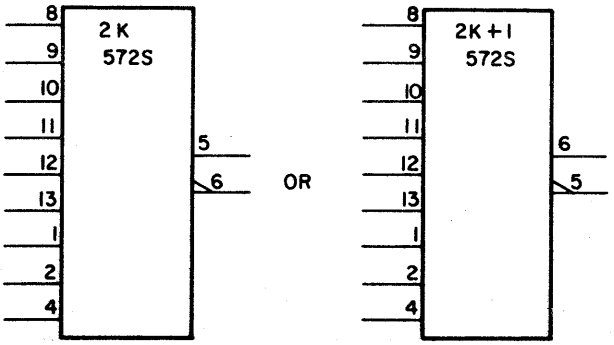
DESCRIPTION

Element 572S is a nine-bit parity generator/ checker. These devices can be cascaded to provide parity for up to 81-bit words in typically 25 ns.

Notes:

1. Vendor identification: 74S280
2. Package pin configuration:





LOGIC SYMBOL

NUMBER OF INPUTS THAT ARE HIGH	OUTPUTS	
	EVEN (5)	ODD (6)
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

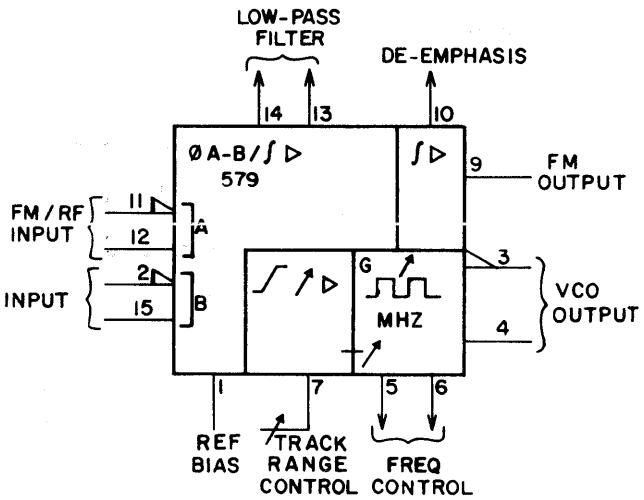
TRUTH TABLE

572
Rev J
Sheet 1 of 1

DESCRIPTION

The 579 phase-locked loop (PLL) is a monolithic signal conditioner and demodulator system. As shown in the block diagram on sheet 2, the PLL comprises a VCO (voltage-controlled oscillator), phase comparator, amplifier and low-pass filter. The center frequency of the PLL is determined by the free-running frequency (fo) of the VCO. This VCO frequency is set by an external capacitor attached to the Frequency Control, pins 5 and 6. The low-pass filter, which determines the capture characteristics of the loop, is formed by an external RC network connecting pins 13 and 14.

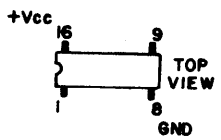
The 579 has two sets of differential inputs, one for the FM/RF input and one for the phase comparator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source (pin 1) is provided to bias the phase comparator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division application. Pin 7 is provided for the optional extension of the tracking range.



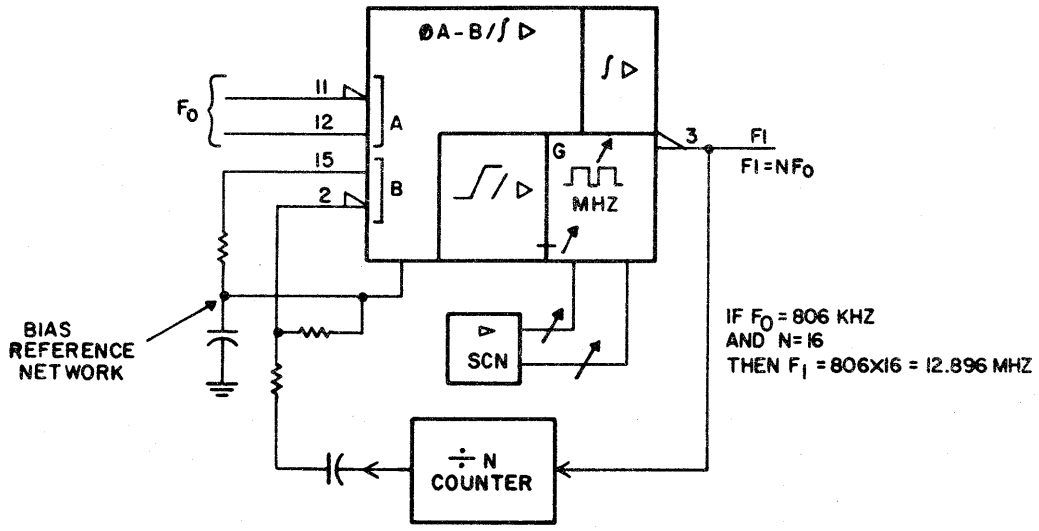
LOGIC SYMBOL

NOTES:

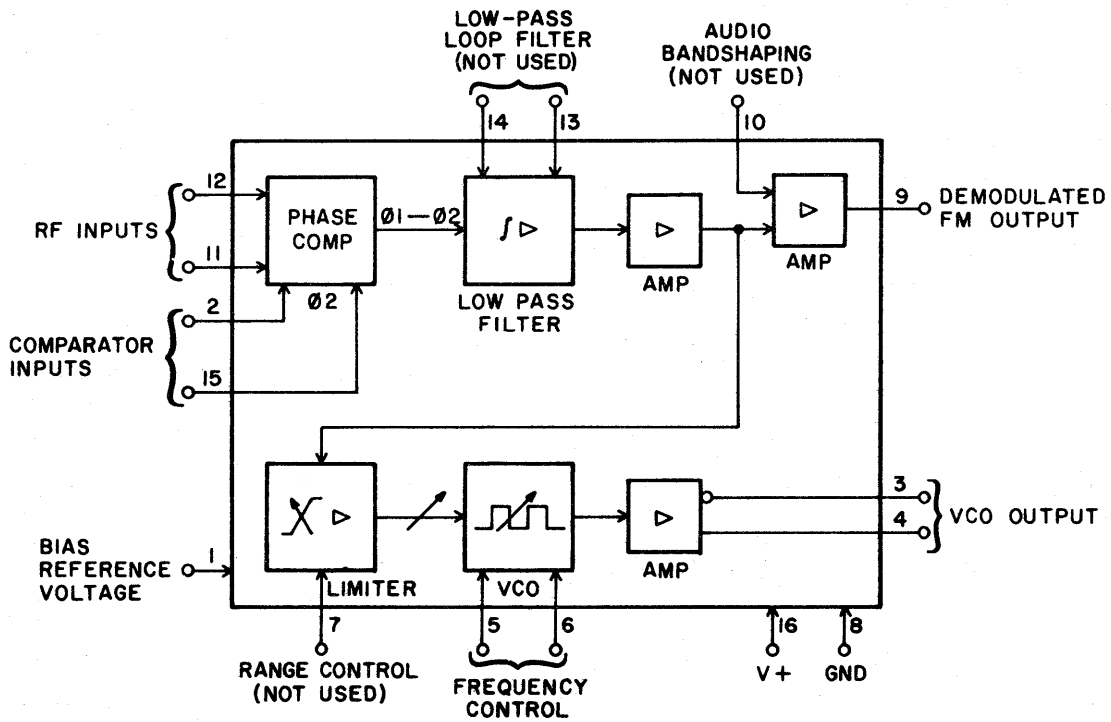
1. Vendor identification: 562B
2. Package pin configuration.



579
Rev J
Sheet 1 of 2



APPLICATION



BLOCK DIAGRAM

579
Rev J
Sheet 2 of 2

DESCRIPTION

The 581 circuit is a phase-frequency detector. This device contains two digital phase detectors, an emitter follower amplifier, and a charge pump circuit that converts TTL inputs to a dc voltage for use in frequency discrimination and phase-locked-loop applications.

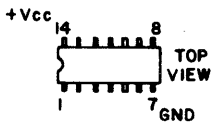
The two phase detectors have common inputs. Phase-frequency detector A is locked in (indicated by both outputs high) when the negative transitions of the variable input (pin 3) and the reference input (pin 1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, output pin 13 goes low; conversely, output pin 2 goes low when the variable input is higher in frequency or leads the reference input in phase. The variable and reference inputs to phase detector A are not affected by duty cycles because negative transitions control operations.

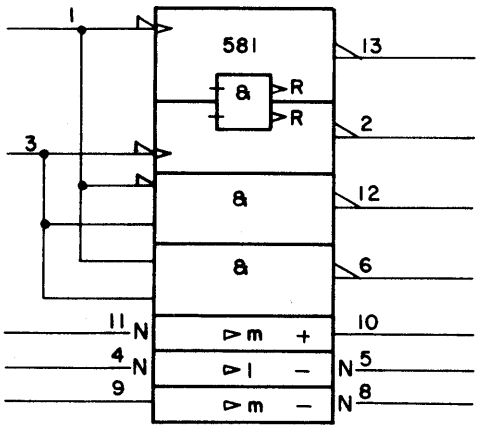
Phase detector B is locked in when the variable input phase lags the reference phase by 90° (indicated by output pins 6 and 12 alternately going low with equal pulse widths). If the variable input lags by more than 90°, pin 12 will remain low longer than pin 6 Conversely, if the variable input phase lags the reference phase by less than 90°, pin 6 remains low longer. In phase detector B, the variable input and the reference input must have 50% duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed-amplitude positive and negative pulses.

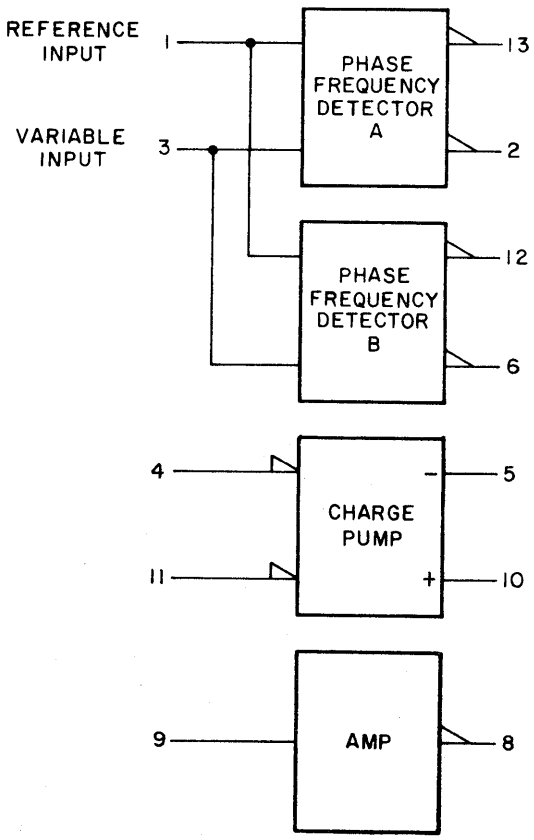
NOTES:

1. Vendor identification: 4044, 4344
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION DIAGRAM

581
Rev J
Sheet 1 of 1

DESCRIPTION

The 582 circuit is a dual voltage-controlled multivibrator. The dc control input on pins 2 and 12 determines the precise frequency of the multivibrator. The value of the external capacitor between pins 3 and 4 or 10 and 11 determines the operating frequency range. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5.0 volts. The value of the external capacitor may be determined by either of two equations:

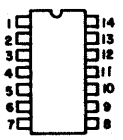
$$C = \frac{500\ uF}{F\ max} \text{ or } C = \frac{100\ uF}{F\ min},$$

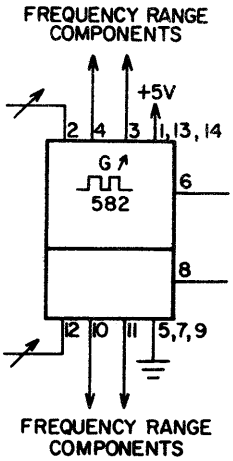
with F given in hertz. The maximum operation frequency is 30 megahertz.

The 582 has three power and three ground connections. Each multivibrator has its separate power (pins 1 and 13) and ground (pins 5 and 9) connection. The two output buffers have a common power (pin 14) and ground (pin 7) connections. All grounds must always be connected. The output buffer transforms the logic levels.

NOTES:

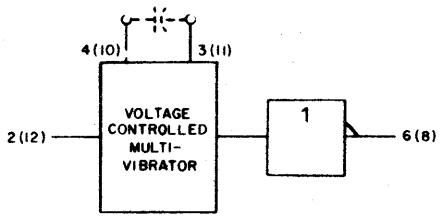
1. Symbol sections may appear separately.
2. Vendor identification: MC4024
3. Package pin configuration:





LOGIC SYMBOL

NOTE: Lines to pins 2 and 12 could be thus: —X— , —/— , or —↗— depending upon whether the input is analog or non-logic level, non-standard logic level, or from a variable parameter control, respectively.



FUNCTIONAL DIAGRAM

FIGURE 1
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(15pF FEEDBACK CAPACITOR)

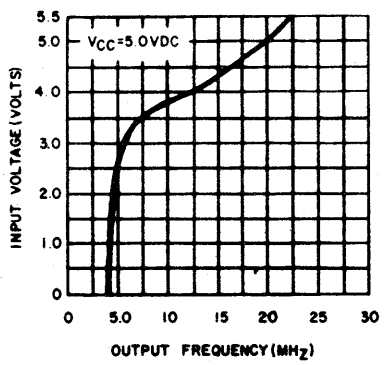


FIGURE 2
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(100pF FEEDBACK CAPACITOR)

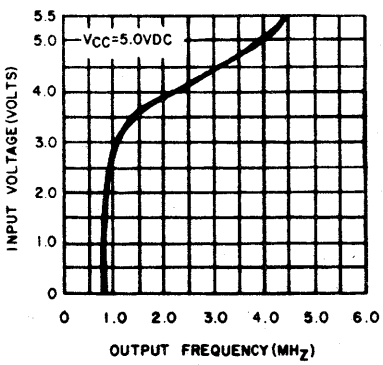
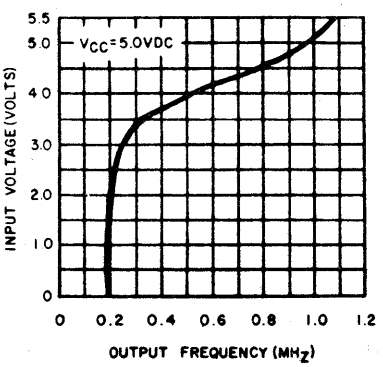


FIGURE 3
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(430pF FEEDBACK CAPACITOR)



582
Rev J
Sheet 1 of 1

DESCRIPTION

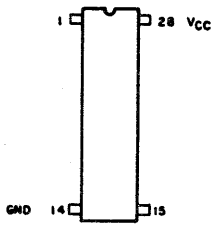
Element 768 is a 576-bit random access memory, organized as 64 words of 9 bits each. Input data appears at the open-collector outputs in inverted form.

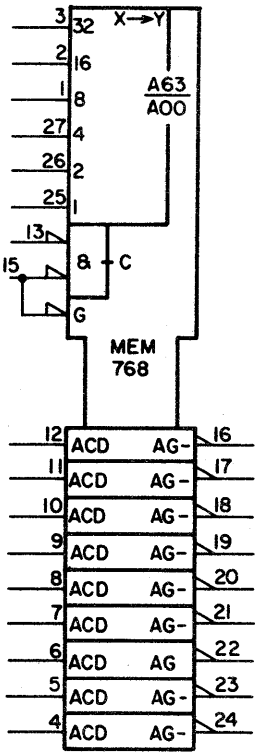
Data is written when pins 13 and 15 are both low. Data is read when pin 15 is low and pin 13 is high. Access time is typically 30 ns.

NOTES:

1. Vendor identification: 82S09, 93419

2. Package pin configuration:





LOGIC SYMBOL

768
Rev J
Sheet 1 of 1

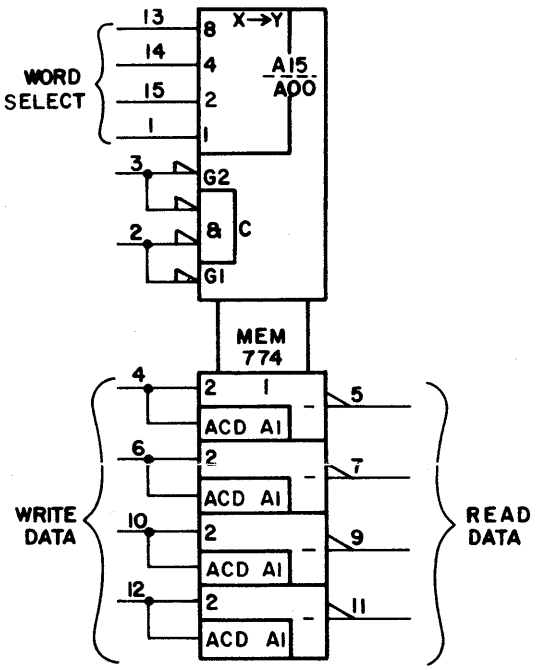
DESCRIPTION

The 774 is a TTL 64-bit Read/Write Random Access Memory organized as 16 words of 4 bits each.

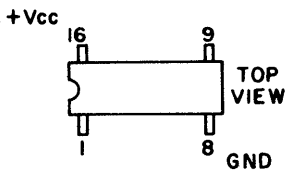
Words are selected through a 4-input binary decoder when the Chip Select input (2) is at logical 0. Data is written into the memory when Read Enable (3) is at logical 0 and read from the memory when pin 3 is at logical 1. The complement of the Write Data inputs is available at the Read Data outputs whenever Read Enable is a logical 0, regardless of the State of Chip Select.

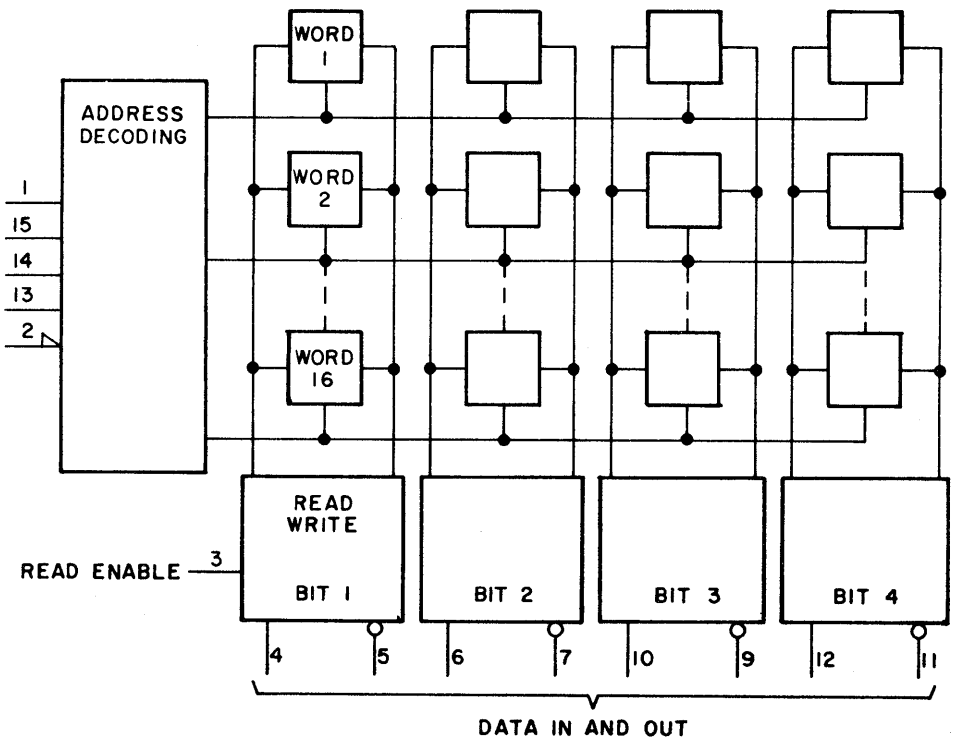
NOTES:

1. Vendor identification: 7489
2. Package pin configuration.



LOGIC SYMBOL





FUNCTION DIAGRAM

774
Rev J
Sheet 1 of 1

DESCRIPTION

The 775 circuit is a 256-bit read/write memory with a three-state output. The inputs to this memory consist of eight address lines, a write enable and three memory enables (all three must be low to read from or write into a memory location). This memory provides three output states; high or low (depending on stored data) and a high-impedance state. The high-impedance state permits bus connecting to similar outputs.

A Write operation is performed by placing a low on the write enable input, a low on all three memory enable inputs and selecting a memory address. This stores the complement of the input data in the selected location.

A Read operation is performed by placing a high on the write enable input, a low on all three memory enable inputs and selecting a memory address. This places the complement of the stored information at the output.

The output is held in a high-impedance state when the write enable is low or if any one of the three memory enables is high

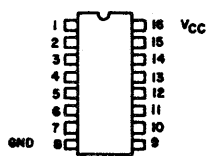
The two circuits (775 and 775A) are functionally identical except for cycle time.

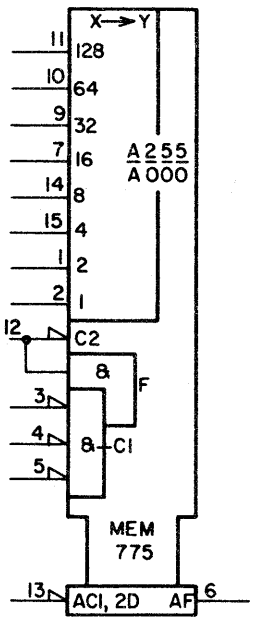
NOTES:

1. Vendor identification:

Element M	Vendor Number
775	74200
775A	82S06

2. Package pin configuration:





NOTE:
SEE FUNCTIONAL DIAGRAM FOR PIN FUNCTIONS

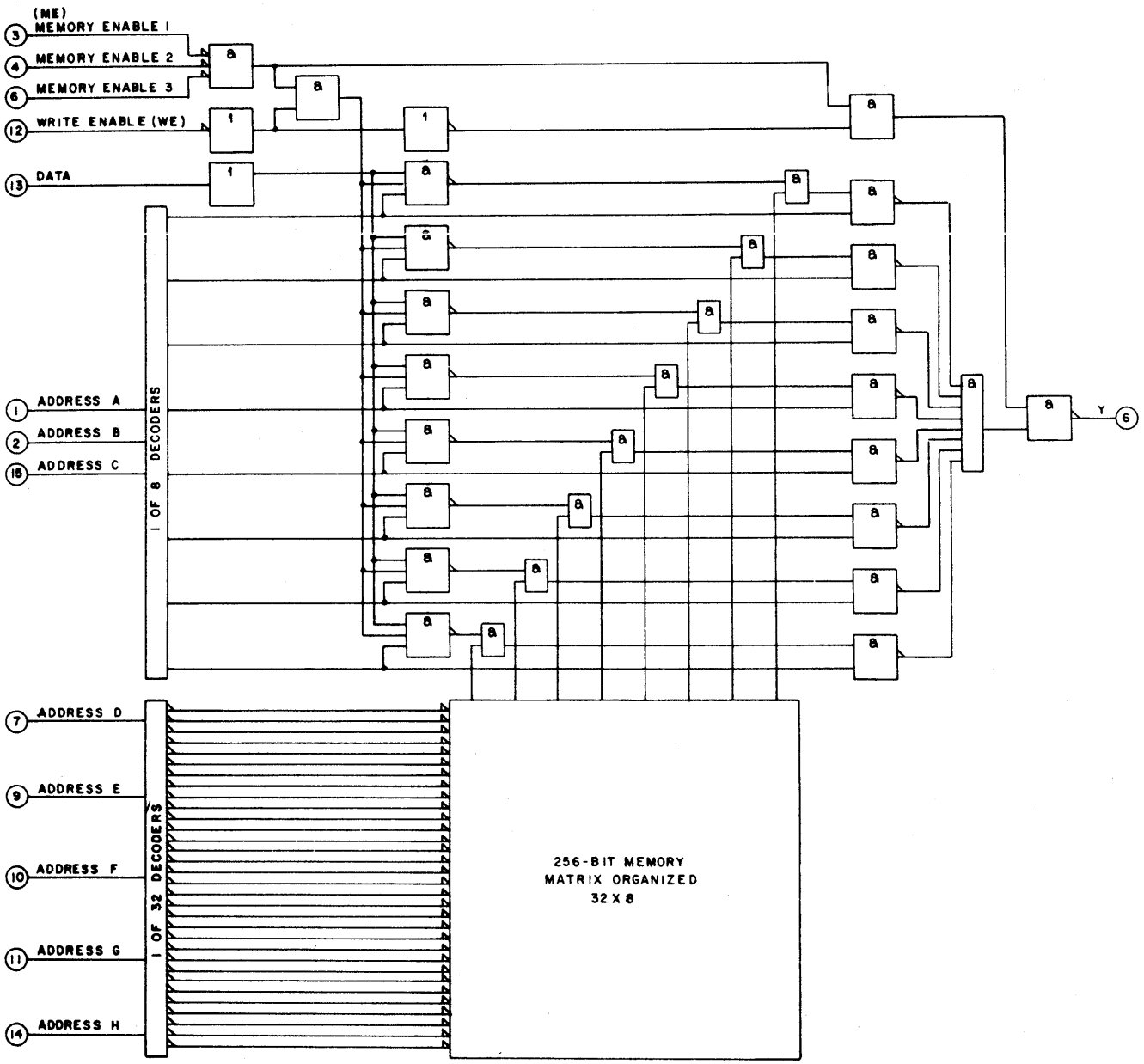
LOGIC SYMBOL

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE*	WRITE ENABLE	
WRITE (STORE COMPLEMENT OF DATA)	L	L	HIGH IMPEDANCE
READ	L	H	STORED DATA
INHIBIT	H	X	HIGH IMPEDENCE

* FOR MEMORY ENABLE:
L = ALL ME INPUTS LOW
H = ONE OR MORE ME INPUTS HIGH

TRUTH TABLE

775
Rev M
Sheet 1 of 2



FUNCTION DIAGRAM

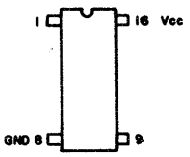
775
Rev J
Sheet 2 of 2

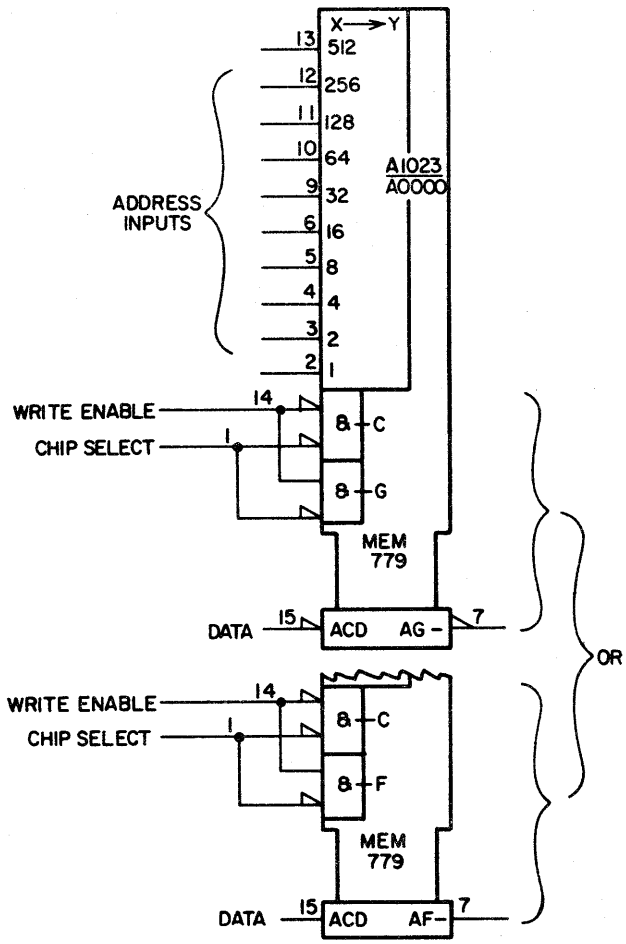
DESCRIPTION

Element 779 is a 1024-word by 1-bit (1024x1) random-access memory with an open-collector output. On-chip address selection is made when the Chip Select input goes low. Read and Write operations are controlled by the low-active Write Enable signal, as given in the truth table. Information read from the selected address is real (non-inverted) data. As in all open-collector elements, a pull-up resistor is required to provide a High output.

NOTES:

1. Vendor identification: 93415
2. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUT	MODE
CHIP SELECT	WRITE ENABLE	DATA (PIN 15)	PIN 7	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D	READ

D = DATA STORED AT SELECTED ADDRESS

TRUTH TABLE

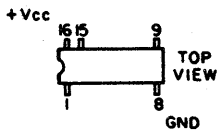
779
Rev J
Sheet 1 of

DESCRIPTION

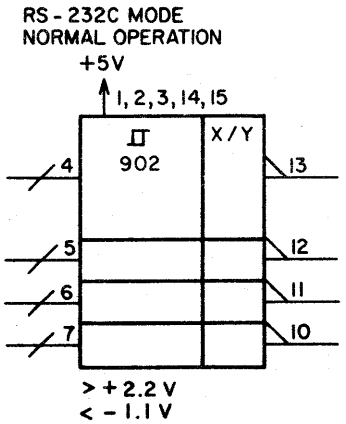
The 902 is a monolithic quadruple line receiver satisfying interface requirements for equipments as defined by EIA Standard RS-232C. The receiver is DTL/TTL compatible on inputs and inverting outputs.

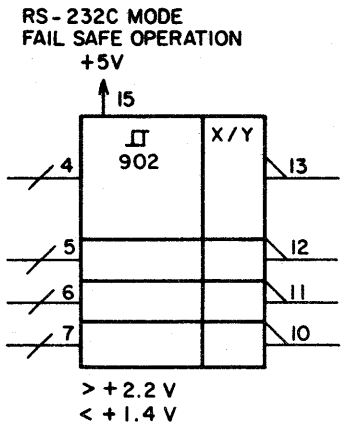
NOTES:

1. Vendor identification: 75154
2. Package pin configuration.

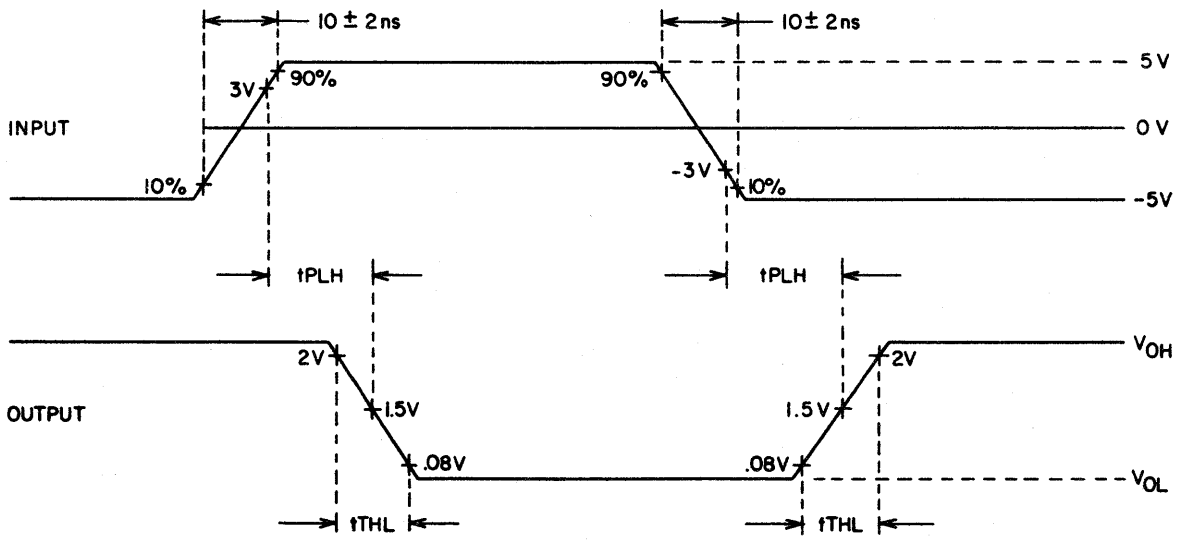


3. For normal operation connect threshold-control terminals to Vcc 1, pin 15.
4. For fail-safe operation threshold-control terminals are open.





LOGIC SYMBOLS



VOLTAGE WAVEFORMS

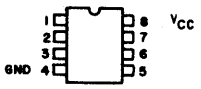
902
Rev. J
Sheet 1 of 1

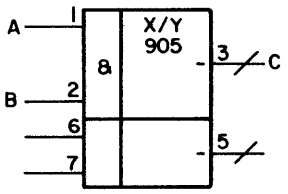
DESCRIPTION

The 905 circuit is a dual driver incorporating TTL logic with open-collector output. The output is low when either or both inputs are low. The output is I (indeterminate) when both inputs are high. When an external pull-up resistor is used the output is high, instead of I. The propagation delay from a low to a high output is typically 45 ns. The total power dissipation is 800 mW (continuous). The input threshold is approximately 1.4V. Output drive current in the low state is 150 mA. The input or output may be open or grounded for troubleshooting without damage to the chip.

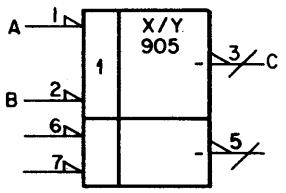
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 75451AP
3. Package pin configuration:





*C=AB



$\overline{C}=\overline{A}+\overline{B}$

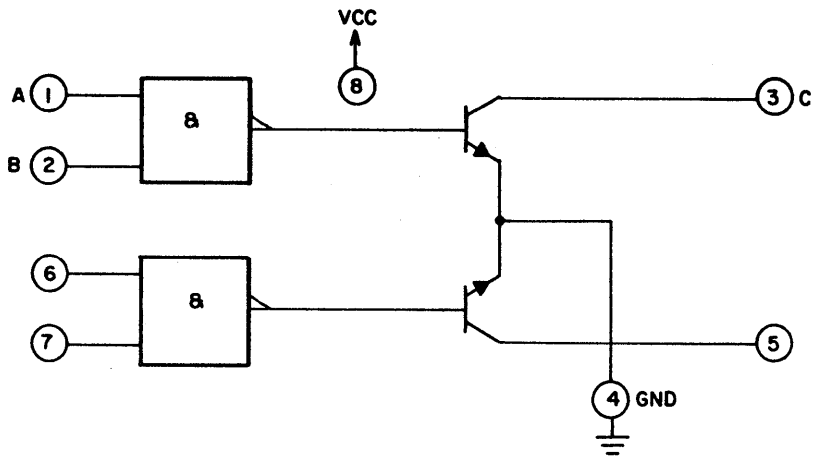
* Depends upon external output circuitry. A high is supplied when an external pull-up resistor is used in the output. The maximum voltage that the resistor can be connected to is 30 V.

LOGIC SYMBOL

INPUT PINS		OUTPUT PINS
A(1,6)	B(2,7)	C(3,5)
L	L	L
L	H	L
H	L	L
H	H	I

I=Indeterminate-the open-collector output supplies neither a high nor a low. A high is supplied when an external pull-up resistor is used in the output.

TRUTH TABLE



FUNCTIONAL DIAGRAM

905
Rev J
Sheet 1 of 1

DESCRIPTION

Element 909 is a dual differential-line driver featuring a 4-input positive AND gate.

NOTES:

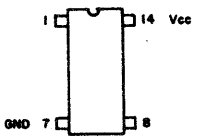
1. Symbol sections may appear separately.
2. Vendor identification:

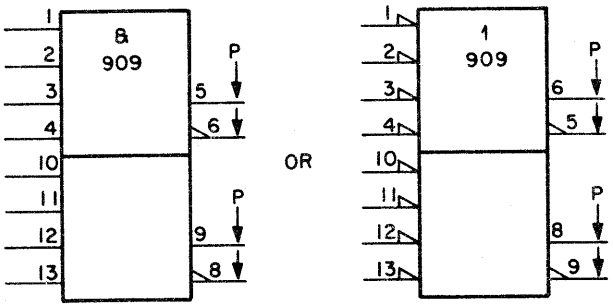
Element	Vendor Number
909	7830
909A	8830

3. Temperature range:

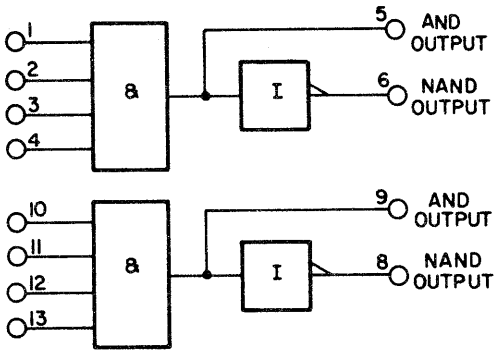
   909(7830): $-55^{o}C$ to $+125^{o}C$
   909A(8830): $0^{o}C$ to $70^{o}C$

4. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM
(POSITIVE LOGIC)

909
Rev J
Sheet 1 of 1

DESCRIPTION

Element 910 is a dual differential-line receiver with an independent strobe (G) for each section. Response time can be controlled by an external capacitor to reject input noise spikes. The output is forced High if both differential input pins are open, or if the strobe is held Low.

NOTES:

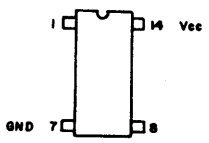
1. Symbol sections may appear separately.
2. Vendor identification:

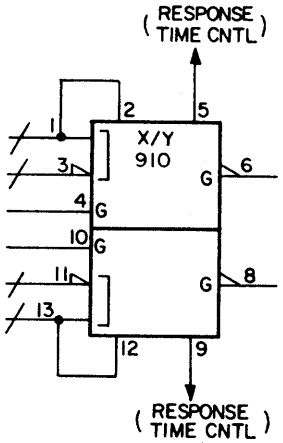
Element	Vendor Number
910	7820
910A	8820

3. Temperature range:

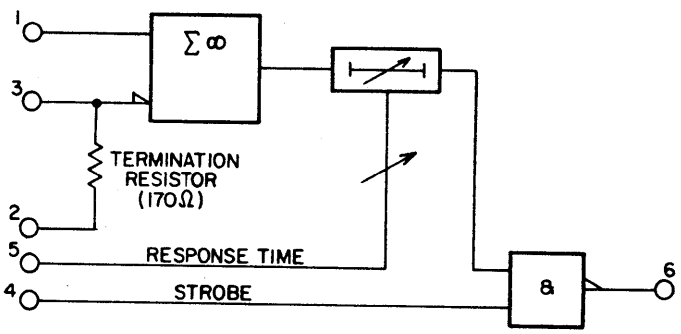
   910 (7820): $-55^{\circ}C$ to $+125^{\circ}C$.
   910A (8820): $0^{\circ}C$ to $+70^{\circ}C$.

4. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM
(ONE SECTION)

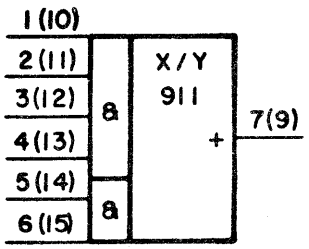
910
Rev J
Sheet 1 of 1

DESCRIPTION

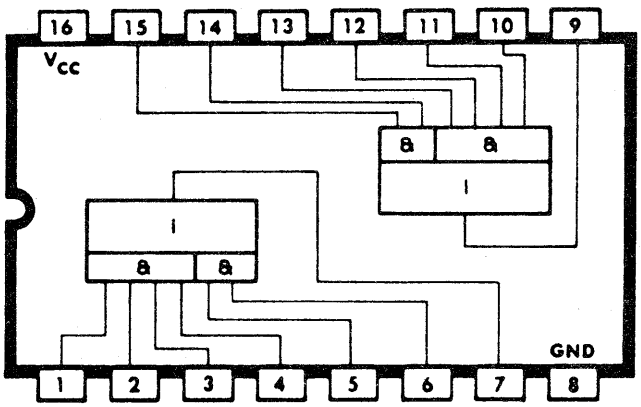
Element 911 consists of two dual input, non-inverting AND/OR line drivers mounted on a single chip.

NOTES:

1. Pin numbers in parentheses are for second section.
2. Sections may appear separately.
3. Vendor identification: 9743 (Honeywell)



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

	IN	OUT
0	0V	0V
1	3V	2.5–3.5V

LOGIC VOLTAGES

INPUT PINS						OUTPUT (PIN 7)
1	2	3	4	5	6	
1	1	1	1	X	X	1
X	X	X	X	1	1	1

X = DON'T CARE CONDITION
ALL OTHER INPUT CONDITIONS RESULT IN "0" OUTPUT

TRUTH TABLE

911
Rev J
Sheet 1 of 1

DESCRIPTION

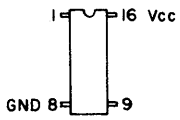
Element 912 consists of three line receivers mounted on a single chip.

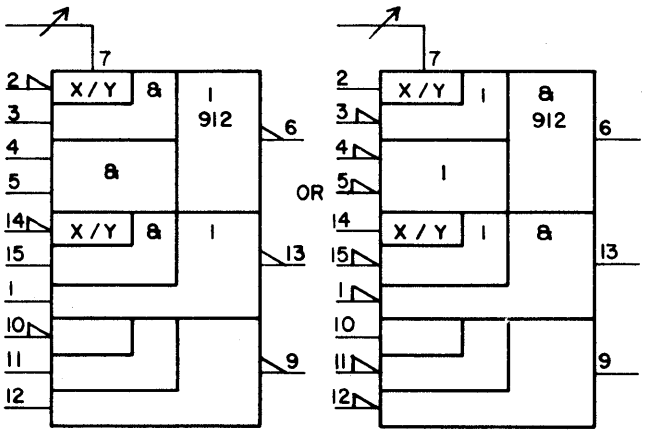
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
912	9748
912R	9749

3. Package pin configuration:





LOGIC SYMBOLS

TRUTH TABLE

INPUT PINS										OUTPUT PINS					
										HI-ACTIVE			LO-ACTIVE		
14	15	1	2	3	4	5	10	11	12	13	6	9	13	6	9
L	H	X								L	–	–	H	–	–
X	X	H								L	–	–	H	–	–
			X	X	H	H				–	L	–	–	H	–
			L	H	X	X				–	L	–	–	H	–
							L	H	X	–	–	L	–	–	H
							X	X	H	–	–	L	–	–	H

L = LOW, H = HIGH, X = DON'T CARE
INPUT CONDITIONS OTHER THAN THOSE SHOWN RESULT IN "H" OUTPUT FOR HI-ACTIVE-OUT CONFIGURATION AND "L" OUTPUT FOR LO-ACTIVE-OUT CONFIGURATION.

LOGIC VOLTAGES

	INPUT (PINS 2, 10, 14)	OUTPUT
L	<1.5 V ± 0.2 V	0.5 V MAX
H	>1.5 V ± 0.2 V	3.0–3.9 V

912
Rev J
Sheet 1 of 1

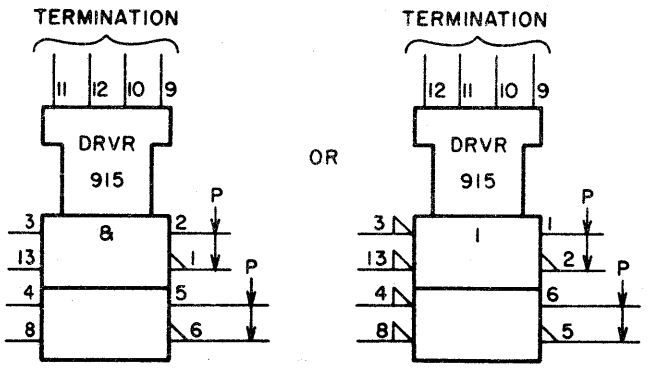
Sheet 1 of 1

DESCRIPTION

The 915 circuit consists of two monolithic TTL line drivers in one package. A 20-ohm, 1 percent resistor is connected between each of the TERMINATION pins (see logic symbol) and Vcc. Thus terminated, the relationship between the two inputs and the two outputs of either section are as follows (second-section pin numbers in parentheses):

a. With both inputs in a High state, pin 2(5) is at a higher potential than pin 1(6).

b. With either or both inputs in a Low state, pin 1(6) is at a higher potential than pin 2(5).

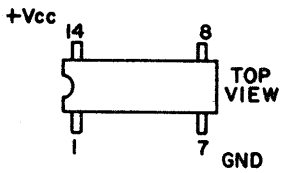


LOGIC SYMBOL

NOTES:

1. Vendor Identification: 5065989

2. Package pin configuration:



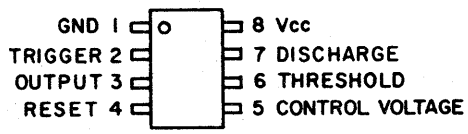
915
Rev. J
Sheet 1 of 1

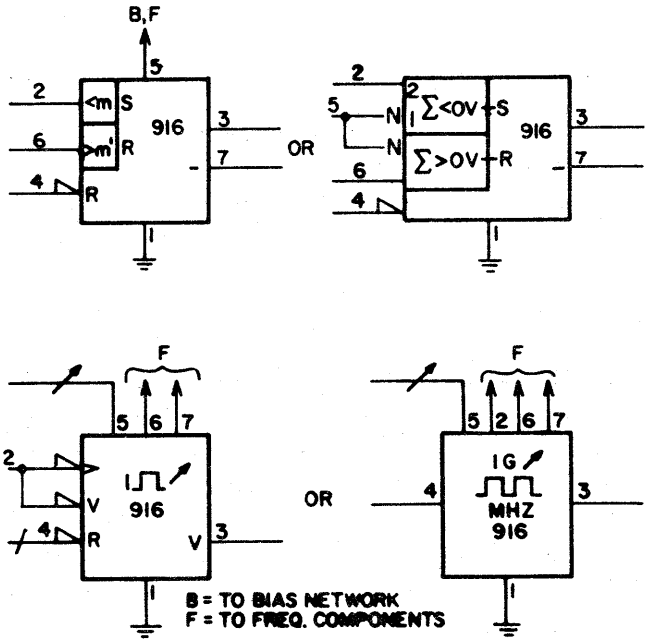
DESCRIPTION

The 916 circuit may be used as a one-shot, a free-running multivibrator, or a comparator-input FF. Descriptions are provided for each of these applications.

NOTES:

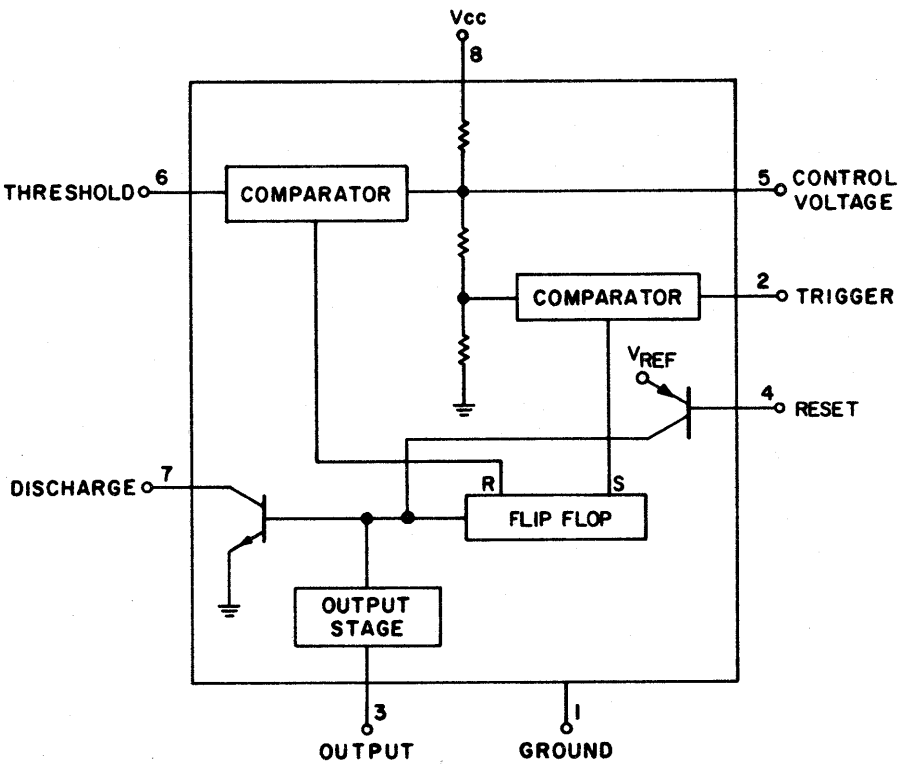
1. Vendor identification: NE555
2. Package pin configuration.





Arrows within the symbol outline and in the line to pin 5 are omitted for fixed-frequency or fixed delay applications.

LOGIC SYMBOLS



BLOCK DIAGRAM

916
Rev J
Sheet 1 of 3

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set. This releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with the time constant $\tau=R_AC$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which, in turn, discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t=1.1\ R_AC$. Because the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

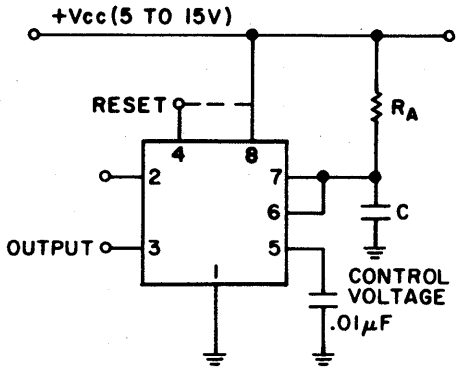


Figure 1a.

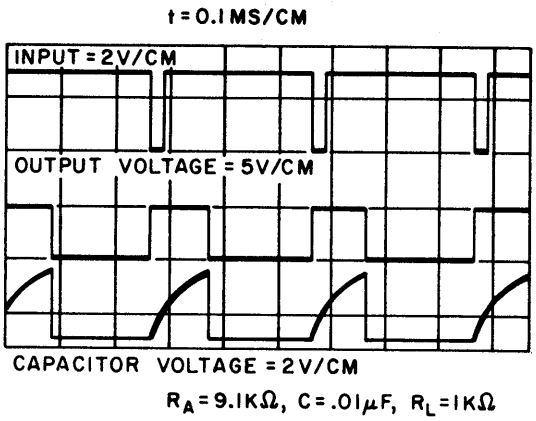


Figure 1b.

Astable Operation

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency, are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.

The charge time (output high) is given by:

$$t1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t2 = 0.693\ (R_B)\ C.$$

Comparator-Input Flip-Flop

This application is depicted by the top two symbol drawings on sheet 1. Pin 5 determines the quiescent voltage levels of the trigger (pin 2) and the threshold (pin 6). In practice:

$$Vpin6 = Vpin5;\ Vpin2 = \frac{Vpin5}{2}$$

When the level at pin 6 exceeds that at pin 5, the FF sets. When the level at pin 2 exceeds one-half of that at pin 5, the FF resets.

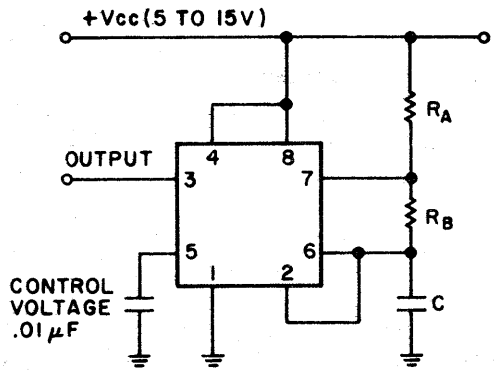


Figure 2a.

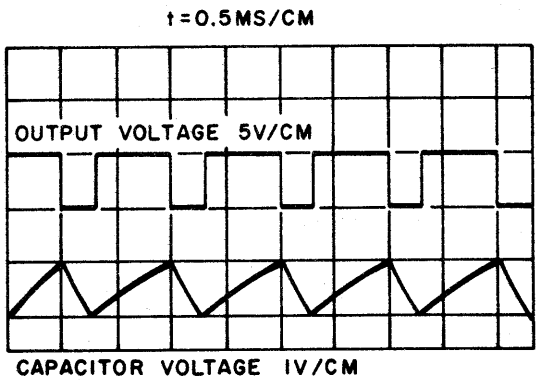


Figure 2b.

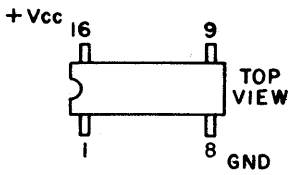
DESCRIPTION

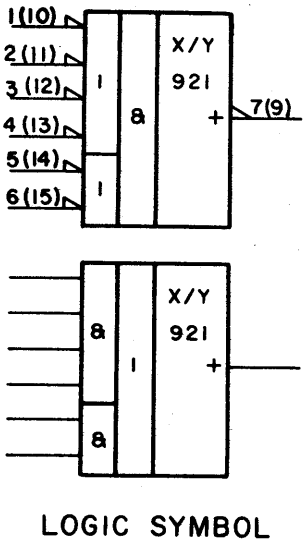
Element 921 is a line driver capable of driving terminated lines such as coaxial cable or twisted pairs. The outputs can also be used in wired OR circuits.

NOTES:

1. Vendor identification: 8T23

2. Package pin configuration.





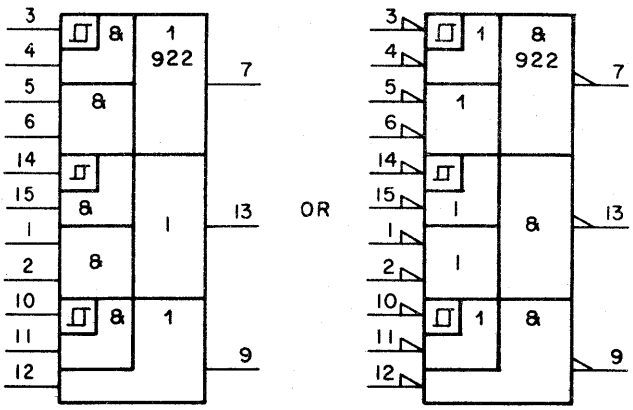
LOGIC SYMBOL

921
Rev J
Sheet 1 of 1

DESCRIPTION

The 922 is a triple Line Receiver. Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the drive circuit.

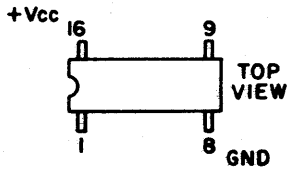
An input voltage of +1.8 volts or more is interpreted as a logical one; an input of +1.2 volts or less is interpreted as a logical zero, and is an open-circuited input.

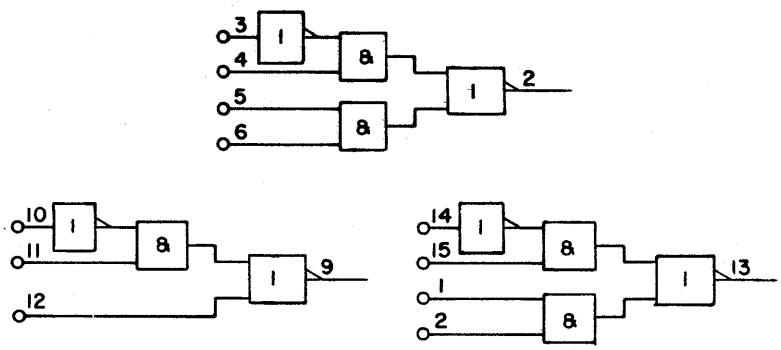


LOGIC SYMBOL

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 8T24
3. Package pin configuration.





FUNCTIONAL DIAGRAM

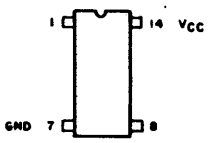
922
Rev J
Sheet 1 of 1

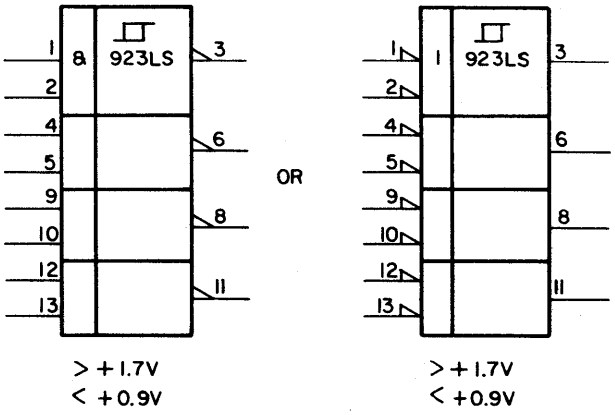
DESCRIPTION

Element 923LS consists of four 2-input, Schmitt trigger, positive NAND gates. The input threshold levels, which differ by typically 800 mV for positive-and negative-going signals because of hysteresis (backlash) in the trigger circuit, are a part of the logic symbol.

NOTES:

1. Sections may appear separately.
2. Vendor identification: 74LS132
3. Package pin configuration:





LOGIC SYMBOL

923
Rev J
Sheet 1 of 1

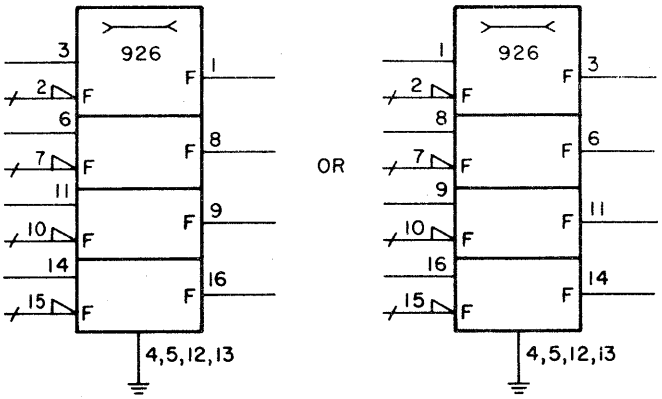
DESCRIPTION

Element 926 is an analog gate that switches on and off under the control of a binary input. A logic "0" turns the gate on and allows it to pass an analog signal from input to output. A logic "1" turns the gate off and causes it to block the analog signal.

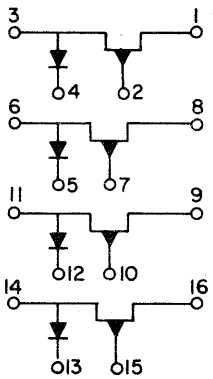
Pins	Function
3,6,11,14	Analog Inputs
1,8,9,16	Analog Outputs
2,7,10,15	Binary Inputs
4,5,12,13	Ground

NOTES:

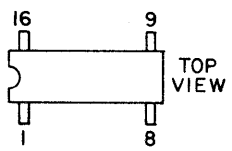
1. Symbol sections may appear separately.
2. Vendor Identification: IH5012



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



PACKAGE PIN CONFIGURATION

BINARY INPUT	FUNCTION
1	BLOCKS ANALOG SIGNAL
0	PASSES ANALOG SIGNAL

TRUTH TABLE

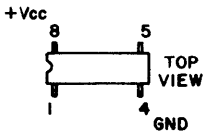
926
Rev. J
Sheet 1 of 1

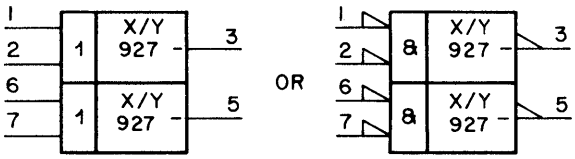
DESCRIPTION

The 927 is a dual peripheral positive-OR driver with DTL/TTL compatible inputs and an open-collector output.

NOTES:

1. Vendor identification: 75453
2. Package pin configuration.

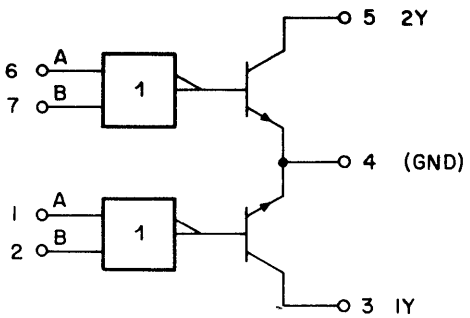




LOGIC SYMBOL

INPUTS		OUTPUT
A	B	Y
L	L	L (ON STATE)
L	H	H (OFF STATE)
H	L	H (OFF STATE)
H	H	H (OFF STATE)

TRUTH TABLE



FUNCTION DIAGRAM

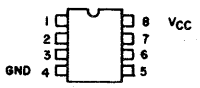
927
Rev J
Sheet 1 of 1

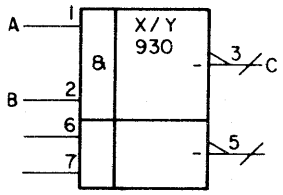
DESCRIPTION

The 930 circuit is a dual driver incorporating TTL logic with an open-collector output. The output is low when both inputs are high. The output is I (indeterminate) when either of both inputs are low. When an external pull-up output resistor is used, the output is high instead of I. The propagation delay time from a low to a high output is typically 50 ns. The power dissipation is 800 mW (continuous). The input threshold voltage is approximately 1.4 V. Output drive current in the low state is 150 mA. The input or output may be open or grounded for troubleshooting without damage.to the chip.

NOTES:

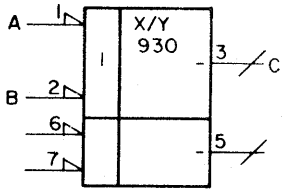
1. Symbol sections may appear separately.
2. Vendor identification: 75452
3. Package pin configuration:





$\overline{C} = AB$

VCC = PIN 8
GND = PIN 4



* $C = \overline{A} + \overline{B}$

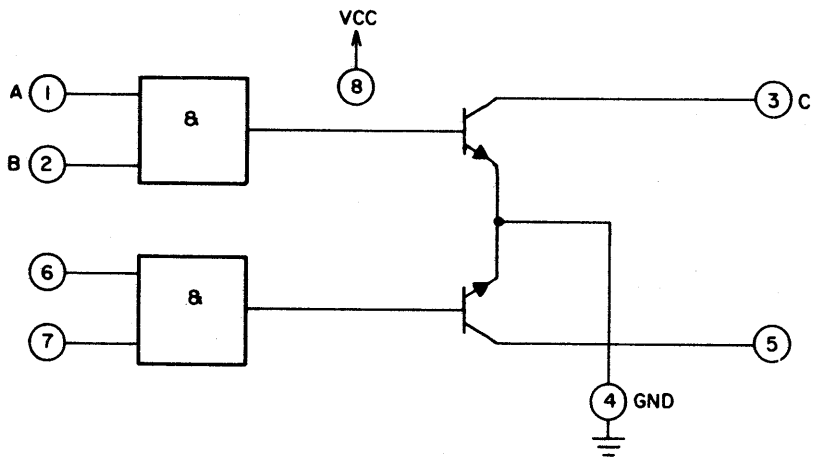
* Depends upon external output circuitry. A high is supplied when an external pull-up resistor is used in the output. The maximum voltage that the resistor can be connected to is 30 V.

LOGIC SYMBOL

INPUT PINS		OUTPUT PINS
A(1,6)	B(2,7)	C(3,5)
L	L	I
L	H	I
H	L	I
H	H	L

I=Indeterminate-the open-collector output supplies neither a high nor a low. A high is supplied when an external pull-up resistor is used in the output.

TRUTH TABLE



FUNCTIONAL DIAGRAM

930
Rev J
Sheet 1 of 1

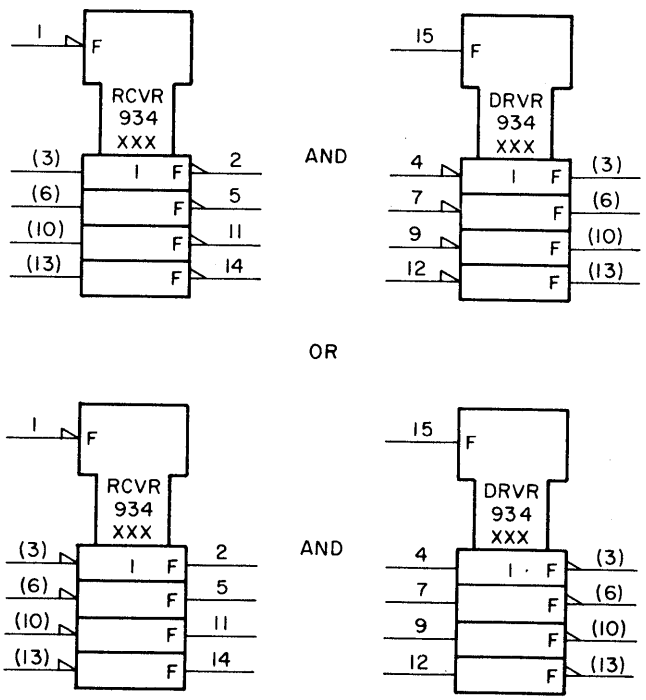
DESCRIPTION:

Element 934 is a quad bus receiver/driver with four pairs of inverting gates that have 3-state outputs. All four sections are controlled in common by separate Receive and Drive enable lines.

A low on pin 1 (Receive Enable) enables the 3-state receiver outputs; a high on pin 1 forces the receiver outputs to the high-impedence state.

Conversely, a high on pin 15 (Drive Enable) enables the 3-state driver outputs, while a low on pin 15 forces them to the high-impedance state.

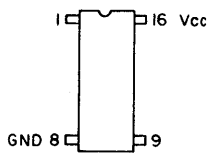
Each driver gate can sink up to 40 mA.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 8T26
2. Package pin configuration:



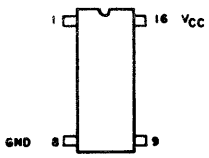
934
Rev. J
Sheet 1 of 1

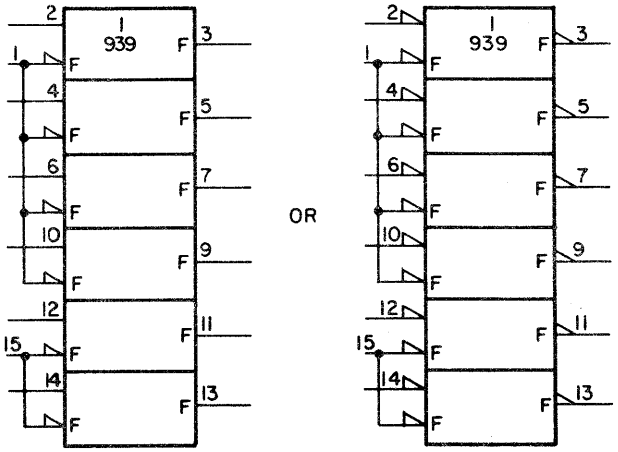
DESCRIPTION

Element 939 is a TTL non-inverting hex buffer with three-state outputs.

NOTES:

1. Vendor identification: 8097/74367
2. Package pin configuration:





LOGIC SYMBOL

INPUTS		OUTPUT
F	DATA	
H	X	HI-Z
L	H	H
L	L	L

TRUTH TABLE
(EACH SECTION)

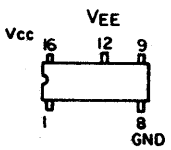
939
Rev M
Sheet 1 of 1

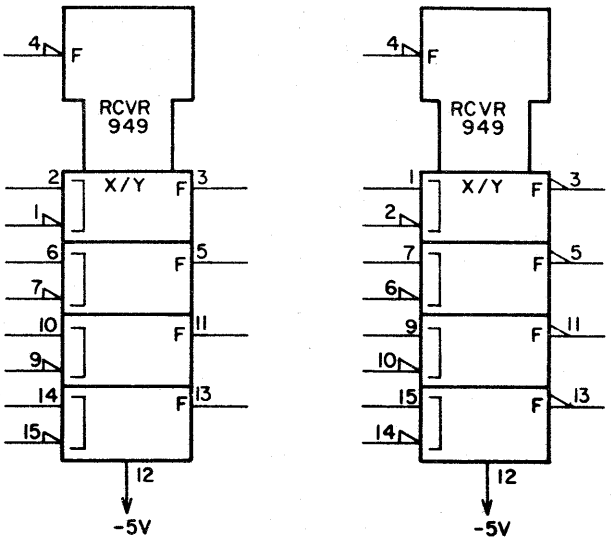
DESCRIPTION

The 949 circuit is a quad differential line receiver with three-state outputs and a common strobe input. When the strobe input (Pin 4) is low, the output of each receiver section is determined by the differential voltage across its line inputs. With the strobe input high, all receiver outputs are in the high-impedance (Hi-Z) state.

NOTES:

1. Vendor identification: MC3450
2. Package pin configuration:





LOGIC SYMBOL

INPUT	STROBE	OUTPUT
VID ≥ +25mV	L	H
	H	HI-Z
-25 mV < VID < +25mV	L	I
	H	HI-Z
VID ≤ -25mV	L	L
	H	HI-Z

I = INDETERMINATE STATE

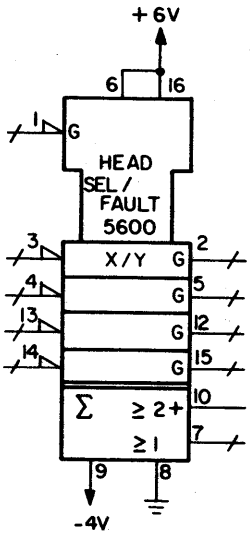
TRUTH TABLE

949
Rev M
Sheet 1 of 1

DESCRIPTION

Element 5600, or its improved version, element 950A, consists of four head-select buffers having high-current capability, and a comparator for determining when multiple heads have been selected. A high on the low-active Chip Select input (pin 1) forces all output pins low, as seen in the truth table on sheet 3.

Pin 10 is an open-emitter that can provide only a high-level output. The low level must be supplied by the IC (or other component) to which pin 10 is connected.



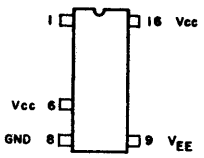
LOGIC SYMBOL

NOTES:

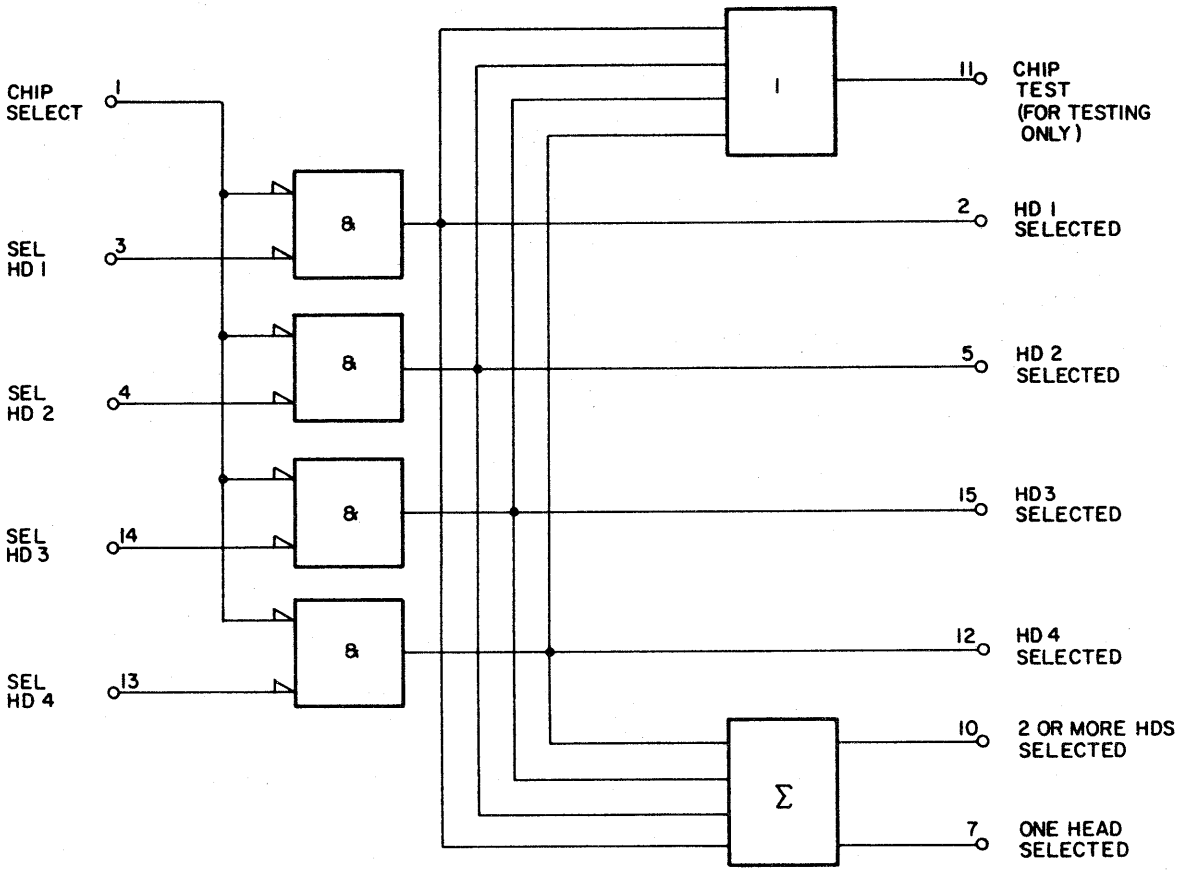
1. Vendor identification:

Element	Part Number
5600	50255600
950A	15157500

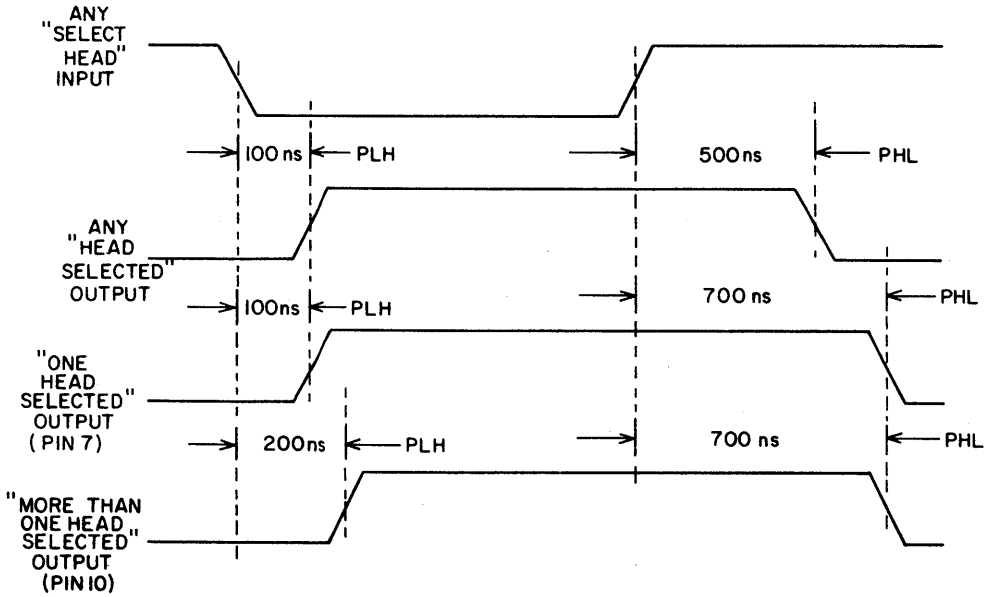
2. Package pin configuration:



950A/5600
Rev J
Sheet 1 of 3



FUNCTIONAL DIAGRAM



PLH: PROPAGATION DELAY, L-TO-H

PHL: PROPAGATION DELAY, H-TO-L

TIMING DIAGRAM

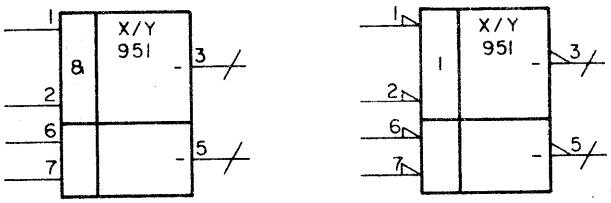
CONDITIONS	CHIP SEL	HEAD-SELECT INPUTS	HEAD SELECTED OUTPUTS	LOGIC OUTPUTS
	(1)	(3)(4)(13)(14)	(2)(5)(12)(15)	(7) (10)
CHIP NOT SELECTED	H	X X X X	L L L L	L L
CHIP SELECTED NO HEAD SELECTED	L	H H H H	L L L L	L L
CHIP SELECTED ONE HEAD SELECTED	L	ONE INPUT LOW ALL OTHERS HIGH	INVERSE OF RESPECTIVE INPUT VOLTAGE	H L
CHIP SELECTED $\geqslant$ 2 HEADS SELECTED	L	$\geqslant$ 2 INPUTS LOW ALL OTHERS HIGH	INVERSE OF RESPECTIVE INPUT VOLTAGE	H H

X = IRRELEVENT
L = LOW LEVEL VOLTAGE
H = HIGH LEVEL VOLTAGE
( ) = PIN NUMBERS

TRUTH TABLE

DESCRIPTION

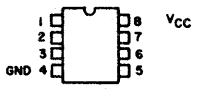
Element 951 is a dual driver incorporating TTL logic with open-collector outputs. Maximum voltage to which the external pull-up resistor may be connected is 35 V.



LOGIC SYMBOL

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 75461
3. Package pin configuration:

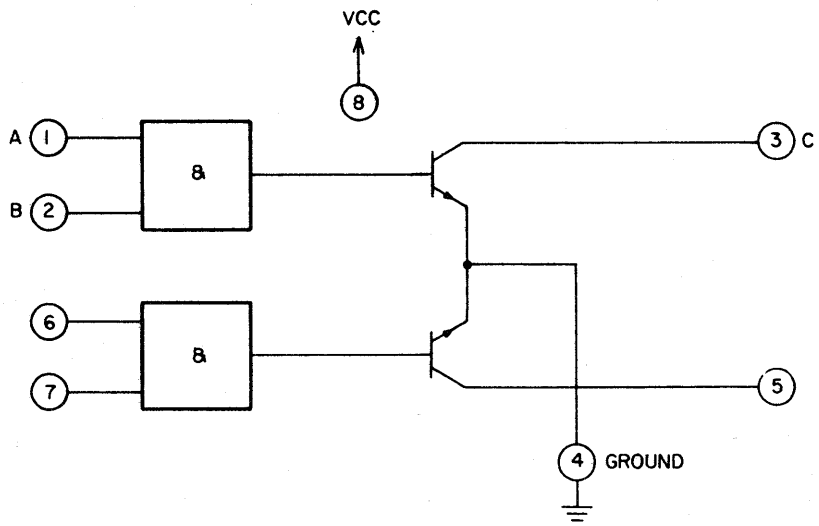


A(1,6) B(2,7)

OUTPUT PINS

TRUTH TABLE

INPUT PINS		OUTPUT PINS
A(1,6)	B(2,7)	C(3,5)
L	L	L
L	H	L
H	L	L
H	H	H



FUNCTIONAL DIAGRAM

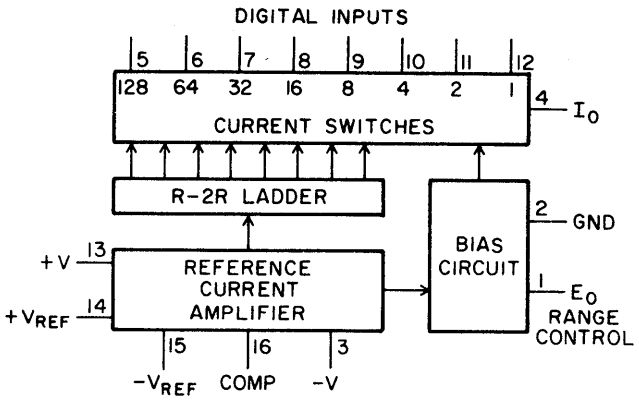
951
Rev J
Sheet 1 of 1

DESCRIPTION

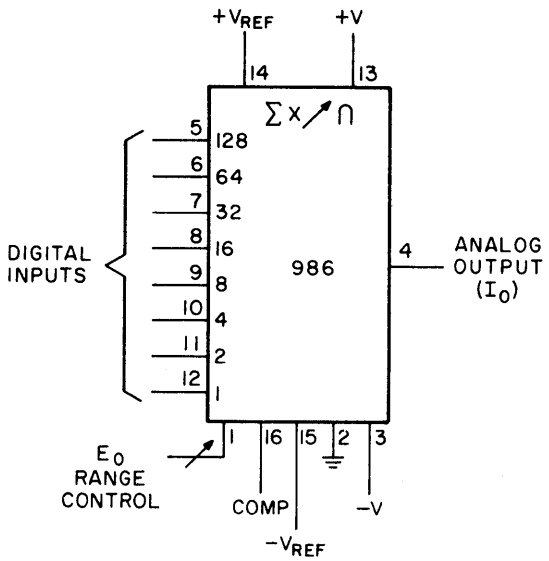
The 986 circuit is an eight-input digital-to-analog converter that provides its maximum output current (I_0) when all digital inputs are high (K=255), decreasing in discrete steps as the count goes from 255 to zero.

A reference current amplifier provides a constant current into the R-2R ladder, which divides the current into binary-related components that are fed to the current switches. Current from the reference amplifier is controlled by adjusting the positive/negative reference voltages. The output voltage (E_0) range may be varied by the voltage applied to pin 1. The compensation input, pin 16, maintains correct phase margin throughout the range.

The Typical Application diagram shows the 986 connected to provide 128 discrete output current values to an op amp (not a part of the 986 circuit). The op amp feed-back resistor is selected to provide an E_0 of 10 volts when input current to the op amp is maximum – that is, for a count of 127.



BLOCK DIAGRAM



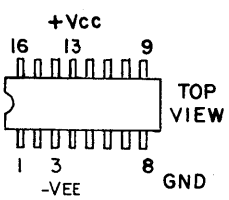
LOGIC SYMBOL

NOTES:

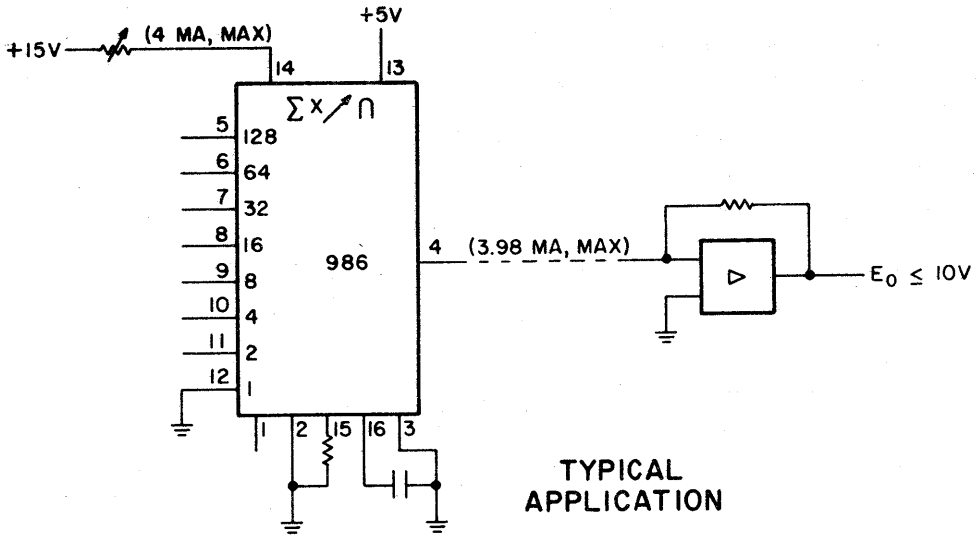
1. On a logic diagram, usually only the digital input and analog output pins are shown.
2. Vendor identification:

Element	Vendor Number
986A (6-Bit)	MC1408L-6
986B (7-Bit)	MC1408L-7
986D (8-Bit)	MC1408L-8
986E (8-Bit)	MC1408L-7.5

3. Package pin configuration.



986
Rev J
Sheet 1 of 2



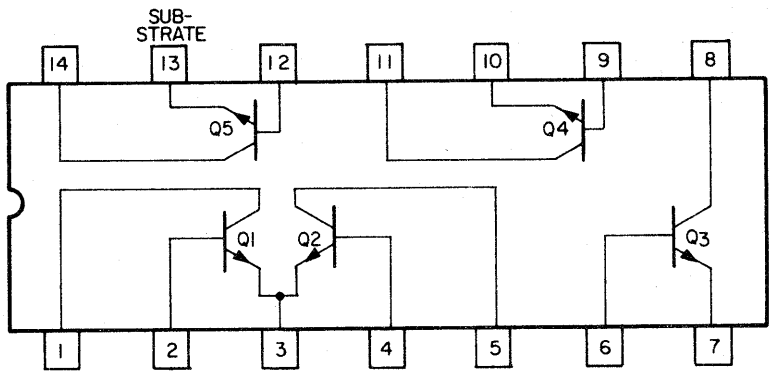
TYPICAL APPLICATION

DESCRIPTION

Element 3046 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected as a differential pair.

NOTES:

1. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to ensure normal transistor action.
2. Vendor identification: CA3046
3. Pin connections are shown below.



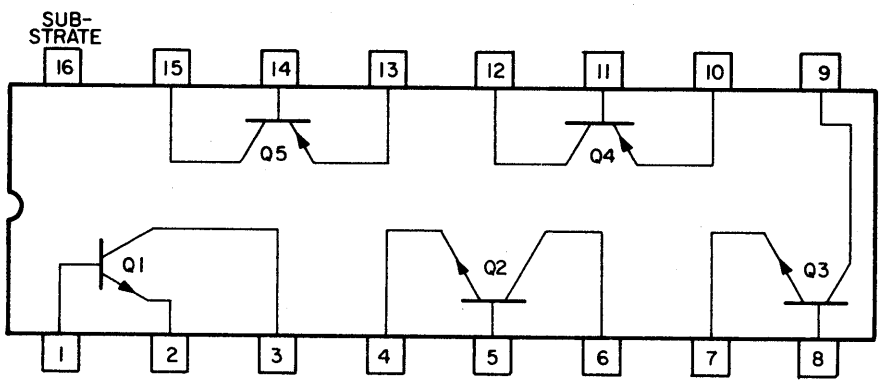
3046
Rev J
Sheet 1 of 1

DESCRIPTION

Element 3096 consists of five high-voltage, general-purpose silicon transistors mounted on a common substrate, which has a separate connection. The five-transistor array comprises three n-p-n and two p-n-p types. Typical collector-to-emitter breakdown voltage is 100 V.

NOTES:

1. Vendor identification: CA3096E
2. Pin connections are shown below.



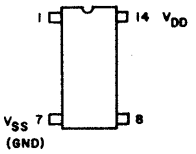
3096
Rev J
Sheet 1 of 1

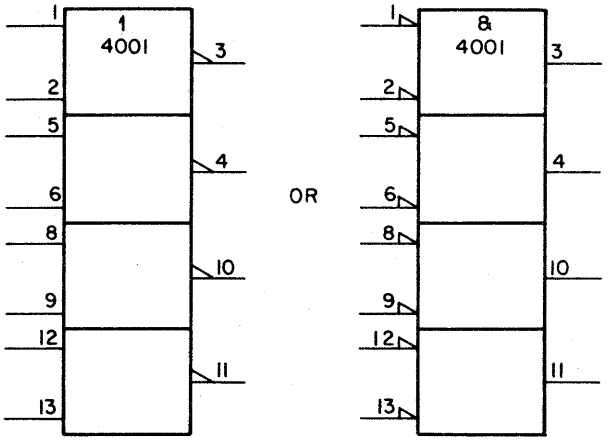
DESCRIPTION

The 4001 circuit is a CMOS package consisting of four 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4001
3. Package pin configuration:





LOGIC SYMBOL

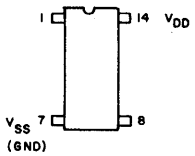
4001
Rev J
Sheet 1 of 1

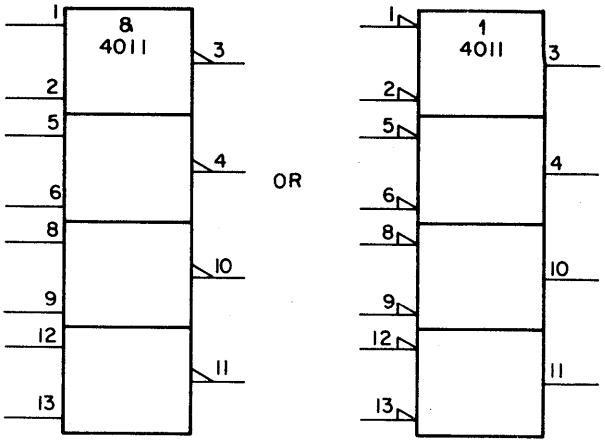
DESCRIPTION

The 4011 Circuit is a CMOS package consisting of four 2-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4011
3. Package pin configuration:





LOGIC SYMBOL

4011
Rev J
Sheet 1 of 1

DESCRIPTIONS:

Element 4016 consists of four independent CMOS bilateral switches. As shown in the functional diagram, a transmission gate (TG) responds to control input V_C (usually a binary signal) to pass or cut off the input data V_{IN}. V_{IN} may be either an analog or a binary signal with frequencies up to 54 MHz. The maximum effective pulse frequency of V_C depends upon V_{DD}, as shown below:

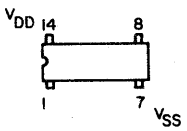
V_{DD}	V_C freq (max)
+5 V	5 MHz
+10 V	10 MHz
+15 V	12 MHz

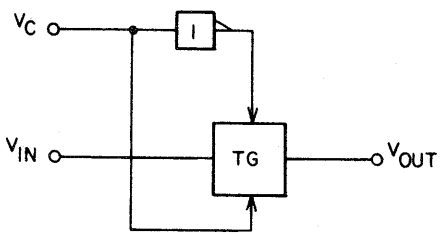
NOTES:

1. V_C high = TG ON
   V_C low = TG OFF
   (See Transmission Gate description on page 1-17)

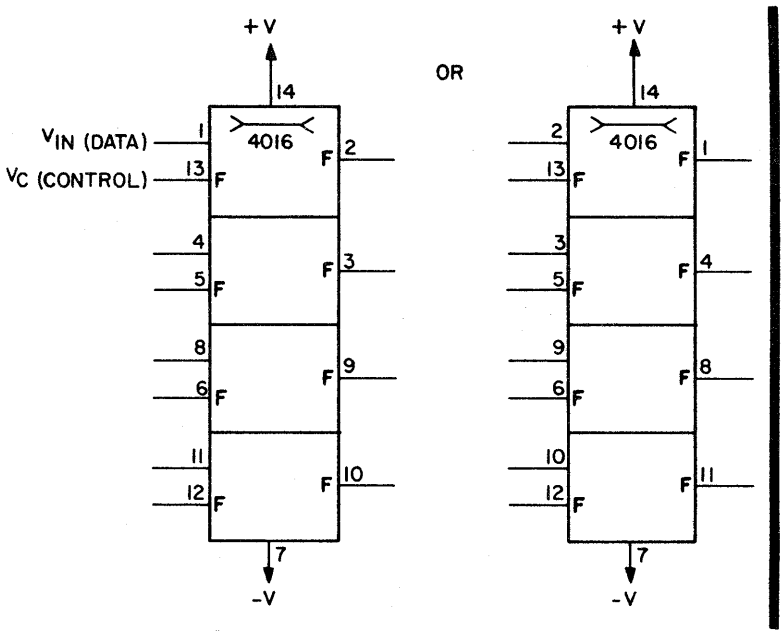
2. Vendor identification: MC14016B

3. Package pin configuration:





FUNCTIONAL DIAGRAM
(EACH SECTION)



LOGIC SYMBOL

4016
REV L
Sheet 1 of 1

DESCRIPTION

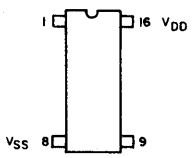
The 4017 circuit is a CMOS decade counter with an asynchronous, active-high reset and a built-in count decoder. Changes in the output occur on the positive-going edge of C (pin 14), provided that $\overline{C}$ (pin 13) is held low, or on the negative-going edge of $\overline{C}$, provided that C is held high.

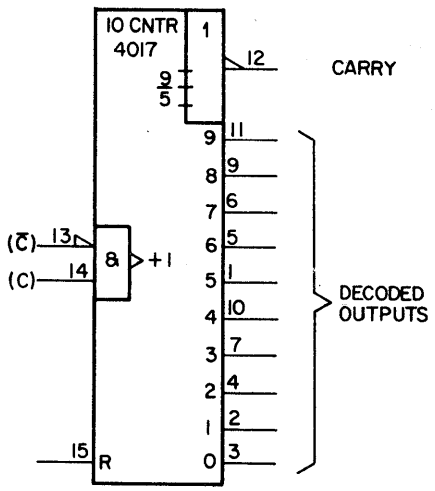
Outputs are normally low, going high only at the appropriate decimal count time.

A Carry output is provided that is high for all counts less than 5, and low for counts 5 through 9.

NOTES:

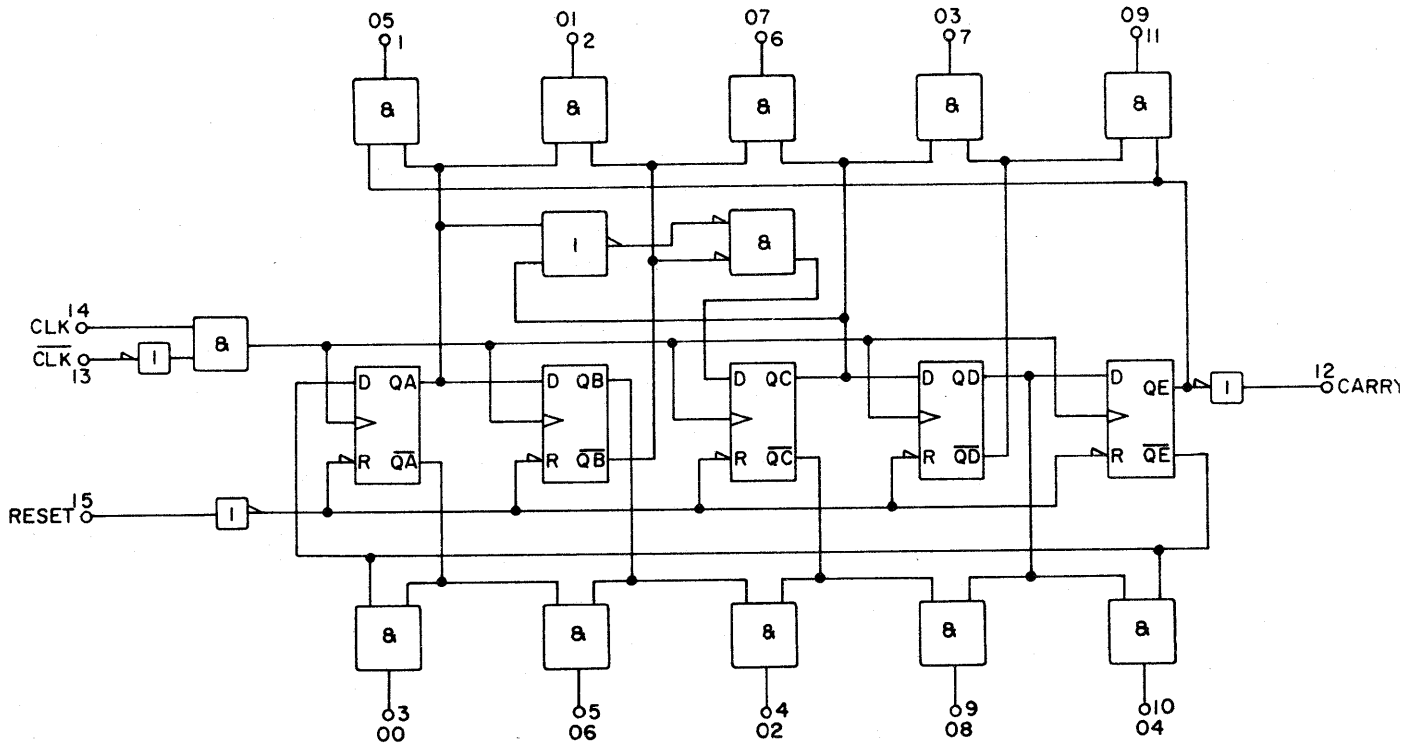
1. Vendor identification: 4017
2. Package pin configuration:

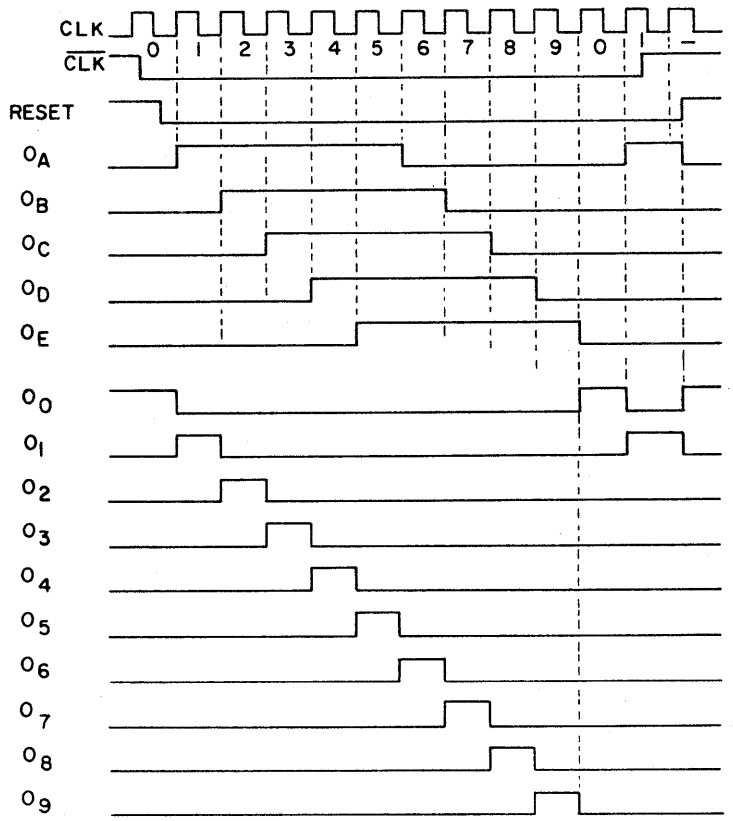




LOGIC SYMBOL

4017
Rev K
Sheet 1 of 2





TIMING DIAGRAM

(SHOWN FOR POSITIVE-GOING CLOCK ONLY)

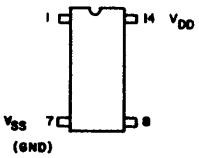
4017
Rev K
Sheet 2 of 2

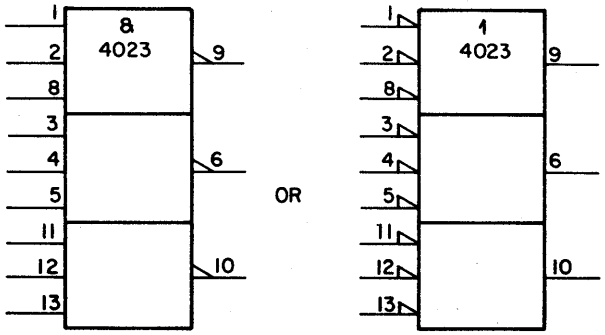
DESCRIPTION

The 4023 circuit is a CMOS package consisting of three 3-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4023
3. Package pin configuration:





LOGIC SYMBOL

4023
Rev J
Sheet 1 of 1

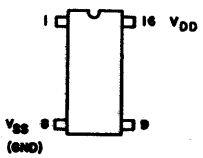
DESCRIPTION

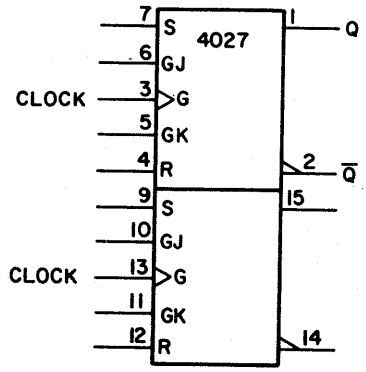
The 4027 circuit is a CMOS package consisting of two positive-edge-triggered J-K flip-flops with asynchronous set and clear inputs.

The functional (logic) diagram for the 4027 circuit appears as figure 1-15 in section 1 of this manual.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4027
3. Package pin configuration:





LOGIC SYMBOL

INPUTS					OUTPUT Qn+1		
G	GJ	GK	S	R	Q	$\overline{Q}$	
X	X	X	0	1	0	1	
X	X	X	1	0	1	0	
X	X	X	1	1	1	1	
⌐	0	0	0	0	Qn	$\overline{Qn}$	NO CHANGE
⌐	1	0	0	0	1	0	
⌐	0	1	0	0	0	1	
⌐	1	1	0	0	$\overline{Qn}$	Qn	TOGGLE

Qn = STATE OF Q OUTPUT PRIOR TO CLOCK TIME.

Qn + 1 = STATE OF OUTPUT AFTER CLOCK TIME.

⌐ = CLOCK TIME (L-TO-H TRANSITION)

X = DON'T CARE

TRUTH TABLE

4027
Rev J
Sheet 1 of 1

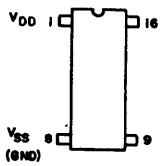
DESCRIPTION

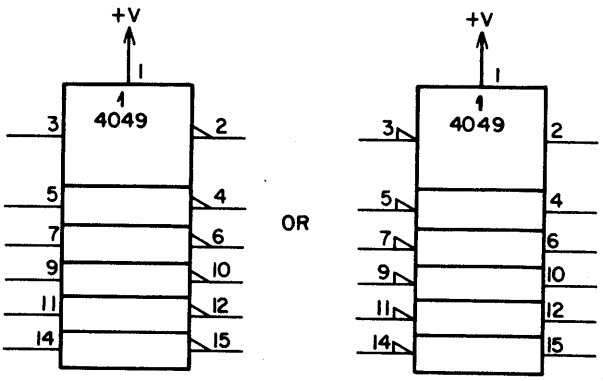
The 4049 circuit is a CMOS package consisting of six inverting buffers, each capable of driving up to two TTL loads when used as a CMOS-to-TTL converter. For that application, the high-level input voltage may exceed the TTL supply voltage (V_{CC}).

Pin 16 (normal V_{DD}) is not connected internally in this circuit, nor is pin 13.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4049
3. Package pin configuration:





LOGIC SYMBOL

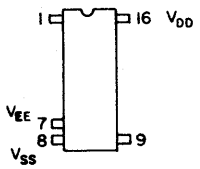
4049
Rev J
Sheet 1 of 1

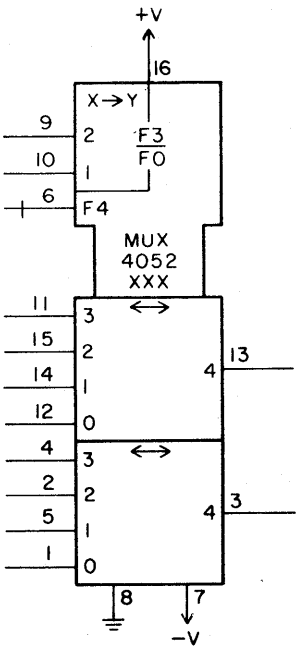
DESCRIPTION:

CMOS element 4052 is a dual 1-of-4 selector/ multiplexer with bi-directional data-flow capability. For left-to-right data flow, each section acts as a 4PST switch. For right-to-left data flow, each section acts as a SP4T switch. Both sections share the same select and inhibit controls. The inhibit line (pin 6) must be low for the device to operate.

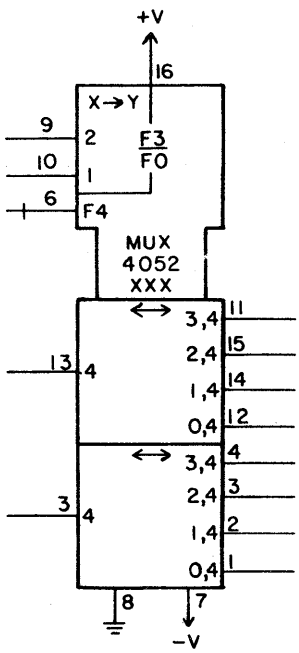
NOTES:

1. Vendor identification: 4052
2. Package pin configuration:





OR



LOGIC SYMBOL

4052
REV L
Sheet 1 of 1

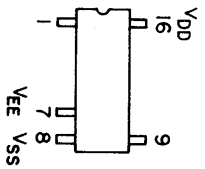
DESCRIPTION

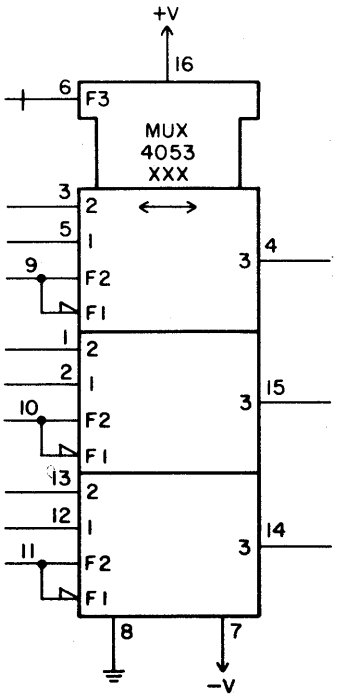
CMOS element 4053 is a bidirectional 1-of-2 selector/multiplexer with 3 sections. The sections have individual select inputs (F1, F2) and a common low-active enable (F3).

NOTES:

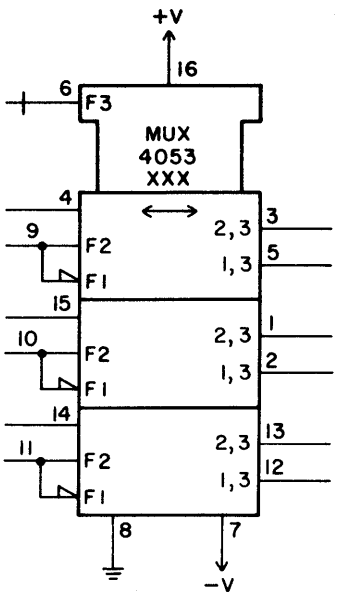
1. Vendor identification: 4053

2. Package pin configuration:





OR



LOGIC SYMBOL

4053
Rev. J
Sheet 1 of 1

Elements 5100, 5200, 5300, and 5400 constitute a phase-locked-loop oscillator (PLO), a simplified diagram of which is shown in figure 1. Table 1 gives a list of center frequencies for typical applications of the oscillator. A schematic diagram of the PLO is presented in figure 2, and subsequent sheets in this series provide the symbols and descriptions for each of the four elements, with frequent references to the schematic.

GENERAL DESCRIPTION, PLO

The phase-locked-loop oscillator affords a means of locking the timing of internal logic circuits to an external signal frequency. Typical usage is in the read/write circuits of disk memories, where the external signal is a series of servo-clock or data pulses from the rotating disk.

The essential elements of a PLO are 1) the current pump, which either pumps current into or out of a filter (R2/C2), depending upon the state of a Comparator FF (not a part of the PLO), and 2) a voltage-controlled oscillator (VCO), the frequency of which is determined by the charge across the aforementioned filter capacitor.

Supplemental elements include a constant-current source to minimize VCO frequency shifts due to power supply fluctuations, and a fast-start circuit that increases loop gain to achieve rapid lock-in -- typically with 20 pulses. When the low-active fast start signal disappears, the inertia of the PLO returns to normal so that it continues to track at the locked-in frequency despite data shift, gaps, or uneven spots in the data.

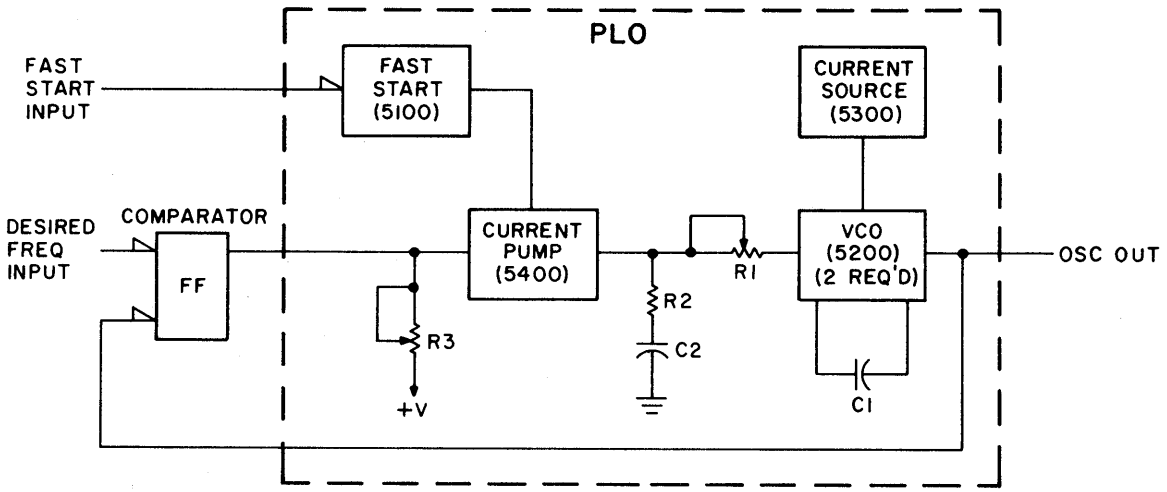


Figure 1. PLO, Simplified Block Diagram

The desired frequency and the VCO frequency will be 180 degrees out of phase when the PLO is locked in. Resistor R3 allows for precise adjustment of this relationship.

NOTE

R3 is adjusted for optimum phase relationship at the time the PLO is fabricated at the factory. This potentiometer must not be altered or adjusted in the field.

The capture range and response time of the VCO are determined by filter R2/C2. Rapid lock-in is provided to frequencies that deviate by up to 20% from the center frequency.

The center frequency of the VCO is determined by R1 and C1, and can be varied from 1 MHz to 40 MHz.

NOTE

At the time the PLO is fabricated, R1 is adjusted to the center frequency for the particular application. This potentiometer must not be altered or adjusted in the field.

Typical center frequencies (fc), with R1 and C1 values for each, are given in table 1 for various PLO applications.

TABLE 1. TYPICAL VCO/PLO CENTER FREQUENCIES

Application	fc (MHz)	R1 (Ω)	C1 (pF)
DMD Data Recovery	7.09	590	68
FMD Data Recovery	9.58	590	51
DMD Servo Input (x2)	0.886	590	680
x2	1.773	590	330
x2	3.545	590	150
x2	7.09	590	47
FMD Servo Input (x8)	2.4	590	220
x2	4.79	590	110
x2	9.58	590	68

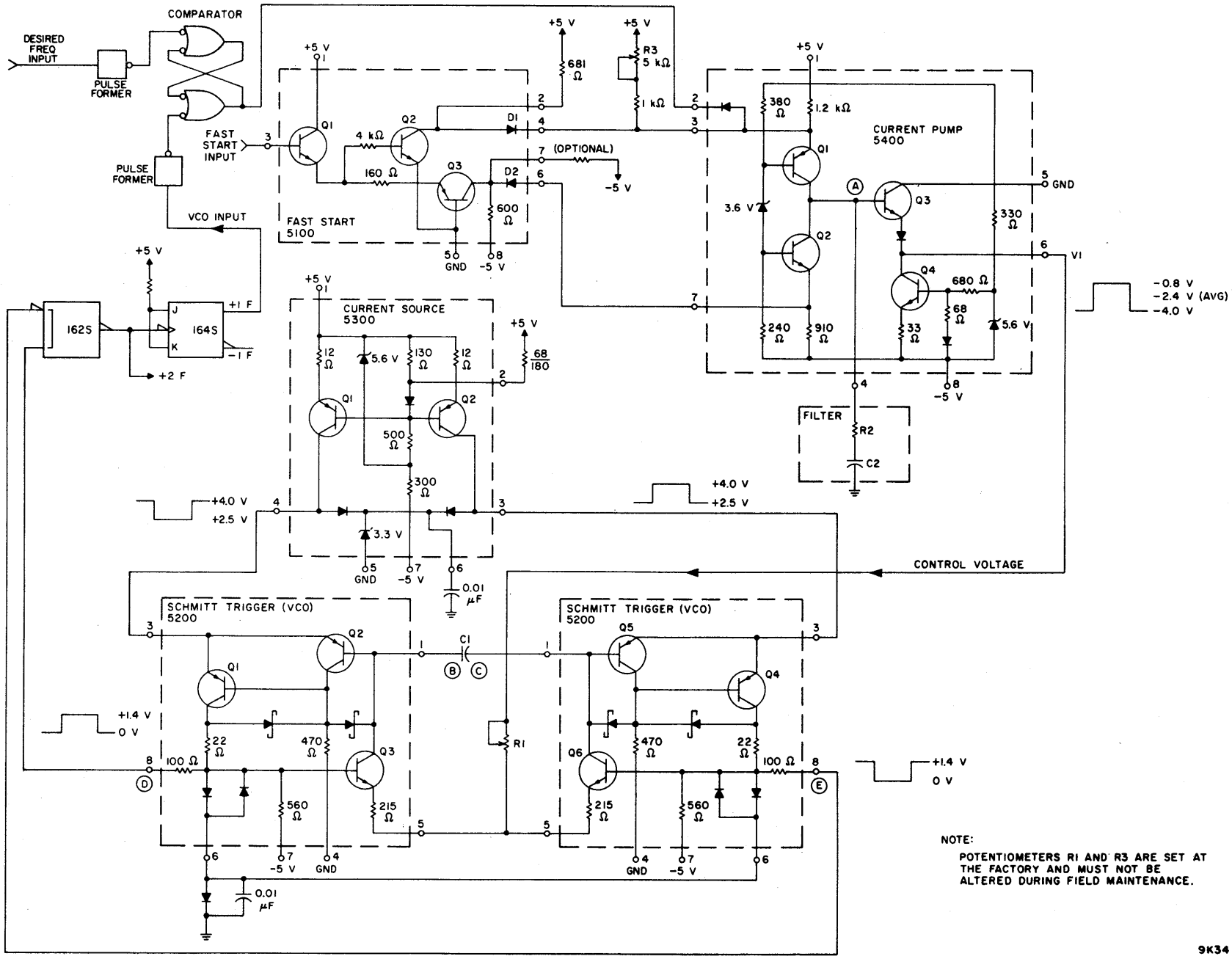
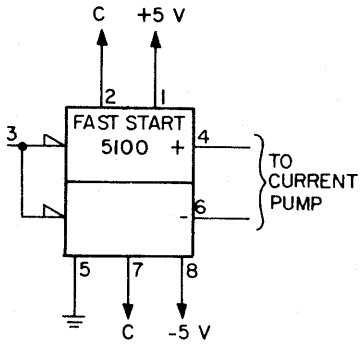


Figure 2. Schematic Diagram, Phase-Locked Oscillator (PLO)

DESCRIPTION

Element 5100 is a Fast Start circuit that accelerates the locking in of a phase-locked oscillator (PLO), usually to a data or servo-clock signal from a disk drive. It accomplishes this by increasing the current handled by the current pump (element 5400), which increases the current going into (and out of) filter R2/C2, thereby increasing the voltage swing of the pump's output (V1). This, in turn, extends the band width of the PLO, allowing it to more quickly capture, and then synchronize itself with, the desired input frequency.

In figure 2 (schematic, sheet 4), note the interconnections between elements 5100 and 5400. When diodes D1 and D2 are forward biased by a low input (Fast Start) signal to pin 3 of element 5100, the external 681 Ω resistor connected to +5 V is paralleled with the 1.2 kΩ resistor in element 5400 (via pin 4). Likewise the 600 Ω resistor is paralleled with the pump's 910 Ω resistor via pin 6. As a result, current flowing in the integrating circuit of the pump (see 5400 description) increases.

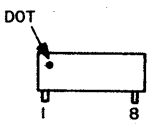


LOGIC SYMBOL

NOTES:

1. Vendor identification is the CDC part number -- 50255100.

2. Package pin configuration:



Rev J
Sheet 5 of 9

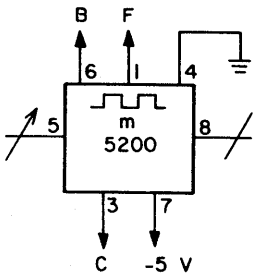
DESCRIPTION

Element 5200 consists of a Schmitt trigger and a current switch. Two 5200 elements are cross-coupled to form a voltage-controlled oscillator (VCO) for the PLO network, as shown in figure 2 on sheet 4. The transistor labellings in figure 2 are merely to aid in the circuit analysis. If the analysis applies to both the left-hand and right-hand elements in the VCO, the left-side transistors are given first, with those for the right side shown in parentheses.

Transistors Q1 and Q2 (Q4, Q5) always assume opposite states, as is typical of a Schmitt-trigger configuration. The ON state of the circuit is considered to be that in which Q1 (Q4) conducts. In this state, output pin 8 is held about two diode-drops above ground (approximately +1.4 V). This positive voltage also appears at the base of Q3 (Q6) which, because its emitter is connected to the negative control voltage from element 5400, turns Q3 (Q6) on. Q3 (Q6) then acts as a switch to sink current from the associated terminal of capacitor C1.

The OFF state of the Schmitt trigger exists when Q1 (Q4) is off and Q2 (Q5) is on. In this state, the output voltage at pin 8 falls to ground and base current through Q2 (Q5), as well as excess collector current through the associated Schottky diode, charges the capacitor.

In the ON state, the relatively heavy current through Q1 (Q4) holds the current-source voltage from element 5800 (as seen at pin 3) to +2.5 V. In the OFF state, Q2 (Q5) draws little current, so pin 3 rises to +4.0 V and is clamped there by the 5300 element. These voltage waveforms are shown in figure 2 and are important to understanding the following circuit analysis, which examines one complete cycle of the VCO.



F: TO FREQUENCY - DETERMINING COMPONENTS.

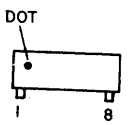
C: TO CONSTANT - CURRENT SOURCE

B: TO BIAS COMPONENTS

LOGIC SYMBOL

NOTES:

1. Vendor identification is the CDC part number -- 50255200.
2. Package pin configuration:



REV L
Sheet 6 of 9

Let's assume that, as shown in figure 3, t1 has transpired and point B is more positive than point C. In this state, Q2 is off, Q1 and Q3 are on, with Q3 sinking current out of point B, while the output at point D rises to +1.4 V. Meanwhile, Q5 and the associated Schottky diode are conducting current into point C, which is held at +3.3 V by the base-emitter drop in Q5 (+4.0 -0.7 = +3.3 V).

As the ramping action passes t2, the charge across C1 actually reverses, making point C more positive than point B. Ramping continues until, at t3, point B reaches the switching point of Q2 (+2.5 -0.7 = +1.8 V). Schmitt trigger action between Q1 and Q2 causes Q2 to rapidly turn on, while Q1 turns off. (With Q2 conducting, the base-emitter junction of Q1 is biased below its conduction level by the emitter-to-collector drop in Q2.)

Meanwhile, the output at point D has fallen from +1.4 V to ground, turning off Q3, while pin 3 has risen sharply from +2.5 V to +4.0 V.

This 1.5-volt rise is reflected through Q2 and the associated Schottky diode to point B.

Because the charge across a capacitor cannot change instantaneously, point C is also raised 1.5 volts -- from +3.3 V to +4.8 V.

As a result, Q5 turns off, causing Q4 and Q6 to conduct. The output at point E now rises to +1.4 V, while Q6 ramps current out of point C.

When point C reaches +1.8 V (at t5), Q5 turns on. The resultant increase in voltage at pin 3 of the right-hand 5200 chip is reflected to point B, cutting off Q2 and turning on Q1 and Q3. The VCO has now passed through one complete cycle.

If the control voltage at pin 5 goes more negative, more current is sinked via Q3 (Q6), causing C1 to reach +1.8 V sooner. Thus, the VCO frequency increases. The opposite condition (a frequency decrease) results if pin 5 goes less negative.

The Schottky diodes enhance the switching time of the circuit by preventing Q1 and Q2 (Q4, Q5) from going into saturation.

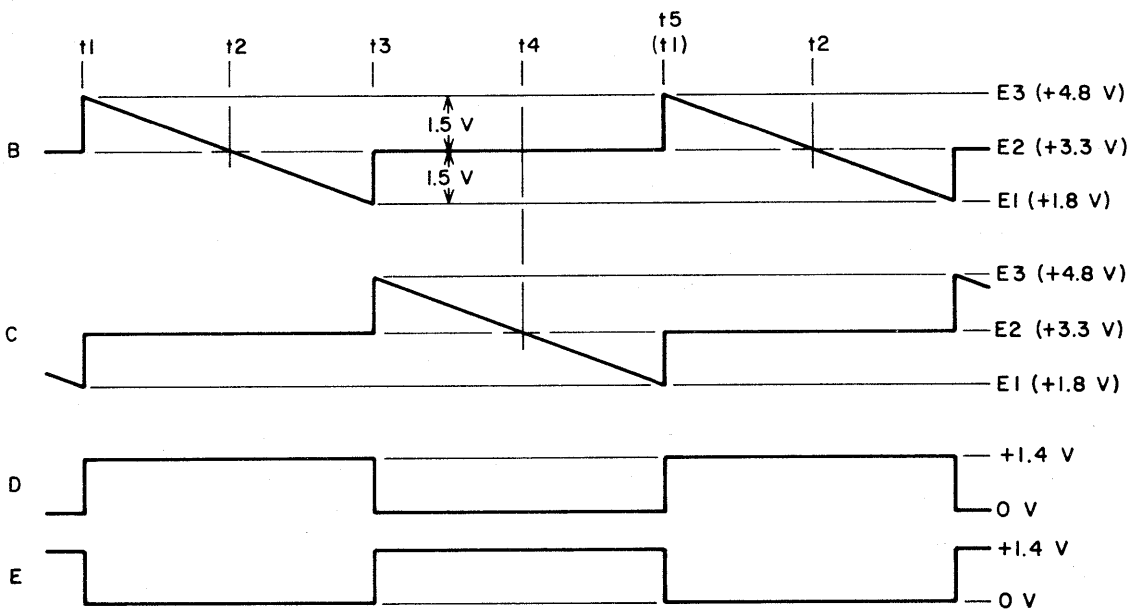


Figure 3. VCO Waveforms

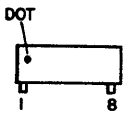
DESCRIPTION

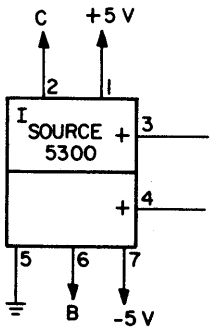
Element 5300 provides a stable current source for the VCO (element 5200), regardless of fluctuations in the logic-power-supply voltage(s). As shown in the schematic diagram of the 5300 element on page 5100-2, this is accomplished by using a zener diode that allows the base potentials of Q1 and Q2 to track voltage variations in the +5 V supply. The external resistor (connected to pin 2) is selected at the time the logic board is fabricated, and provides base drive in accordance with the output current requirement.

NOTES:

1. Vendor identification is the CDC part number -- 50255300.

2. Package pin configuration:





B: TO BIAS COMPONENTS
C: TO CURRENT-ADJUST COMPONENTS

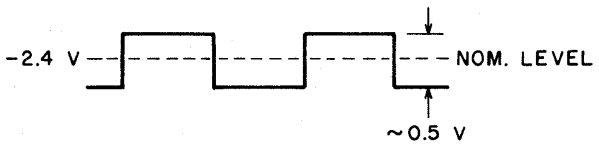
LOGIG SYMBOL

DESCRIPTION

Element 5400, in conjunction with filter R2/C2, is an integrating circuit that raises or lowers its output voltage (V1) in response to the phase relationship between the desired input frequency and that of the associated VCO.

Transistors Q1 and Q2 of element 5400 form a current pump, biased such that Q2 always conducts a current equal to I, regardless of whether or not Q1 is also conducting. When Q1 conducts, it supplies a current equal to 2I, half of which sources Q2 and the other half of which charges filter R2/C2. When Q1 is cut off, the current through Q2 is supplied by the filter.

Current through R2, in charging and discharging C2, causes a small-amplitude digital signal that rides on the nominal level maintained by C2.

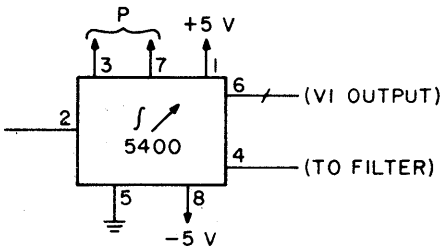


This is called the "proportional" component of the control voltage, V1. The nominal level maintained by C2 is the "integral" component.

The amplitude of the proportional component determines how quickly the PLO can respond to peak shifts in the individual pulses of the desired input frequency. The rate at which the integral component can change determines how quickly the PLO can respond to input frequency variations.

The Comparator FF (top left in the schematic) is set by a positive-going pulse from the desired input frequency. This puts the emitter of Q1 essentially at ground, and Q1 is cut off. The filter now pumps current through Q2, causing the voltage at point A to decrease. This voltage is passed through emitter-follower Q3 to output pin 6. (Q3 and Q4 constitute a buffer that minimizes the effect of output loading at point A.) The voltage at pin 6 (V1) is referred to as the "control voltage" input to the VCO.

When the Comparator FF is cleared by a positive-going pulse from the VCO, Q1 turns on, conducting a current equal to 2I. Because the current through Q2 is limited by the 910-ohm resistor, the excess current (2I-I=I) is pumped into the filter, thereby raising the voltage at point A.



P: TO INPUT-PHASE-DETERMINING COMPONENTS

LOGIC SYMBOL

If the Comparator is in a set state longer than it is reset (Desired Freq > VCO Freq), the voltage at point A becomes less positive, causing the frequency of the VCO to increase. If the Comparator is reset (cleared) longer than it is set (Desired Freq < VCO Freq), the voltage at point A becomes more positive, and the VCO frequency decreases.

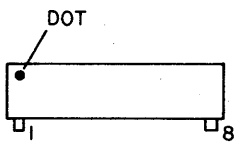
When the Comparator set/reset states reach an equilibrium (square-wave output is symmetrical), the voltage at point A stabilizes.

The Fast Start input to the 5400 (pins 3 and 7) increase the current through Q1 and Q2, as described in the description of the 5100 circuit. The proportional component, as well as the rate of change of the integral component, of the control voltage are thereby increased, reducing the PLO response time and allowing it to lock in more quickly to the desired frequency.

NOTES:

1. Vendor identification is the CDC part number -- 50255400.

2. Package pin configuration.



(PIN 2 UNUSED)

REV L
Sheet 9 of 9

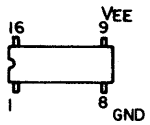
DESCRIPTION

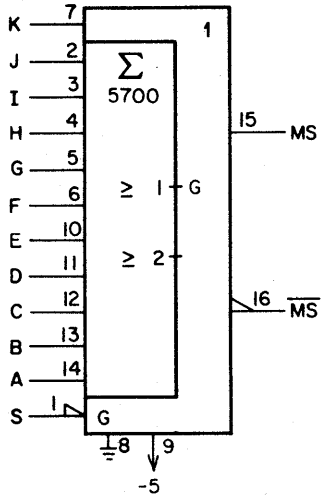
This ECL circuit functions as an 11-input, multiple-select fault detector. Ten of the inputs, A through J, are monitored according to the state of S (mode select) when input K is low: If S is low, one or more of the ten inputs being in the high state will produce a fault indication (MS=H, $\overline{MS}$=L). If S is high, two or more of the ten inputs must be high to give the fault indication. A high on input K produces a fault indication regardless of the state of any of the other inputs, including S.

NOTES:

1. The element identifier is the last four digits of the part number 50255700.

2. Package pin configuration:



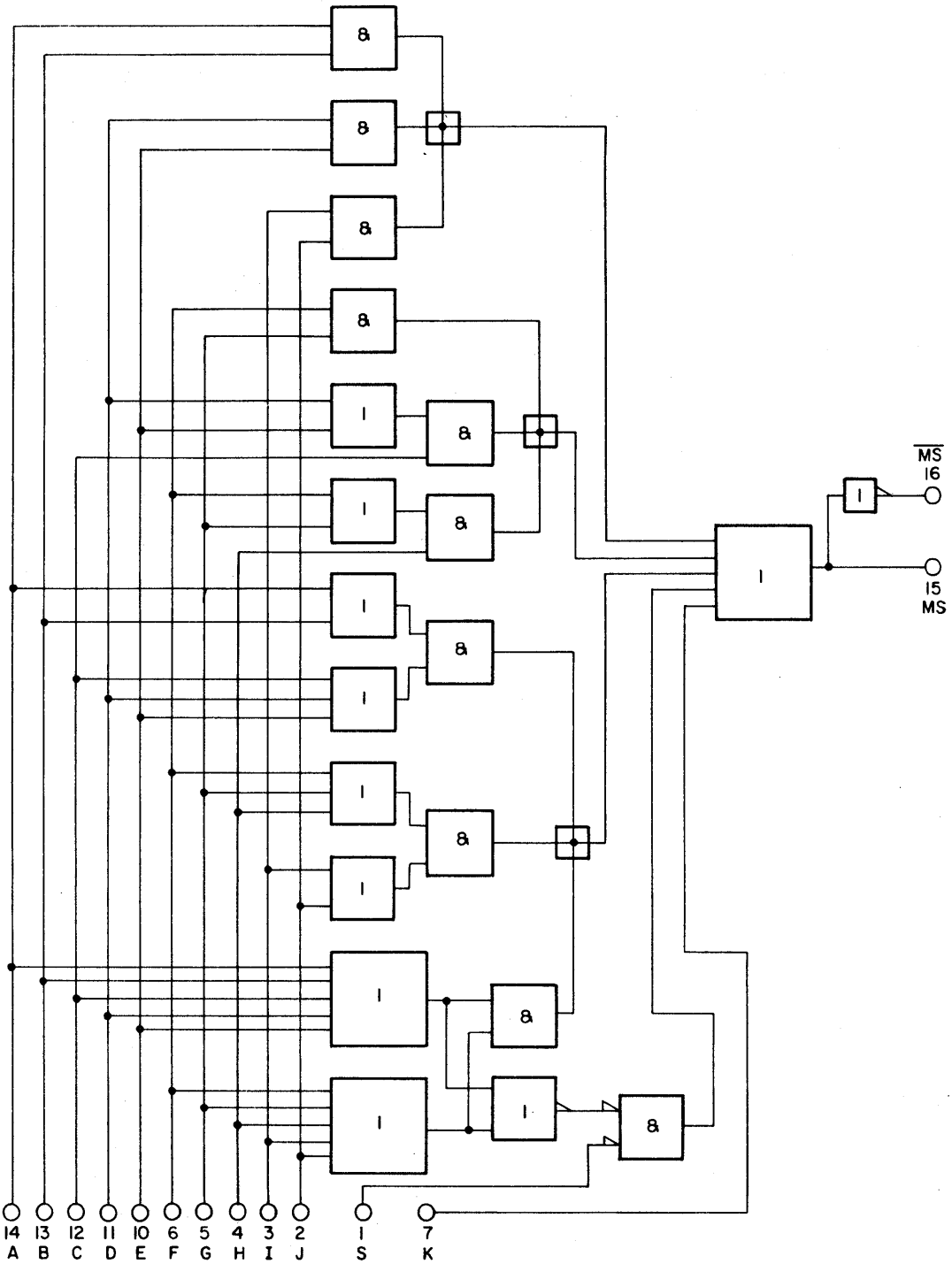


LOGIC SYMBOL

INPUTS			OUTPUTS		OUTPUT CONDITION
S	K	A THRU J	MS	$\overline{MS}$	
X	L	ALL INPUTS LOW	L	H	NO FAULT
H	L	ONLY ONE INPUT HIGH	L	H	NO FAULT
H	L	TWO OR MORE INPUTS HIGH	H	L	FAULT
L	L	ONE OR MORE INPUTS HIGH	H	L	FAULT
X	H	←X→	H	L	FAULT

TRUTH TABLE

5700
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM

5700
Rev J
Sheet 2 of 2

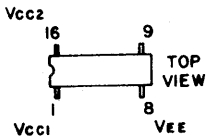
DESCRIPTION

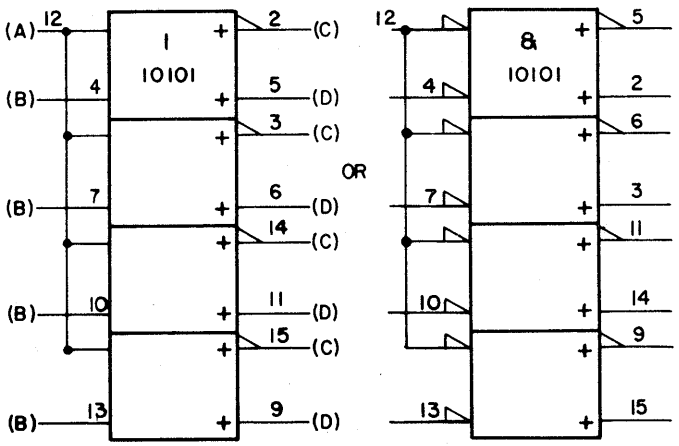
The 10101 is a ECL quad OR/NOR gate with one input from each gate common to pin 12. All sections provide complementary outputs.

NOTES:

1. Vendor identification: MC 10101L

2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
A	B	C	D
0	0	1	0
1	0	0	1
0	1	0	1
1	1	0	1

TRUTH TABLE

10101
Rev J
Sheet 1 of 1

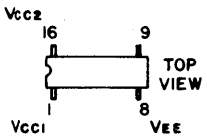
DESCRIPTION

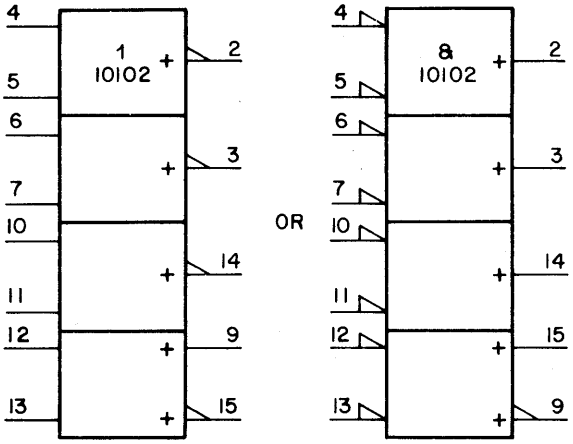
The 10102 is a ECL quad 2-input NOR gate. The last section provides complementary (OR/NOR) outputs.

NOTES:

1. Vendor identification: MC10102L

2. Package pin configuration





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

TRUTH TABLE
(LAST SECTION)

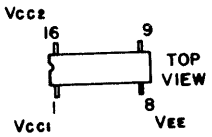
10102
Rev J
Sheet 1 of 1

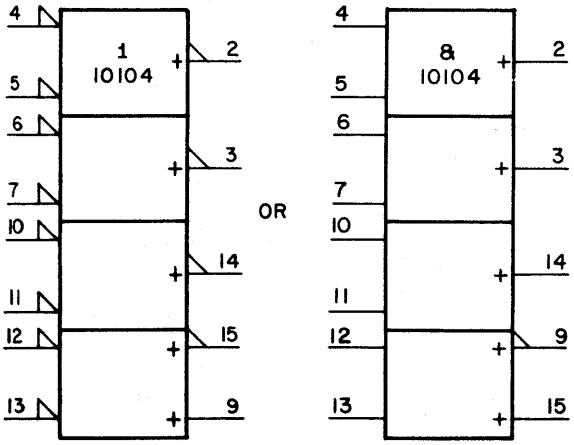
DESCRIPTION

The 10104 is a ECL quad 2-input AND gate. The last section provides complementary (AND/NAND) outputs.

NOTES:

1. Vendor identification: MC10104L
2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

TRUTH TABLE
(LAST SECTION)

10104
Rev J
Sheet 1 of 1

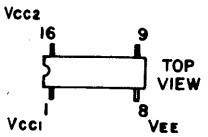
DESCRIPTION

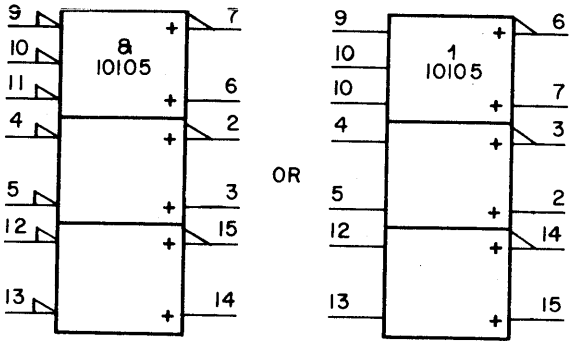
The 10105 is an ECL triple OR/NOR gate with a 3-2-2 input configuration. All sections provide complementary outputs.

NOTES:

1. Vendor identification: MC10105L

2. Package pin configuration.





LOGIC SYMBOL

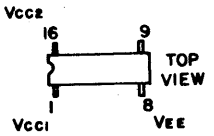
10105
Rev J
Sheet 1 of 1

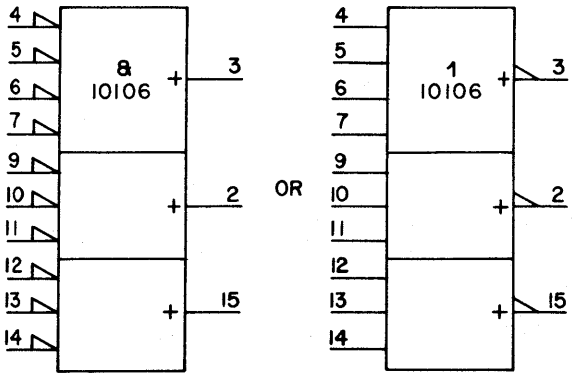
DESCRIPTION

The 10106 is a ECL, triple, 4-3-3-input NOR gate.

NOTES:

1. Vendor identification: MC10106L
2. Package pin configuration.





LOGIC SYMBOL

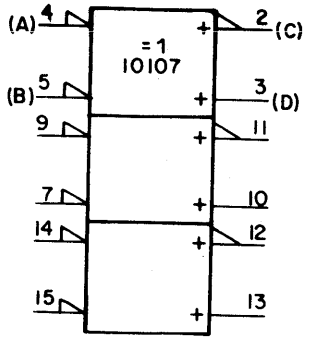
10106
Rev J
Sheet 1 of 1

DESCRIPTION

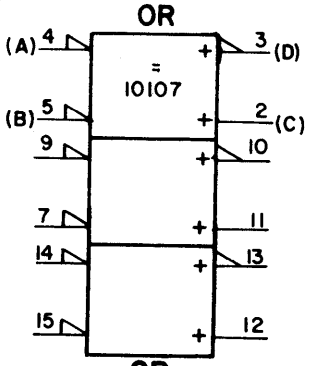
ECL element 10107 is basically a triple, 2-input Exclusive OR gate with complementary outputs that also allow the Exclusive NOR function. In fact, for either high-active or low-active inputs, the circuit offers a choice of X-OR, X-NOR, or Equivalence functions, depending upon which output is considered active. (See truth tables.)

NOTES:

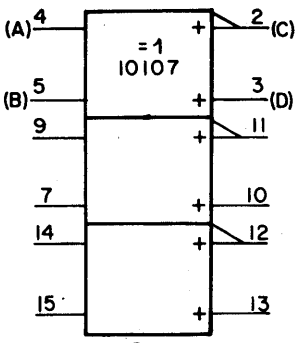
1. Vendor identification: 10107
2. Package pin configuration.



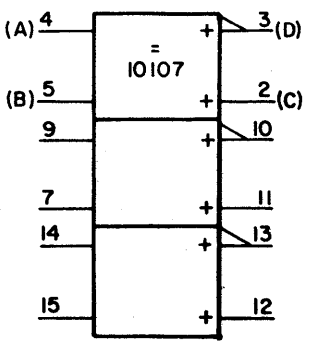
OR



OR



OR



LOGIC SYMBOL

HIGH-ACTIVE TRUTH TABLE

A	B	C	D
L	L	H (1)	L
L	H	L (2)	H (3)
H	L	L (2)	H (3)
H	H	H (1)	L

LOW-ACTIVE TRUTH TABLE

A	B	C	D
L	L	H	L (1)
L	L	L (3)	H (2)
H	L	L (3)	H (2)
H	H	H	L (1)

(1) = EQUIVALENCE
(2) = X-NOR
(3) = X-OR

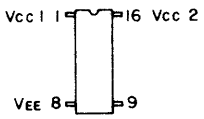
10107
REV L
Sheet 1 of 1

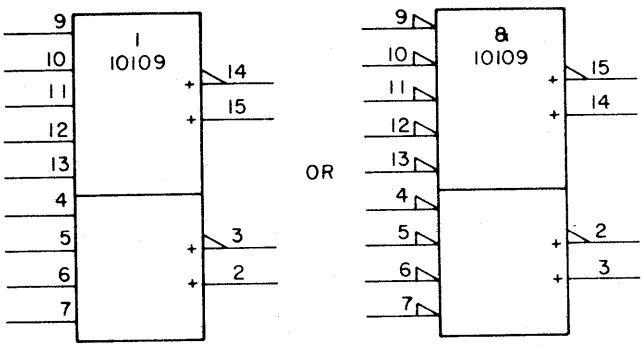
DESCRIPTION

Element 10109 is a dual ECL OR/NOR gate with 4 and 5 inputs, respectively. Complementary outputs are provided from each section.

NOTES

1. Sections may be shown separately.
2. Vendor identification: MC10109
3. Package pin configuration:





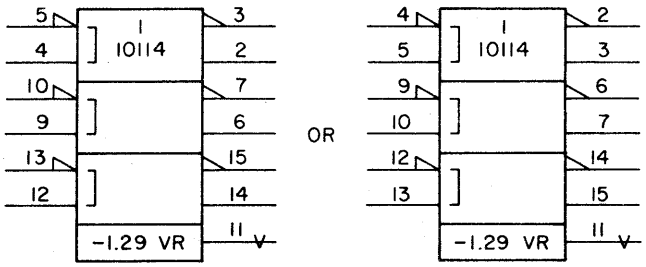
LOGIC SYMBOL

10109
Rev J
Sheet 1 of 1

DESCRIPTION

Element 10114 is an ECL triple line receiver for sensing differential signals. Common-mode noise rejection of 1 volt in either the positive or negative direction allows a large amount of common-mode noise immunity over long lines.

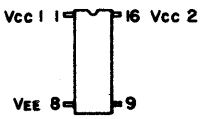
The OR output pins (3,7,15) go low whenever the inputs are left floating. Pin 11 provides a V_{BB} reference that is useful for making the 10114 a Schmitt trigger, allowing single-ended driving of the inputs. The 10114 can also be used as a MOS to ECL interface.



LOGIC SYMBOL

NOTES

1. If sections are shown separately, show the -VR (pin 11) reference in but one section.
2. Vendor identification: MC10114
3. Package pin configuration:

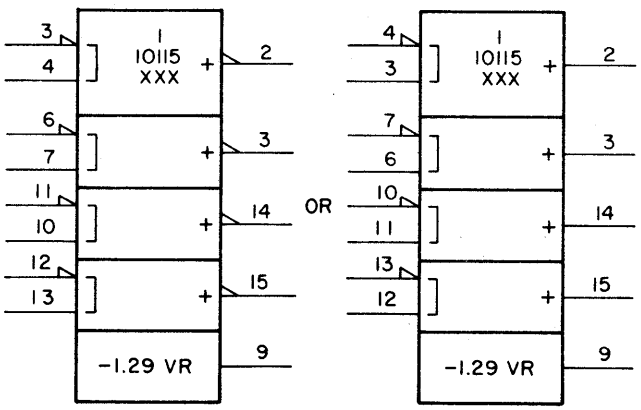


10114
Rev J
Sheet 1 of 1

DESCRIPTION:

ECL element 10115 is a quad differential amplifier designed to sense differential signals over long lines. The base bias supply, V_{BB}, is available at pin 9 when the device is listed as a Schmitt trigger, or in applications where a stable reference voltage is required.

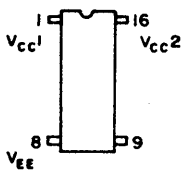
If any section is unused, one of its output pins should be connected to pin 9 to prevent upsetting the current source bias network.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 10115
2. Package pin configuration

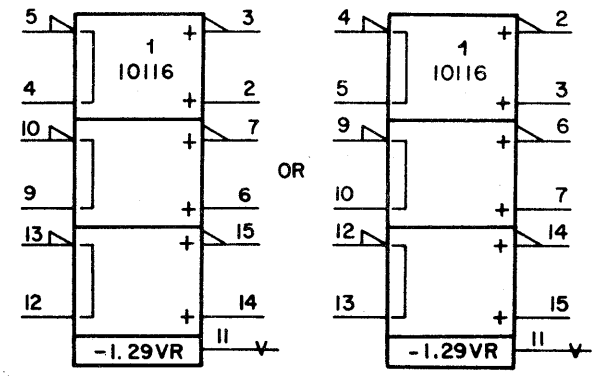


10115
Rev. J
Sheet 1 of 1

DESCRIPTION

The 10116 is a ECL, triple differential line receiver. The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs.

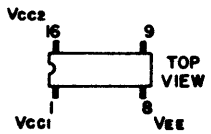
If any amplifier is unused, one input of that amplifier must be tied to V_{BB} (pin 11) to prevent upsetting the current source bias network. In this respect, contrast with element 10114.



LOGIC SYMBOL

NOTES:

1. Vendor identification: MC10116L
2. Package pin configuration.



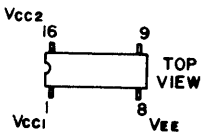
10116
Rev J
Sheet 1 of 1

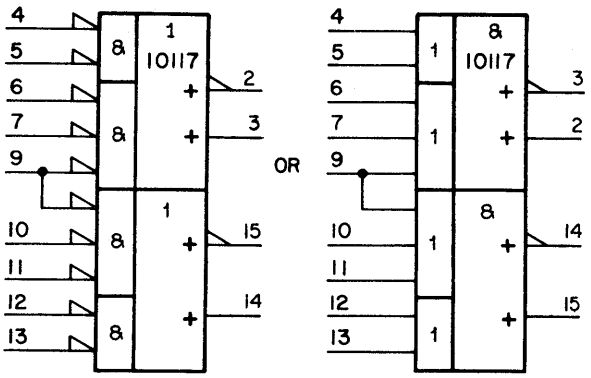
DESCRIPTION

The 10117 is a ECL,dual 2-wide,2-3-input AND-OR / AND-OR-INVERT gate.

NOTES:

1. Vendor identification: MC10117L
2. Package pin configuration:





LOGIC SYMBOL

INPUT PINS					OUTPUT PINS	
4	5	6	7	9	2	3
0	0	X	X	X	0	1
X	X	0	0	0	0	1
ALL OTHER COMBINATIONS					1	0

X = DONT CARE

TRUTH TABLE

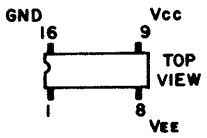
10117
Rev J
Sheet 1 of 1

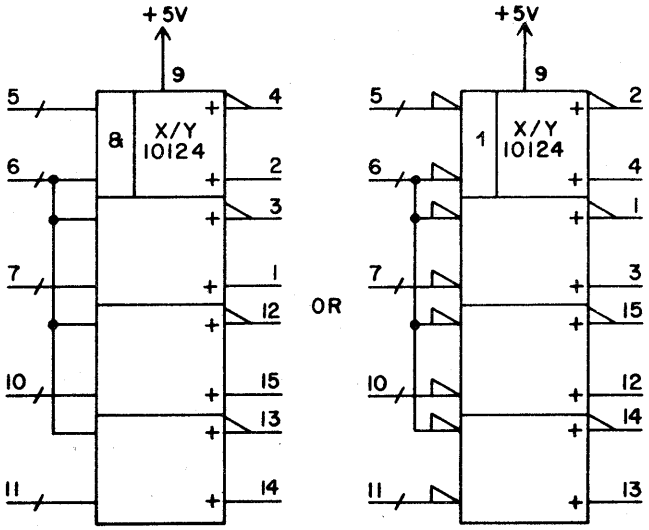
DESCRIPTION

The 10124 is a quad TTL to ECL level translator.

NOTES:

1. Vendor identification: MC10124L
2. Package pin configuration:





LOGIC SYMBOL

10124
Rev J
Sheet 1 of 1

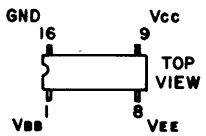
DESCRIPTION

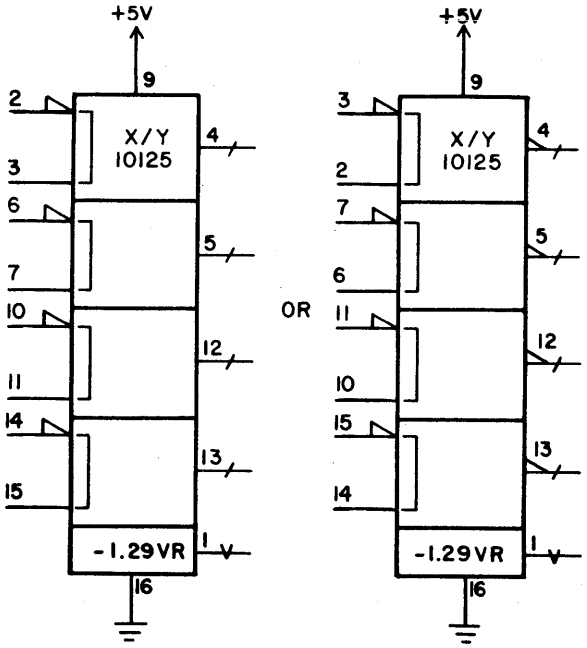
The 10125 is a quad ECL to TTL level translator.

NOTES:

1. Vendor identification: MC10125L

2. Package pin configuration.





LOGIC SYMBOL

10125
Rev J
Sheet 1 of 1

DESCRIPTION

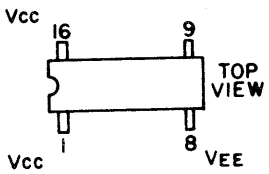
The 10131 is an ECL circuit containing two master-slave, type-D FFs. The FFs are controlled either by the set and reset inputs or by the clock input used in conjunction with the CD (data) input (refer to functional diagram and truth tables).

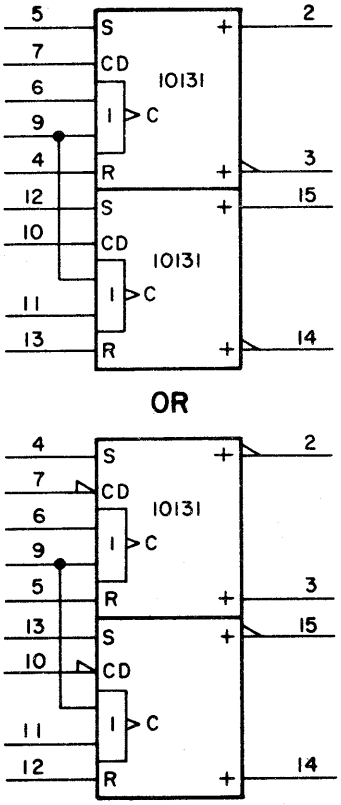
When both the set and reset inputs are low, the FFs are in the clocked mode and their output states change on the positive transition of the clock. The resulting change depends on the information present at the data (CD) input.

The FFs have both common and exclusive clock inputs. The FFs change separately,under control of their exclusive clock inputs, whenever the common clock input is held low. They change states simultaneously, under control of the common clock,whenever the exclusive clock inputs are held low. In either case, the final state of each FF depends on the information present at its data (CD) input at the time of the clock.

NOTES:

1. Vendor identification: MC10131
2. Package pin configuration.





LOGIC SYMBOL

X=DON'T CARE
ND=NOT DEFINED
NC=NO CHANGE

H=LOGICAL ONE
L=LOGICAL ZERO

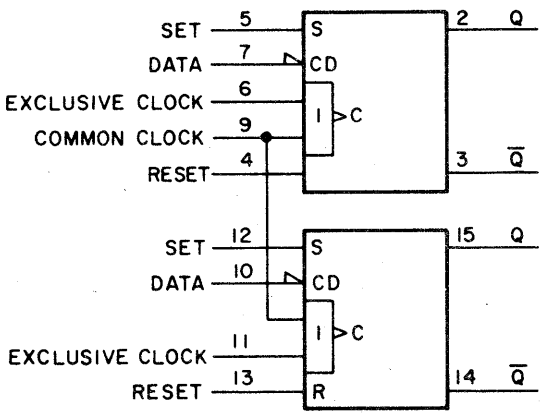
DATA	COMMON CLOCK	EXCLUSIVE CLOCK	Q	$\overline{Q}$
H	L	H	H	L
L	L	H	L	H
H	H	L	H	L
L	H	L	L	H
X	L	L	NC	NC
X	H	H	ND	ND

CLOCKED OPERATION

SET	RESET	Q	$\overline{Q}$
H	L	H	L
L	H	L	H
H	H	ND	ND
L	L	NC	NC

SET/RESET OPERATION

TRUTH TABLES



FUNCTIONAL DIAGRAM

DESCRIPTION:

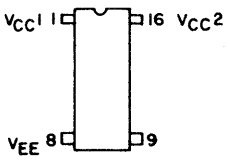
ECL element 10136 is a high-speed, hexadecimal, synchronous up/down counter. Carry Out and Carry In functions are provided to allow cascading two or more counters when more than 4 bits of counting capability is required.

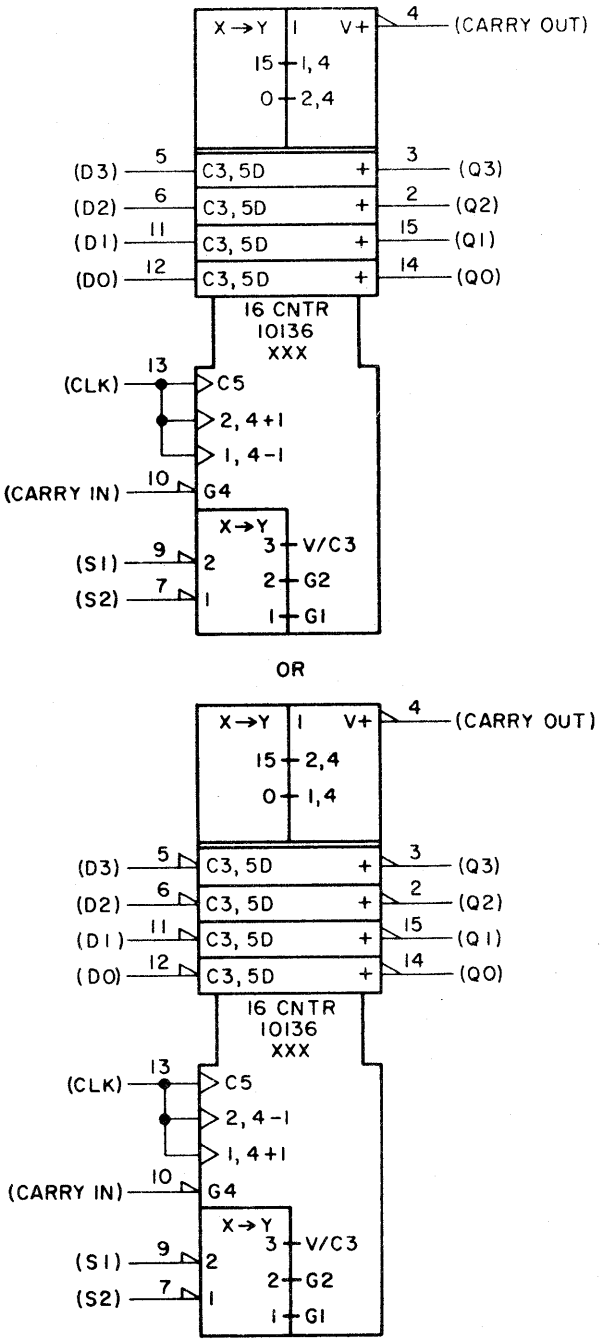
Four operating modes, Load, Count Up, Count Down, and Stop, are provided by decoding signals on select lines S1 and S2, as shown in the Mode Selection table on sheet 2.

(This discussion continues on sheet 3.)

NOTES:

1. Vendor identification: 10136
2. Package pin configuration:





LOGIC SYMBOL

10136
Rev J
Sheet 1 of 3

MODE SELECTION

S1	S2	Operating Mode
L	L	Load (Preset)
L	H	Count Up
H	L	Count Down
H	H	Stop (Hold Count)

TRUTH TABLE FOR HIGH-ACTIVE DATA

	Inputs (Pin No.)								Outputs (Pin No.)				
	S1 (9)	S2 (7)	D3 (5)	D2 (6)	D1 (11)	D0 (12)	Carry in (10)	Clock* (13)	Q3 (3)	Q2 (2)	Q1 (15)	Q0 (14)	Carry out (4)
LOAD	L	L	H	H	L	L	X	H	H	H	L	L	L
CNT UP	L	H	X	X	X	X	L	H	H	H	L	H	H
	L	H	X	X	X	X	L	H	H	H	H	L	H
	L	H	X	X	X	X	L	H	H	H	H	H	L
	L	H	X	X	X	X	H	L	H	H	H	H	H
	L	H	X	X	X	X	H	H	H	H	H	H	H
STOP	H	H	X	X	X	X	X	H	H	H	H	H	H
LOAD	L	L	L	L	H	H	X	H	L	L	H	H	L
CNT DOWN	H	L	X	X	X	X	L	H	L	L	H	L	H
	H	L	X	X	X	X	L	H	L	L	L	H	H
	H	L	X	X	X	X	L	H	L	L	L	L	L
	H	L	X	X	X	X	L	H	H	H	H	H	H

NOTES:

*: A Clock H is defined as the positive-going edge

X: Don't care

During Load, a positive-going clock pulse is needed to gate the preset data into the counter. Clearing the counter is accomplished by tying all data inputs low (or high if low-active data is used), and performing the load function.

During the Load function, the Carry Out signal goes low (active) and the Carry In signal has no effect.

Counting (up or down) is effected on the positive-going edge of the clock, but only if the Carry In signal is low. This is shown in the Truth Table on sheet 2.

The table was constructed for a cascaded counter, the Carry In pulses to which are provided by a lower-order counter. This was done to show the effect of both high and low Carry In signals.

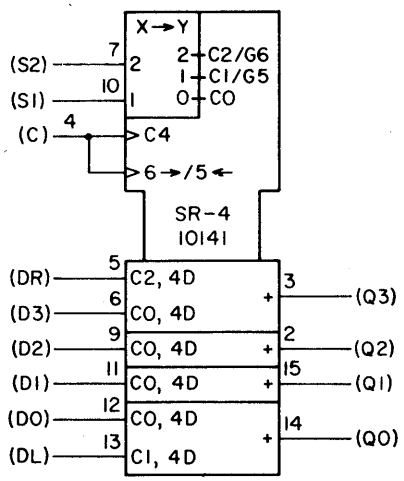
For a single counter, or for the low-order counter in a cascaded network, the Carry In pin is usually left open. In ECL circuits, this provides a constant low-active signal for the input pin.

Note that the truth table represents high-active data. As such, the counter loads 12, counts up to 15, stops, then loads 3 and counts down through 0 to 15.

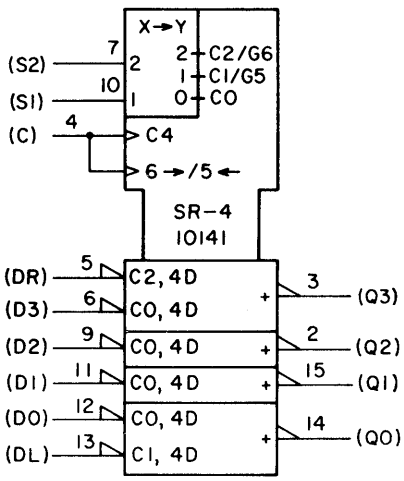
For low active data, merely reverse the count functions: Load 3, count down to 0, stop, load 13, count up through 15 to 0.

DESCRIPTION

The 10141 circuit is an ECL 4-bit universal shift register. Inputs are provided for right shift (DR), left shift (DL), or parallel entry (D0-D3). Outputs are provided from each stage in the register, allowing a choice of parallel or serial output for either shift mode, as well as parallel in/ parallel out operation. Input data is asynchronous, and is shifted to the output on the positive-going edge of the clock pulse (C). Control inputs S1 and S2 determine the operating mode, as given in the truth table. A timing diagram is shown on sheet 2.



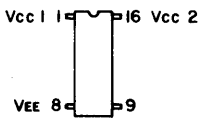
OR



NOTES

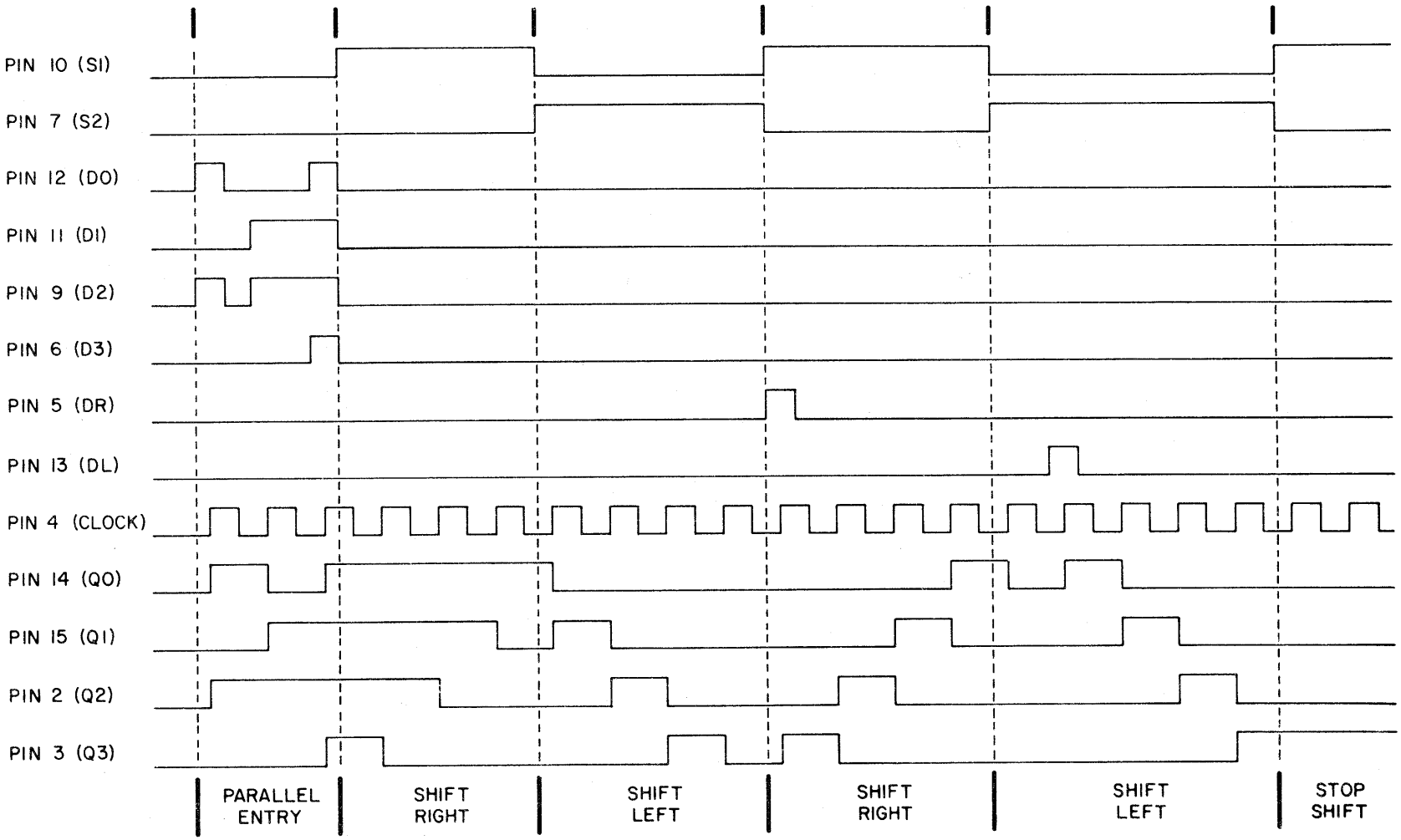
1. Vendor identification: MC10141

2. Package pin configuration:

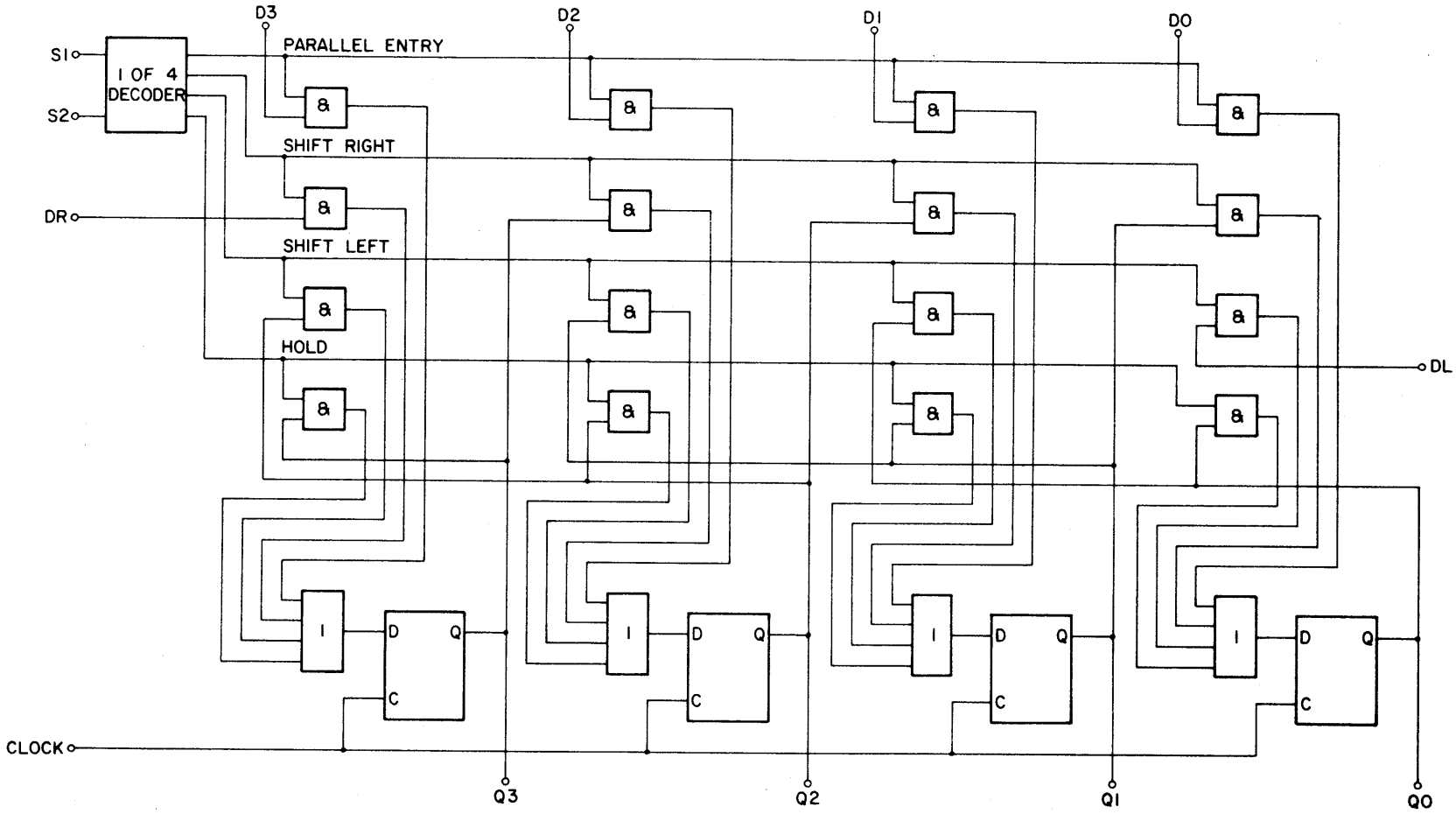


SELECT INPUTS		OPERATING MODE	OUTPUTS			
S2	S1		Q0n+1 (PIN 14)	Q1n+1 (PIN 15)	Q2n+1 (PIN 2)	Q3n+1 (PIN 3)
L	L	PARALLEL ENTRY	D0	D1	D2	D3
L	H	SHIFT LEFT	DL	Q0n	Q1n	Q2n
H	L	SHIFT RIGHT	Q1	Q2n	Q3n	DR
H	H	STOP SHIFT	Q0n	Q1n	Q2n	Q3n

n = BIT TIME BEFORE CLOCK PULSE
n+1 = BIT TIME AFTER CLOCK PULSE



TIMING DIAGRAM



FUNCTIONAL DIAGRAM

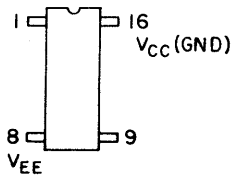
DESCRIPTION

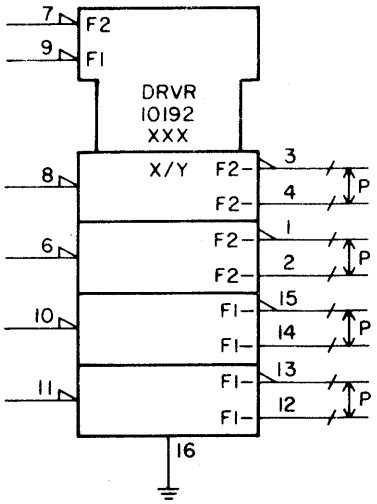
ECL element 10192 is a quad driver with complementary open-collector outputs. Two separate low-active enable inputs each control two of the four sections.

NOTES:

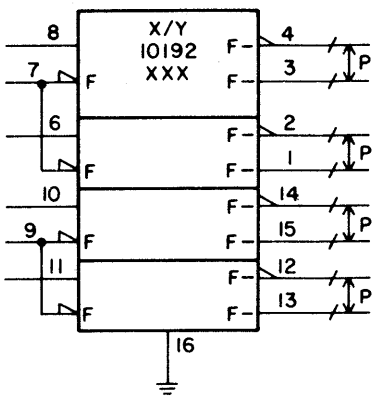
1. Vendor identification: 10192

2. Package pin configuration:





OR



LOGIC SYMBOL

10192
Rev. J
Sheet 1 of 1

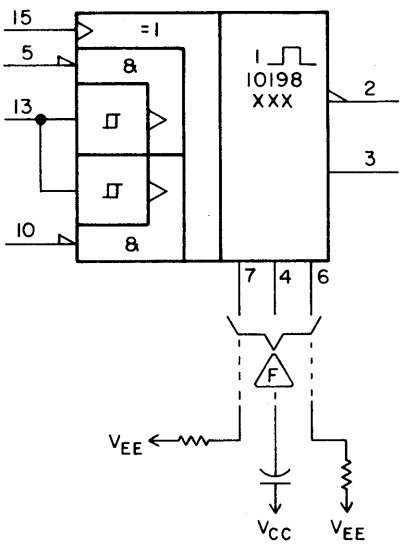
DESCRIPTION:

ECL element 10198 is a monostable, retriggerable multivibrator with two Enables that allow triggering on the positive edge (pin 5) or the negative edge (pin 10), or on both. In addition to the Schmitt-trigger input (pin 13) that operates under control of the two enable inputs, a high-speed input (pin 15) is provided. This input triggers on a rising edge only, and should be used for input pulse widths of 10 ns or less.

Output pulse width is normally controlled by an external resistor and capacitor. The resistor, connected between pin 6 and V_{EE} as shown by the dashed lines in the logic symbol, sets the current that establishes the discharge rate of the capacitor connected between pin 4 and V_{CC}.

Pin 7 is a constant-voltage mode that can also be used as an external timing control. A resistor between pin 7 and V_{EE} then determines the discharge rate of the capacitor.

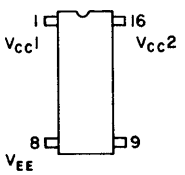
The 10198 can be made non-retriggerable by connecting output pin 3 to the appropriate Enable input.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 10198
2. Package pin configuration:



10198
Rev. J
Sheet 1 of 1

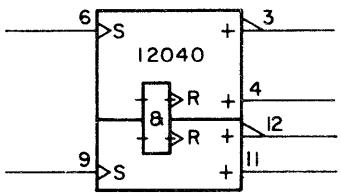
DESCRIPTION

The 12040 is a logic network designed for use as a phase comparator for ECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms.

Operation of the 12040 is best described by assuming that two waveforms of the same frequency, but differing in phase, are applied to input pins 6 and 9 (see timing diagram). If the logic had established by past history that the waveform at pin 6 was leading the waveform at pin 9, the output of the comparator at pin 4 would be a positive pulse whose width is equal to the phase difference; and the output at pin 11 would remain low.

If the logic had established by past history that the waveform at pin 9 was leading the waveform at pin 6, the output of the comparator at pin 11 would be a positive pulse width equal to the phase difference; and the output at pin 4 would remain low.

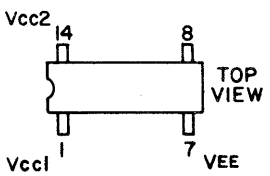
Both outputs for the sample condition are valid, since the determination of lead or lag is dependent on past edge crossings and initial conditions at start-up. A stable phase-locked loop will result from either condition. Phase error information is contained in the output duty cycle - that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the comparator, and by shifting the level to accommodate ECL swings, usable analog information for a voltage-controlled oscillator can be developed.

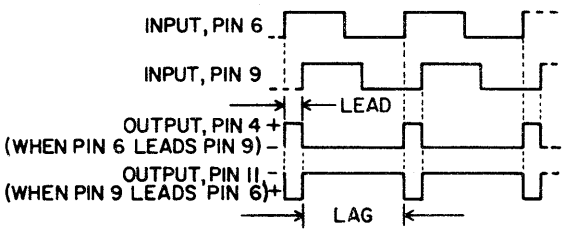


LOGIC SYMBOL

NOTES:

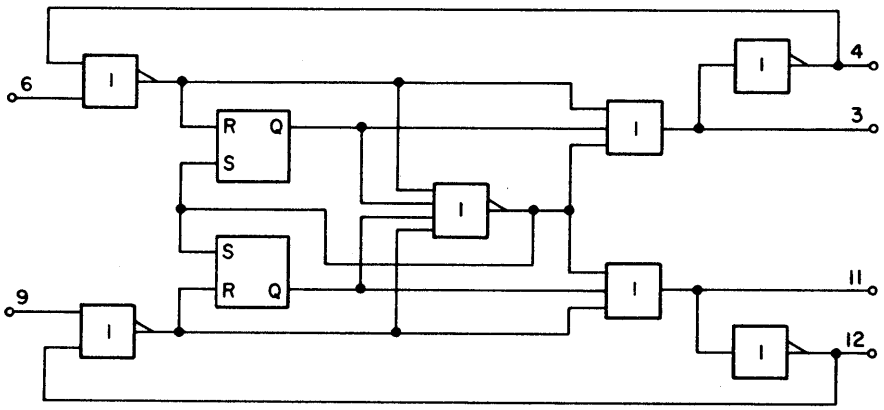
1. Vendor identification: MC12040
2. Package pin identification.





TIMING DIAGRAM

12040
Rev J
Sheet 1 of 2



LOGIC DIAGRAM

12040
Rev J
Sheet 2 of 2

DATA SHEETS ARRANGED BY VENDOR TYPE NUMBER

OR

UNIQUE MICROCIRCUITS IDENTIFIER

DESCRIPTION

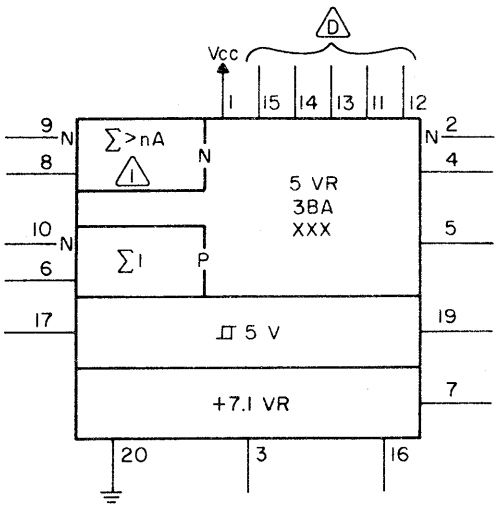
Type 3BA is a hybrid 5-volt regulator encapsulated in a 20-pin package. The package features internal temperature compensation, foldback current limiting, and overvoltage sensing that can be used to drive an external "crowbar" OVP circuit. Output current rating is 150 mA -- determined by the built-in 334 element (LM723C) -- but may be increased by using external pass transistors. By properly connecting Vcc and ground pins, the 3BA may be used to regulate either positive or negative voltages. A typical example of such a dual-voltage application is shown in figure 1.

An electrical schematic of the 3BA, with pins positioned to agree with those in the logic symbol, is given in figure 2. As implied by the logic symbol, the top 334 (IC-1) in figure 1 does the current sensing and voltage regulation. The lower 334 (IC-2) acts as a high-power comparator that provides the Schmitt-trigger function to trip the OVP circuit, most usually by enabling the gate on an (external) SCR.

Source power is applied to pin 1. Pins 16 and 20 are signal and power grounds, respectively. The differential current-sense voltage is applied to pins 8 and 9, while pins 6 and 10 are the regulator inputs. Pins 11-15 are voltage-divider taps that allow selection of the proper level for foldback current protection, which is applied to the Sense inputs. Pin 3 is used for frequency compensation. The functions of the other pins are evident from the logic symbol or figure 2.

A functional diagram of the 334 element is provided in figure 3, and may prove helpful in the circuit descriptions below.

Circuit operation is as follows: The output voltage from pin 4 is applied externally to pin 10, while pin 6 remains at a constant potential because it is tied externally to pin 7 (+7.1 VR) -- usually through a pot that allows precise adjustment of the reference voltage appearing at pin 6. As output current increases, the drop in output voltage causes the differential between pins 6 and 10 to increase. This tells the 334 (IC-1) to provide more base drive to its pass transistor, which raises the voltage at pin 4.

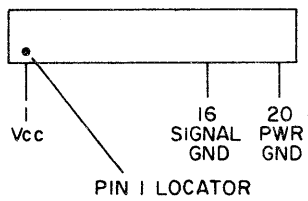


1 INSERT CURRENT-LIMIT VALUE AS DETERMINED BY CONNECTION TO INTERNAL VOLTAGE DIVIDER AT D

LOGIC SYMBOL

NOTES:

1. Element identifier: none
2. Package pin configuration:



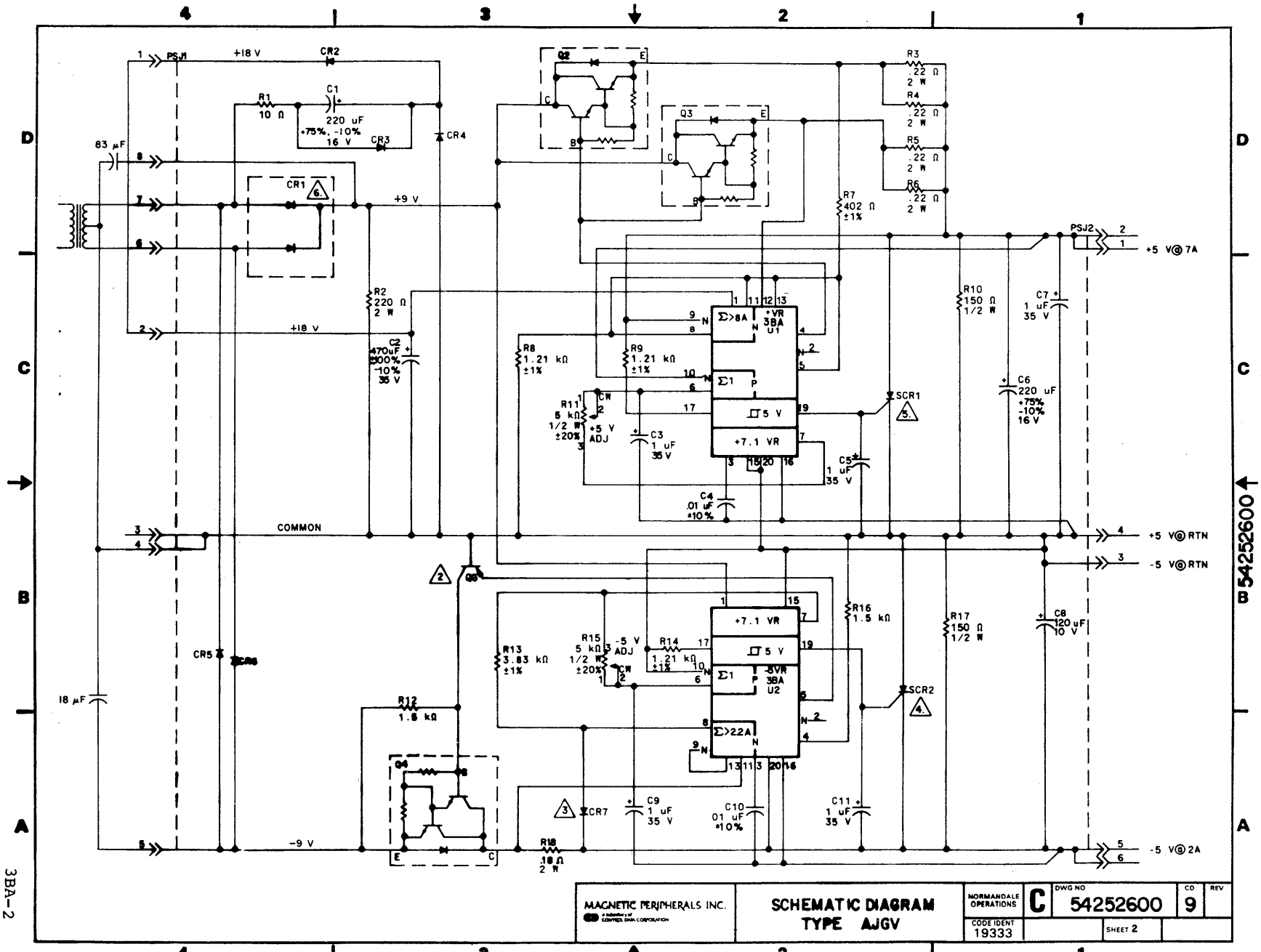
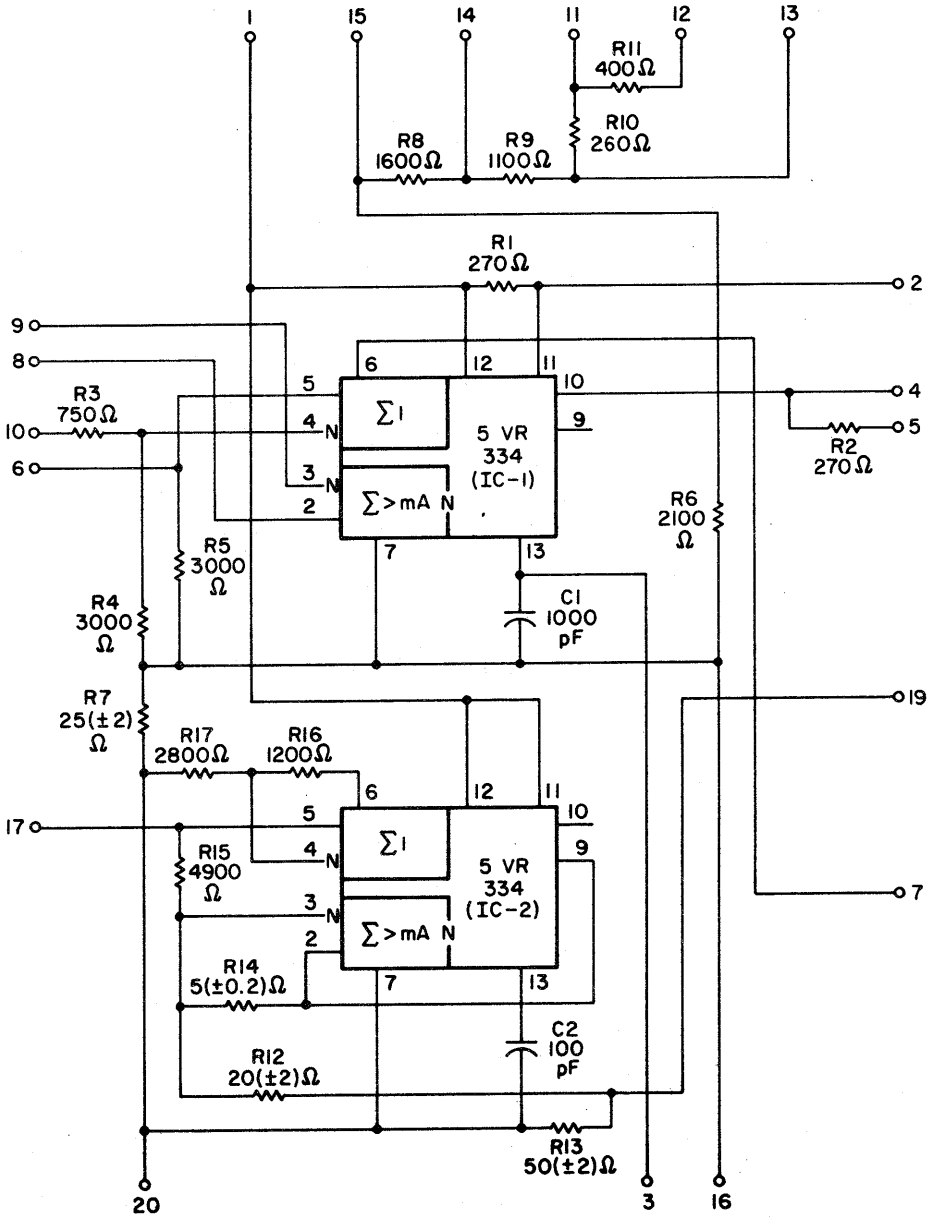


Figure 1. Typical 3BA Application



NOTE: ELEMENT 334 IS DEFINED ELSEWHERE IN THIS MANUAL.

Figure 2. Schematic Diagram, 3BA

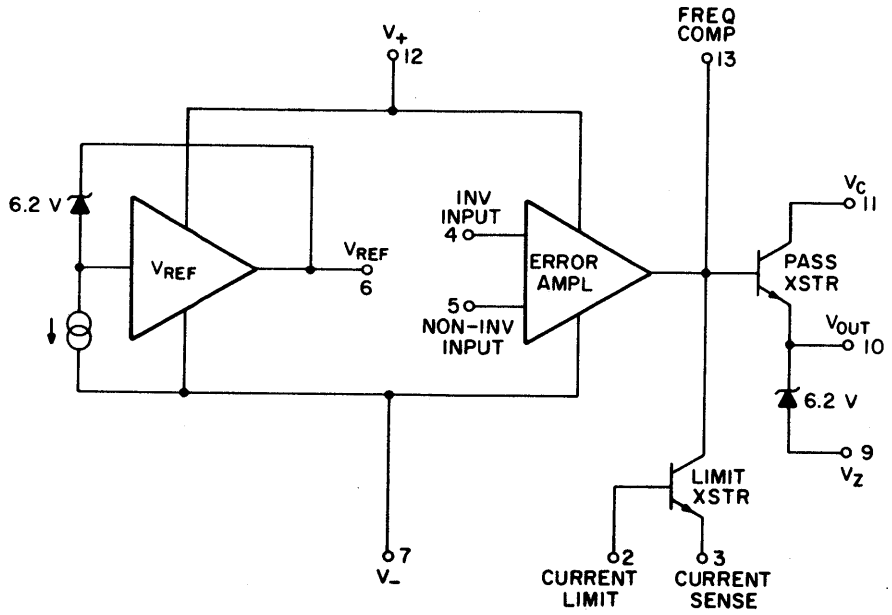


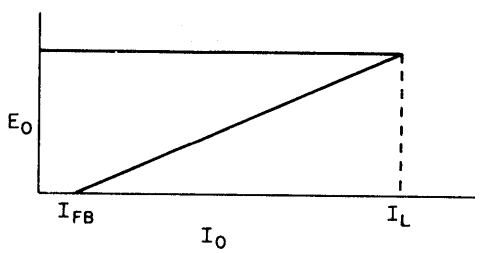
Figure 3. Functional Diagram, Element 334

Meanwhile, the current-sense inputs have been monitoring the load current via an external sense resistor. One of these inputs reflects the increased load, while the other provides a current-limit point as determined by its connection to the foldback resistor network (pins 11-15). Which input is which depends upon whether the 3BA is being used as a positive- or negative-voltage regulator. For this discussion, let's assume positive-voltage regulation, which makes pin 9 the Sense input and pin 8 the Limit input.

With no load current flowing, the connections are such that pin 9 will be positive with respect to pin 8, growing less positive as the load current increases. The limit point is reached when pin 9 goes 0.7 V negative with respect to pin 8. (This is the base-emitter drop across the Limit transistor shown in figure 3). At this point the regulation function, normally performed by pins 6 and 10, is superseded by the current-limit function of pins 8 and 9. The more pin 9 goes negative (with respect to pin 8), the less drive is supplied to the 334's pass transistor, with a consequent reduction in both output current and output voltage.

The foldback function just described is illustrated in the following graph, which plots output current (I_O) against output voltage (E_O). The current-limit point is given by I_L, whereas I_{FB} represents the foldback current with a direct short across the regulator outputs.

The OVP circuit uses IC-2, as mentioned earlier: Pin 6 of IC-2 provides a +6.95-7.35 V reference which, via R16 and R17 to power ground (3BA pin 20), places pin 4 of IC-2 at about +4.9 V. Pin 17 of the 3BA is connected to the regulated output through an external resistor whose valve places the normal operating point of pin 5 (of IC-2) at about 0.5 V negative with respect



to pin 4. As a result, the IC's pass transistor is turned off.

If the output voltage goes high enough to make pin 5 equal to or more positive than pin 4, base drive will be provided to the pass transistor in IC-2, making E_{pin1}-6.2 V available at pin 9 of IC-2. Current now flows to ground (3BA pin 20) through R14, R12, and R13. The value of this current must be such that, as it flows through R14, it will not overcome the base-emitter drop in the current-limit transistor of IC-2. This value is a maximum of 136 mA. Pin 19, therefore, goes to +6.8 V (50 Ω · 0.136A).

As stated previously, pin 19 is usually connected to the gate of an SCR that shunts the load. The SCR turns on, shorting the regulated output, with the result that 3BA pin 17 drops to ground. This pulls down pin 5 of IC-2, shutting off the current source that developed the voltage at pin 19. Removing the trigger voltage, however, has no effect on the SCR which, once it has fired, continues to conduct. (Current through the SCR at this point is I_{FB}, generally 10% of the rated output current).

The shut-down state just described will persist until the SCR is reset, usually by removing the source voltage from pin 1 of the 3B4.

DESCRIPTION

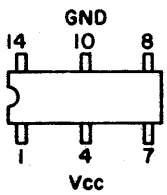
Element 426 is a dual 3-input AND gate that may serve as a pulse shaper or a "1's" delay. The shaping function results from the inherent hysteresis of the Schmitt-trigger circuit. Note the threshold levels, which are a part of the pulse-shaper symbol.

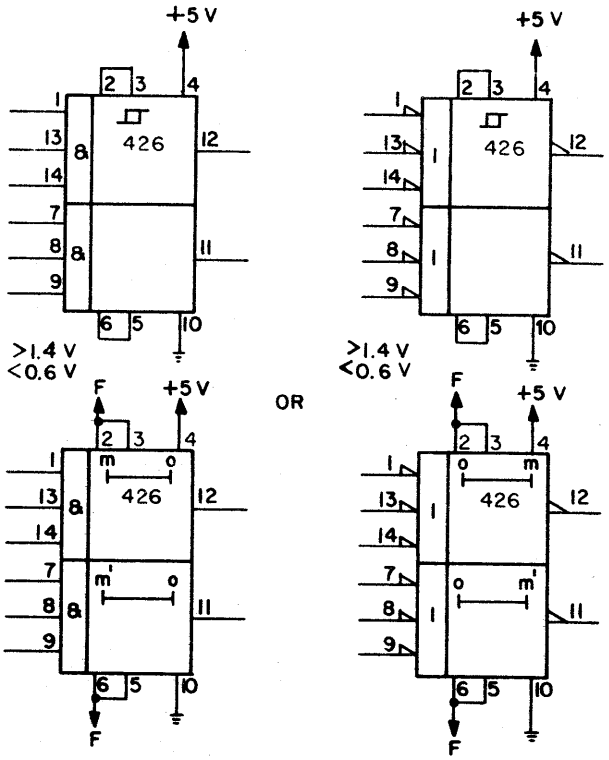
As a "1's" delay, a high input signal appears at the output after a delay period determined by the RC network. As shown by the timing diagram, the falling H-to-L) edge of the input signal is not delayed; if the signal drops before the expiration of the delay period, the output remains low.

The 426 and the SNG83 are identical. The SNG82 differs in that it has a fan-out capability of 12, as opposed to 6 for the 426/ SNG83.

NOTES:

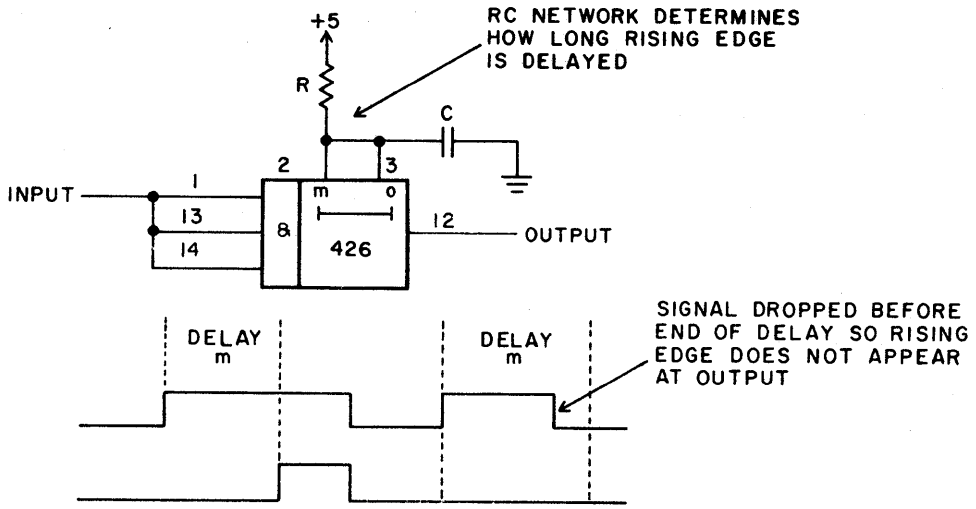
1. Replace m and m' with appropriate delay periods.
2. Element identifier: none
3. Package pin configuration:





LOGIC SYMBOLS

426
Rev J
Sheet 1 of 2



FUNCTIONAL DIAGRAM
(FIRST SECTION)

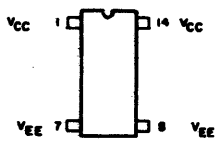
DESCRIPTION

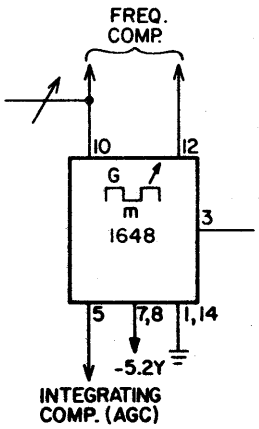
The 1648 circuit is an ECL voltage-controlled oscillator that may be operated from a +5 Vdc or a -5.2 Vdc supply, depending upon system requirements. The external tank circuit connected between pins 10 and 12 may also contain a varactor diode to provide a voltage-variable input for the VCO.

Maximum output frequency (typical) is 225 MHz.

NOTES:

1. Element identifier: none
2. Package pin configuration:





Replace 'm' with frequency or frequency range

LOGIC SYMBOL

1648
Rev J
Sheet 1 of 1

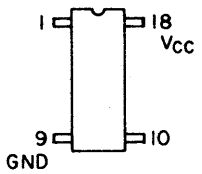
DESCRIPTION

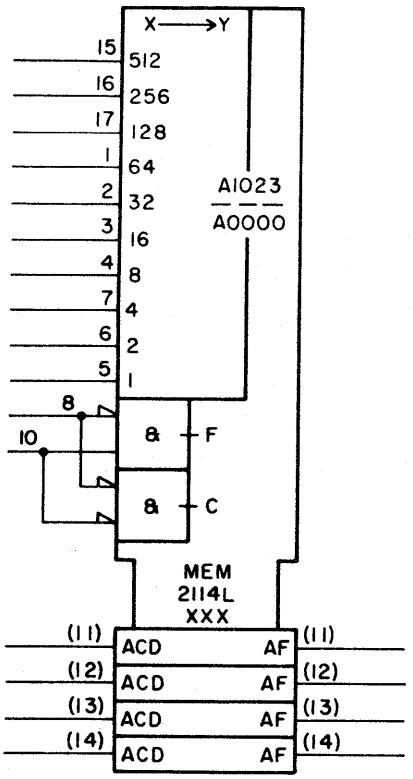
Type 2114L is a 4096-bit static Random Access Memory (RAM) with non-destructive readout. The memory is organized as 1024 4-bit words, has a maximum access time of 450 nanoseconds, and requires neither clocking nor refreshing.

With chip enable (pin 8) low, reading is performed when pin 10 is high, and writing is performed when pin 10 is low.

NOTES:

1. Element identifier: none
2. Package pin configuration:





LOGIC SYMBOL

2114L
Rev. J
Sheet 1 of 1

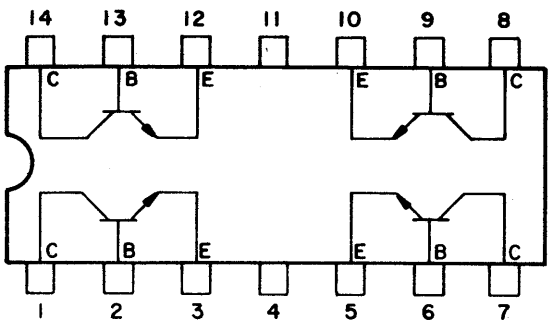
DESCRIPTION

The 2222 is an array of four n-p-n general-purpose silicon transistors in a dual in-line package. Continuous collector current rating is 500 mAdc. Maximum voltage ratings are:

Collector-Emitter	(Vce)	40V
Collector-Base	(Vcb)	60V
Emitter-Base	(Veb)	5.0V

NOTES:

1. **Element identifier: None**
2. **Package pin configuration is shown below.**



2222
Rev K
Sheet 1 of 1

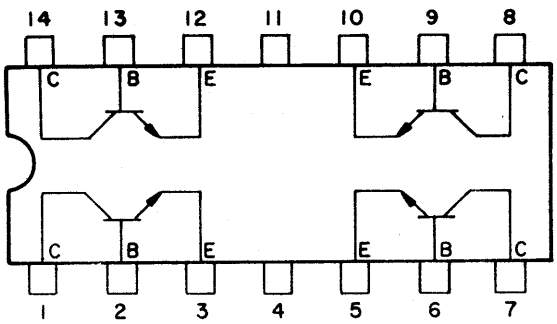
DESCRIPTION

The 2369 is an array of four n-p-n silicon transistors designed for high-speed switching of collector currents up to 500 mAdc (peak). Typical turn on/turn off speeds are 9ns and 15 ns and 15 ns, respectively. Maximum voltage ratings are:

Collector-Emitter	(Vce)	15V
Collector-Base	(Vcb)	40V
Emitter-Base	(Veb)	4.5V

NOTES:

1. **Element identifier: None**
2. **Package pin configuration is shown below.**



DESCRIPTION

Type 2716 is a 16,384-bit Erasable, Programmable Read Only Memory (EPROM) with three-state outputs. The memory is organized as 2048 words of 8 bits each. Maximum acess time is 450 ns.

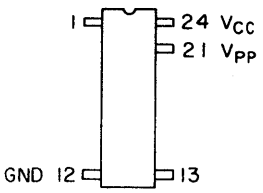
The 2716 incorporates six modes of operation; these are contingent on the states of the chip select input (pin 20), the program input (pin 18), and the +Vpp voltage applied to pin 21. Comments below augment the table data when what happens during a mode selection is not self evident.

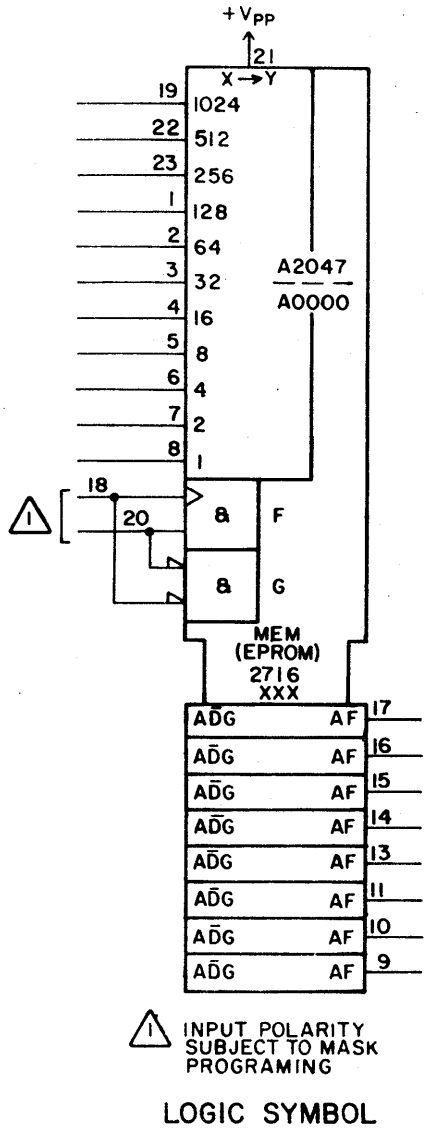
Power Down

This mode reduces by 75% the drain on the +5 V supply caused by the 2716 -- from 525 mW to 132 mW. Note that all data outputs go H_1-Z.

NOTES:

1. Element identifier: none
2. Package pin configuration:





LOGIC SYMBOL

2716
REV L
Sheet 1 of 2

2716 MODE SELECTION

Mode	Input Function (PIN)				Outputs (Pins 9-11, 13-17)
	PRGM (18)	CHIP SEL (20)	Vpp (21)	Vcc (24)	
Read	L	L	+5 V	+5 V	RDM Data
Deselect	Don't care	H	+5 V	+5 V	Hi-Z
Power Down	H	Don't care	+5 V	+5 V	Hi-Z
Program	L to H ⌐	H	+25 V	+5 V	Data In
Program Verify	L	L	+25 V	+5 V	ROM Data
Program Inhibit	L	H	+25 V	+5 V	Hi-Z

PROGRAM

Initially, or when erased by ultraviolet light, all 16,384 outputs are High, so Lows must be programmed. A Low cannot be re-programmed to a High; rather, the entire EPROM must be erased and then programmed for the new data. The "program data", of course, may contain both Highs and Lows. The procedure follows:

1. Apply +25 V to Vpp (pin 21)
2. Bring Chip Select (pin 20) High.
3. Apply selected address to address pins
4. Apply desired data (8 bits) to Data pins
5. Hit pin 18 with a 50-ms high-going TTL-level pulse. (Maximum pulse width is 55 ms).

The next address/data selection may be made as soon as pin 18 goes low. If two or more 2716s are paralleled (for words wider than 8 bits), the entire word can be entered by simultaneously putting all EPROMs in the Program mode. See more about this under Program Inhibit, below.

PROGRAM VERIFY

To verify that the data entered at a given address was written correctly, simply drop Chip Select (pin 20) after the program pulse (pin 18) has gone low. (The data-entry signals, of course, must first be disconnected). Note that verification may be performed even though Vpp remains at +25 V.

PROGRAM INHIBIT

The inhibit mode makes it possible to selectively program several EPROMs that are connected in parallel. The mode is useful when the new word to be programmed does not require changing the bits in all of the paralleled EPROMs, or if, when all inputs to be programmed with similar data are ORed together, the load exceeds the fan-out capacity of the source driving the inputs. In either case, all similar data inputs and all Chip Select pins may still be tied together, with only the Program inputs being grouped according to the manner in which the 2716s are to be programmed.

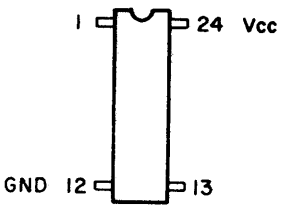
DESCRIPTION

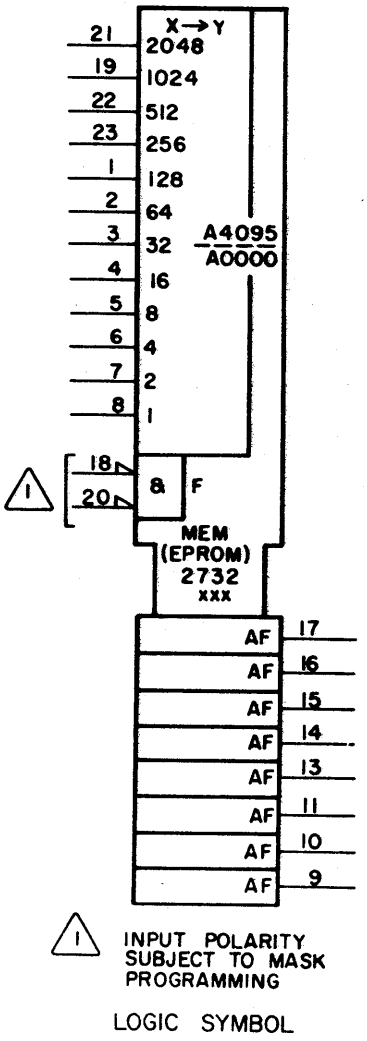
The 2732 is a 32,768-bit Erasable, Programmable, Read-Only Memory (EPROM) with three-state outputs. The memory is organized as 4096 words of 8 bits each. Assuming that the address lines are stable and that a low level is present at the low-active Chip Enable pin (18), data is available at the outputs a maximum of 120 ns after the low-active Output Enable pin (20) goes low.

The 2732 incorporates five modes of operation that are contingent upon the levels applied to pins 18 and 20 as shown in the Mode Selection table. Comments on sheet 2 explain mode-selection contingencies that are not evident from the table.

NOTES:

1. Element identifier: None
2. Package pin configuration:





LOGIC SYMBOL

2732 MODE SELECTION

Mode	Input Function (pin)			Outputs (pins 9-11, 13-17)
	Chip Enable (18)	Output Enable (20)	Vcc (24)	
Read	L	L	+5V	ROM Data
Standby	H	Don't Care	+5V	Hi-Z
Program	⌐‾‾‾‾‾¬	+25V	+5V	Data In
Program Verify	L	L	+5V	ROM Data
Program Inhibit	H	+25V	+5V	Hi-Z

STANDBY

The standby mode reduces current consumption by 85% -- from 160 mA to 25 mA.

PROGRAM

Initially, or when having been erased by ultraviolet light, all 32,768 bits are high; this means that lows have to be programmed. A Low cannot be reprogrammed to a High; rather the entire chip must be erased and then programmed with new data. The program data, of course, may contain both Highs and Lows. The procedure follows.

1. Apply selected address to address lines (TTL level).
2. Apply new data to input pins (TTL level).
3. Apply +25V (Vpp) to Output Enable pin 20.
4. Apply low-going TTL-level pulse of 50 ms (55ms, max) to Chip Enable pin 18.

PROGRAM VERIFY

To verify that the data was written correctly, drop pin 20 from +25V to a TTL low level and, a minimum of 2μs later, apply a TTL low to pin 18.

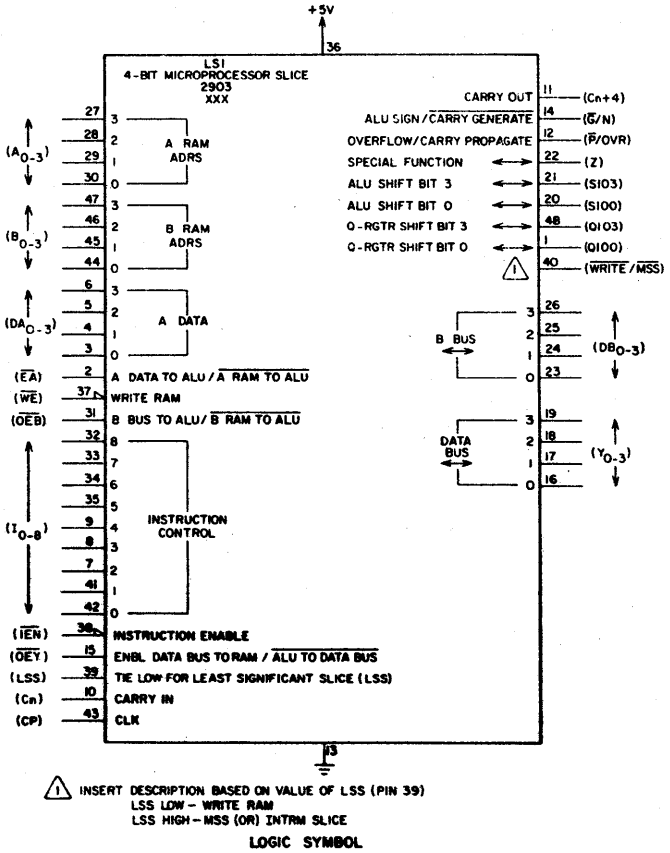
PROGRAM INHIBIT

This feature is useful when programming multiple EPROMs with different data in order to provide word lengths greater than 8 bits. The address, data, and output enable lines can be connected in parallel to all 2732s; only the Chip Enable pins (18) must be connected individually. To program a given 2732, follow the procedure listed above, making sure that the Chip Enable pins of the other EPROMs are held high.

DESCRIPTION

The 2903 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The nine-bit microinstruction selects the ALU sources, function, and destination. The 2903 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

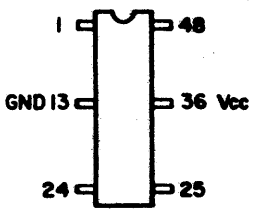
All data paths within the device are four bits wide. As shown in the block diagram, (figure 1), the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder. Vendor pin identifications are shown in parentheses outside the logic symbol.



NOTES:

1. Element identification: None

2. Package pin configuration



PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is Low, data at the Y I/O port is written into the RAM when the CP input is Low. When $\overline{WE}$ is High, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the ALU operand sources; DA_0 is the least significant bit.

$\overline{EA}$ A control input which, when High, selects DA_{0-3} and, when Low, selects RAM output A as the ALU R operand.

DB_{0-3} A four-bit external data input/output. Under control of the OE_B input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when Low, enables RAM output B onto the DB_{0-3} lines and, when High, disables the RAM output B three-state buffers.

C_n The carry-in input to the 2903 ALU.

I_{0-8} The nine instruction inputs used to select the operation to be performed.

$\overline{IEN}$ The instruction enable input which, when Low, enables the $\overline{WRITE}$ output and allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is High, the WRITE output is forced High and the Q Register and Sign Compare flip-flop are in the hold mode.

C_{n+4} This output generally indicates the carry-out of the ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}/N$ A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}/OVR$ A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when High, generally indicates the Y_{0-3} outputs are all Low. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3, Bidirectional serial shift inputs/-outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/-outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied Low, programs the chip to act as the least significant slice (LSS) of a 2903 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When LSS is tied High, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

$\overline{WRITE}/\overline{MSS}$ When LSS is tied Low, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is Low when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied High, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it High programs the chip to operate as an intermediate slice (IS) and tying it Low programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the 2903. Under control of the OE_Y input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when Low, enables the ALU shifter output data onto the Y_{0-3} lines and, when High, disables the Y_{0-3} three-state output buffers.

CP The clock input to the 2903. The Q Register and Sign Compare flip-flop are clocked on the Low-to-High transition of the CO signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is Low.

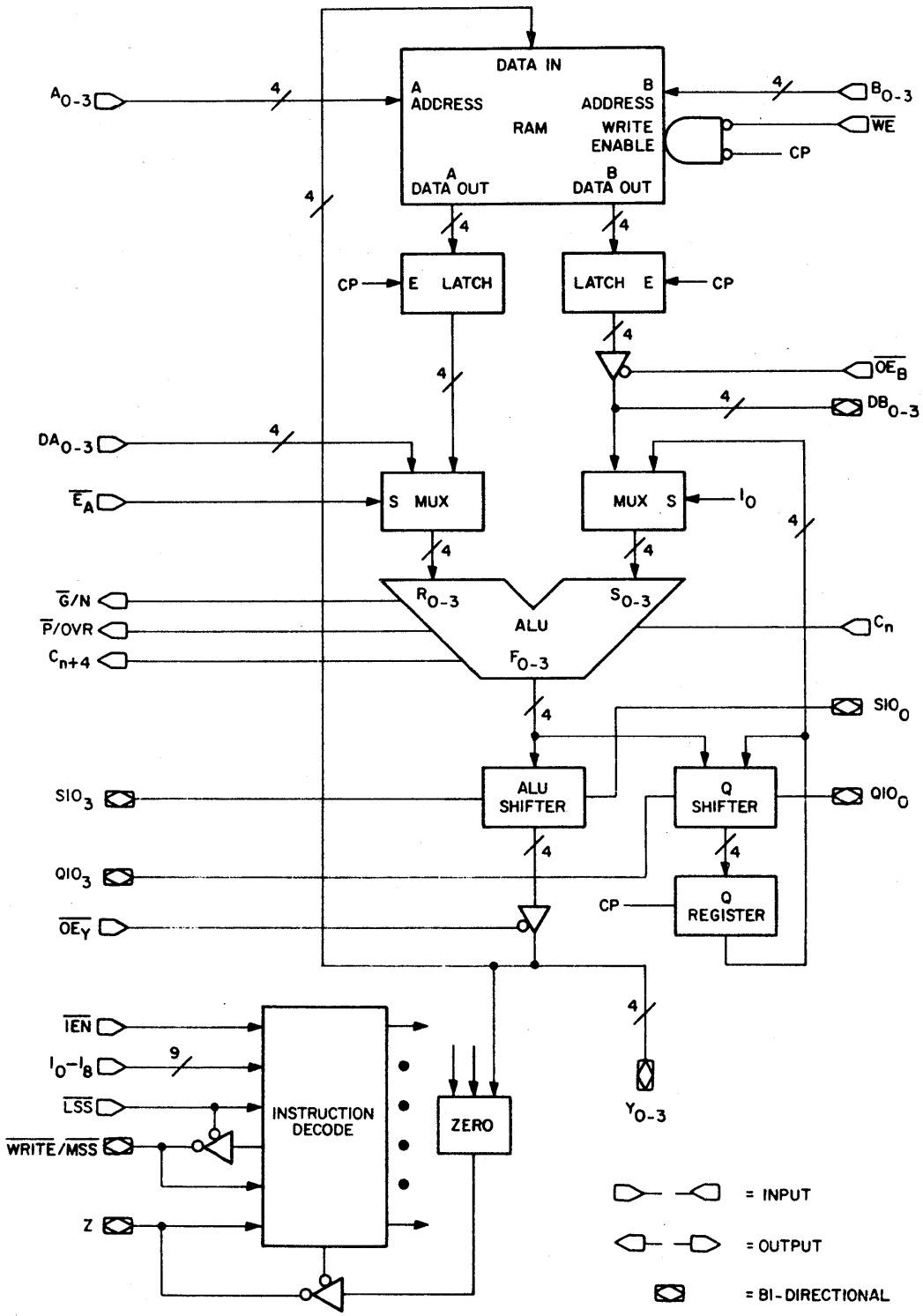


Figure 1. 2903 Block Diagram

ARCHITECTURE OF THE 2903

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is High and they hold the RAM output data when CP is Low. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the DB I/O port.

External data at the Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is Low and the clock input, CP, is Low. The A address is not used when writing into RAM.

Arithmetic Logic Unit

The ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E}_A$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the $\overline{E}_A$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are Low, the 2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the 2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

2903's may be cascaded in either a ripple carry or lookahead carry fashion. When a number of 2903's are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the 2903 and are available as outputs of the least significant and intermediate slices.

TABLE 1. ALU OPERAND SOURCES

$\overline{E}_A$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	Ll	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU Functions	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = S Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = R Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	F_i = R_i AND S_i	
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i	
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i	
H	H	L	L	C	F_i = R_i AND S_i	
H	H	L	H	D	F_i = R_i NOR S_i	
H	H	H	L	E	F_i = R_i NAND S_i	
H	H	H	H	F	F_i = R_i OR S_i	

L = LOW H = HIGH i = 0 to 3

The 2903 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active High. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds

the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multi-purpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the 2903 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure 2). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

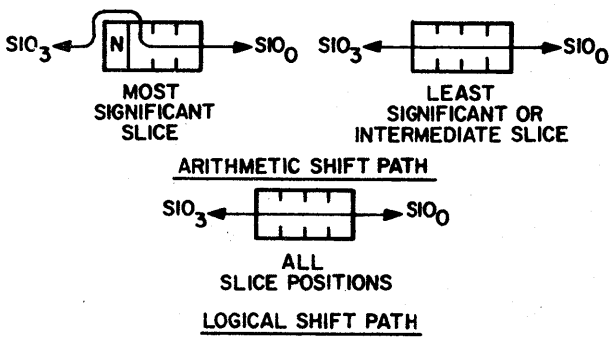


Figure 2. Shift Paths

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/-checker is designed into the shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the applications section for a more detailed description of the sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the shifter performs for each. When the 2903 executes instructions other than the nine special functions, the operation is determined by instruction bits $I_8I_7I_6I_5$. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the Low-to-High transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the 2903. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the special functions and the operations which the Q Register and shifter perform for each. When the 2903 executes instructions other than the nine special functions, the Q Register and shifter operation is controlled by instruction bits $I_8I_7I_6I_5$. Table 3 defines the Q Register and shifter operation as a function of these four bits.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 OR I_4 = HIGH, IEN = LOW

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	WRITE	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith.F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith.F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log.Q/2 Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log.Q/2 Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	PARITY	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	PARITY	H	Log.Q/2 Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	PARITY	H	F Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	PARITY	L	F Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith.2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith.2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log.2Q Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log.2Q Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log.2Q Q	Q_3	Input
H	H	H	L	E	SIO_0 Y_0,Y_1, Y_2,Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \veebar F_2 \veebar F_1 \veebar F_0 \veebar SIO_3$

$\veebar$ = Exclusive OR

L = LOW

H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS: $I_0 = I_1 = I_2 = I_3 = I_4$ = LOW, IEN = LOW

I_8	I_7	I_6	I_5	Hex Code	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig. Slice	Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	WRITE
L	L	L	L	0	Unsigned Multiply	$F=S+C_n$ if Z = L $F=R+S+C_n$ if Z = H	Log.F/2⟶Y (Note 1)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	L	H	L	2	Two's Complement Multiply	$F=S+C_n$ if Z= L $F=R+S+C_n$ if Z = H	Log. F/2⟶Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	H	L	L	4	Increment by One or Two	$F=S+1+C_n$	F⟶Y	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	L	H	5	Sign/Magnitude-Two's Complement	$F=S+C_n$ if Z = L $F=S+C_n$ if Z = H	F⟶Y (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	H	L	6	Two's Complement Multiply, Last Cycle	$F=S+C_n$ if Z = L $F=S-R-1+C_n$ if Z = H	Log. F/2⟶Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
H	L	L	L	8	Single Length Normalize	$F=S+C_n$	F⟶Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L
H	L	H	L	A	Double Length Normalize and First Divide Op.	$F=S+C_n$	Log. 2F→Y	$R_3 \veebar F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	L	L	C	Two's Complement Divide	$F=S+R+C_n$ if Z = L $F=S-R-1+C_n$ if Z=H	Log. 2F⟶Y	$R_3 \veebar F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	H	L	E	Two's Complement Divide, Correction and Remainder	$F=S+R+C_n$ if Z = L $F=S-R-1+C_n$ if Z = H	F⟶Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L

NOTES:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only $F_3 \veebar$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \veebar F_3$ is generated at the Y_3 output.
4. Op codes 1, 3, 7, 9, B, D and F are reserved for future use.

L = LOW H = HIGH X = Don't Care Hi-Z = High Impedance $\veebar$ = Exclusive OR

Parity = $SIO_3 \veebar F_3 \veebar F_2 \veebar F_1 \veebar F_0$

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is Low and are in the high-impedance state when $\overline{OE_Y}$ is High. Likewise, the DB output buffers are enabled when the $\overline{OE_B}$ input is Low and in the high-impedance state when $\overline{OE_B}$ is High.

The zero, Z, pin is an open collector input/output that can be wire-OR ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all Low, whether they are driven from the Y output buffers or from an external source connected to the Y_{0-3} pins. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the 2903 instruction.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/MSS$ input/output.

The $\overline{WRITE}$ output is Low when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the 2903 instruction inputs.

When $\overline{IEN}$ is High, the $\overline{WRITE}$ output is forced High and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is Low, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the 2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation (see figure 3).

Programming the Slice Position

Tying the $\overline{LSS}$ input Low programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/MSS$ bidirectional I/O pin. When $\overline{LSS}$ is tied High, the $\overline{WRITE}/MSS$ pin becomes an input pin; tying the $\overline{WRITE}/MSS$ pin High programs the slice to operate as an intermediate slice (IS) and tying it Low programs the slice to operate as a most significant slice (MSS).

SPECIAL FUNCTIONS

The 2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Increment by One or Two

Table 4 defines these Special Functions.

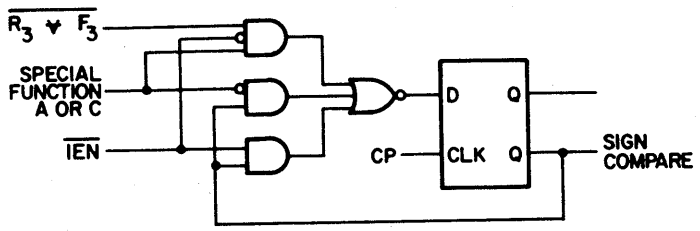
The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the 2903. These functions provide both single- and double- precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Tow's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.



THIS SIGN COMPARE SIGNAL APPEARS AT THE Z OUTPUT OF THE MOST SIGNIFICANT SLICE DURING SPECIAL FUNCTIONS C,D AND E,F. REFER TO TABLE 5.

Figure 3. Sign Compare Flip-Flop

USING THE 2903

The 2903 is designed to be used in microprogrammed systems. Figure 4 illustrates a recommended architecture. The control and data inputs to the 2903 normally will all come from registers clocked at the same time as the 2903. The register inputs come from a ROM or PROM - the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the 2903s and other circuits to execute the desired operation.

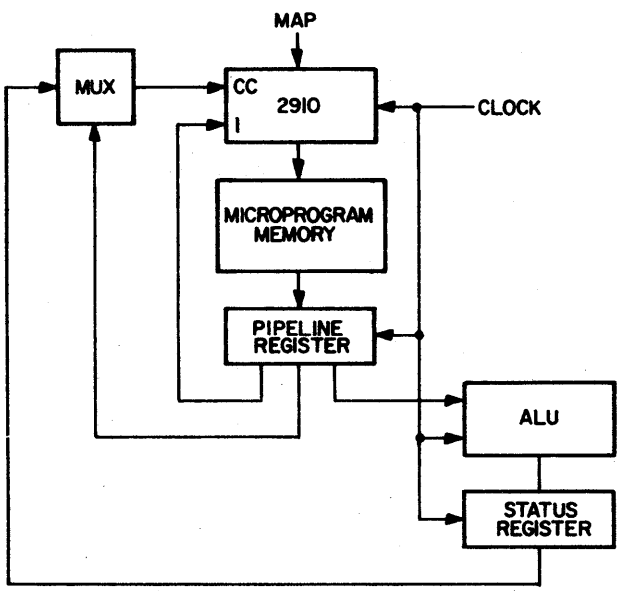


Figure 4. Typical Microprogram Architecture

The address lines of the microprogram store are driven from the 2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The 2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

Note that with the microprogram register in between the microprogram memory store and the 2903s, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the 2903s occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the 2903

The 2903 is a four-bit CPU slice. Any number of 2903s can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 5 illustrates the interconnection of four 2903s to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 are bidirectional left/-right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all 2903s to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted

TABLE 5. 2903 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	G_i (i=0 to 3)	P_i (i=0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z		
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Intermediate Slice	Least Sig. Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
2	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
4	0	L	See Note 1	See Note 2	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z=L $\overline{S}_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
8	0	L	0	S_i	See Note 3	$Q_2 \forall Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	See Note 4	$F_2 \forall F_1$	$\overline{P}$	F_3	$\overline{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_pP_1P_2$

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$
   If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$
   If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$
   At other slices, $C_{n+4} = G \vee PC_n$
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$
   At other slices, $C_{n+4} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

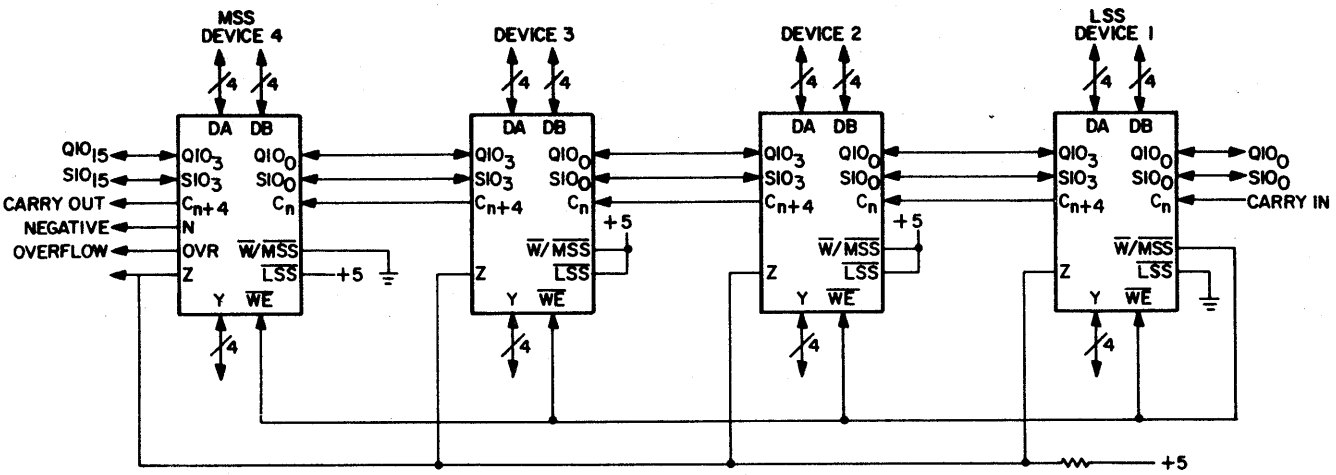


Figure 5. 16-Bit CPU with Ripple Carry

left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied High. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied High and the $\overline{WRITE}/\overline{MSS}$ pin held Low. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry.

The $\overline{IEN}$ pin of the 2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is Low, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is High, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the 2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B B while the three-address mode makes possible A+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The 2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 6_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in figure 5. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

Sign Extend

Sign extension across any number of 2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Instruction E) on I_{5-8} causes the sign present at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is High, Instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are High. Figure 6 outlines the sign extend mode. With I_{6-8} held High, the individual chip sign extend is controlled by I_{5A-D}. If, for example, I_{5A} and I_{5B} are High while I_{5C} and I_{5D} are Low, the signal present at the coundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive adge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension are stored in the RAM.

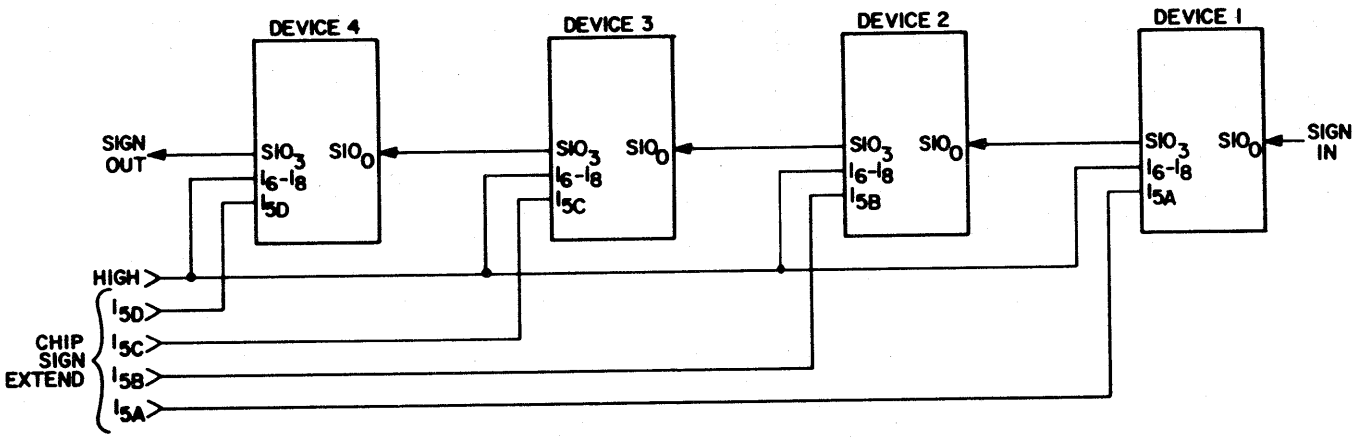


Figure 6. Sign Extend

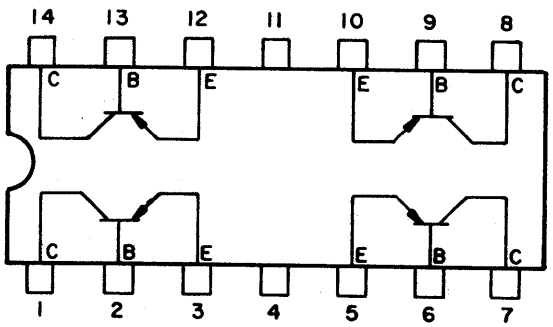
DESCRIPTION

The 2907 is an array of four p-n-p general-purpose transistors in a dual in-line package. Continuous collector current rating is 600 mAdc. Maximum voltage ratings are:

Collector-Emitter	(Vcd)	40V
Collector-Base	(Vcb)	60V
Emitter-Base	(Veb)	5.0V

NOTES:

1. Element identifier: None
2. Package pin configuration is shown below.



2907
Rev K
Sheet 1 of 1

DESCRIPTION

The 2910 is a bipolar microprogram controller intended for controlling the sequence of execution of microinstructions (stored in microprogram memory) in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in figure 1. For convenience, the input/output mnemonics used in figure 1 will be retained throughout these data sheets. The mnemonics are also shown in parentheses outside the logic symbol at the right.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

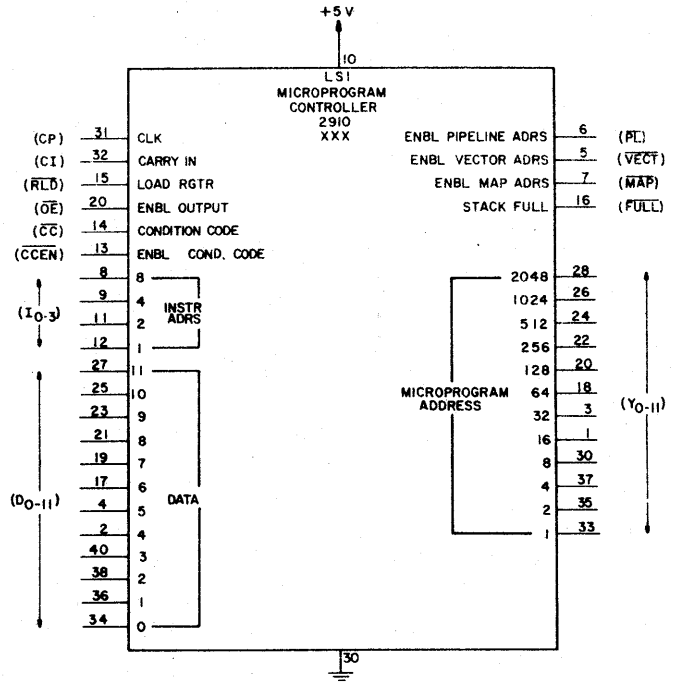
The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is Low, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The 2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in (CI) to the incrementer is High, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1⟶μPC). Sequential microinstructions are thus executed. When the carry-in is Low, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle (Y⟶μPC). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (F). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

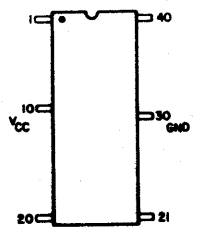
(Continued on sheet 2)



LOGIC SYMBOL

NOTES:

1. Element identification: None
2. Package pin configuration



The stack pointer operates as an up/down counter. During microinstructions 2, 4, and 5, the PUSH operation is performed. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes Low. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three micoinstructions (8,9, F) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During Instruction F, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table 1 shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs.

The value loaded into µPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs PL, MAP, and VECT is Low. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table 2 (Pin Functions), can modify instruction execution. The combination CC High and $\overline{CCEN}$ Low is used as a test in 10 of the 16 instructions. $\overline{RLD}$, when Low, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally Low, may be forced High to remove the 2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during Instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the S outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

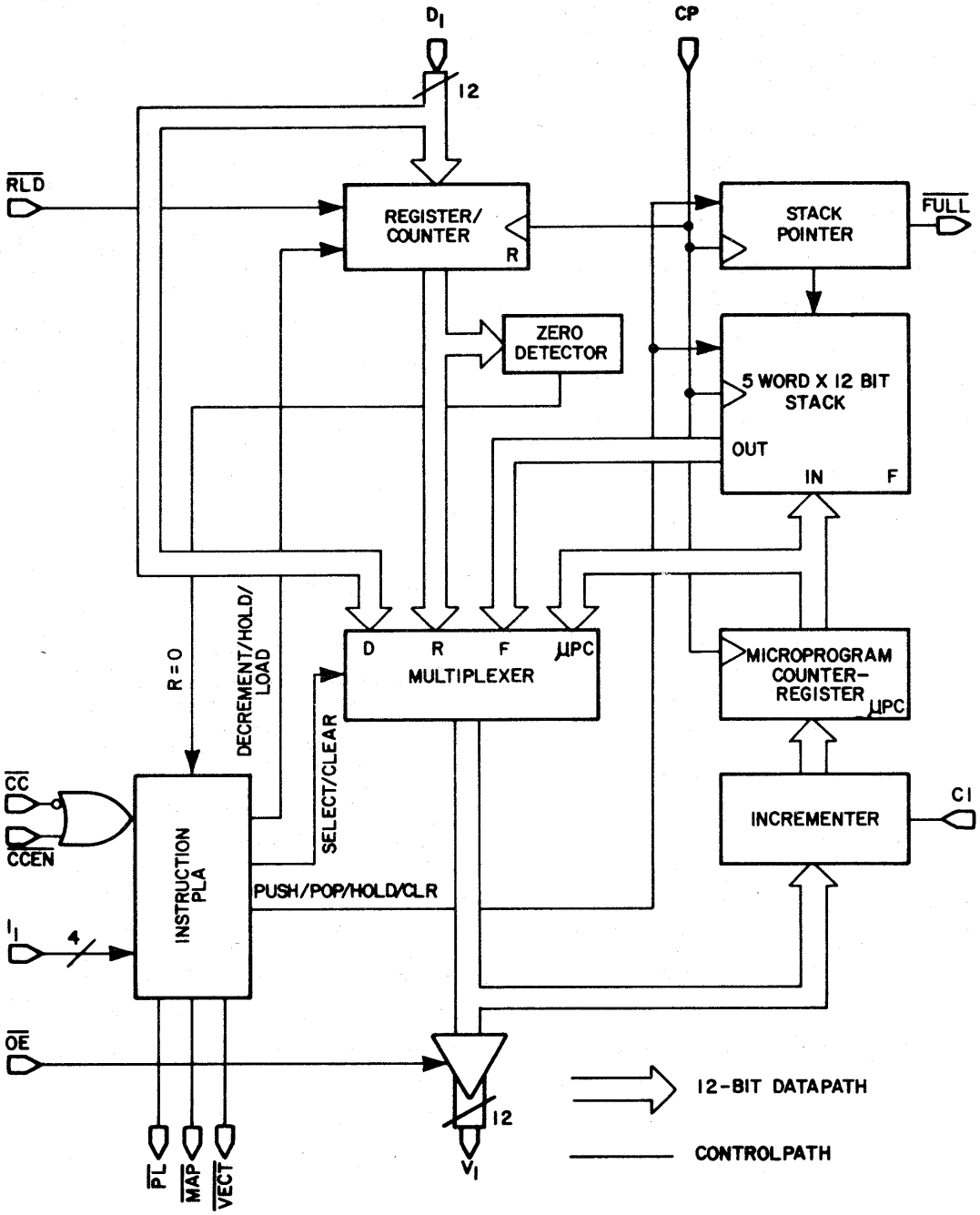


Figure 1. Block Diagram

TABLE I. INSTRUCTIONS

HEX I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
A	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
B	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
C	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
D	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
E	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
F	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

TABLE 2. PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the Am2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

THE 2910 INSTRUCTION SET

The 2910 provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional - their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table 1. In this discussion it is assumed that CI is tied High.

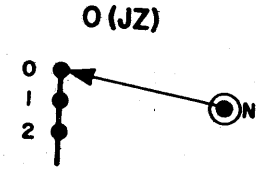
In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is Low, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ High, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it High, which is useful if no microinstruction is data-dependent; (2) tying it Low if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of 2910 instruction bit I_0, which leaves instructions 4, 6, and A as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction F is affected both by the external condition code and the internal register/counter.

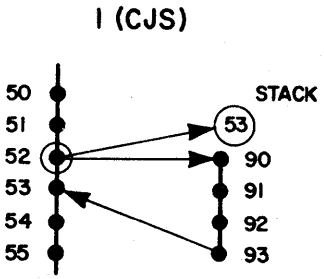
Perhaps the best technique for understanding the 2910 is simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, examples are shown to the right of each description.

The examples should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number E, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the test to follow will explain what the conditional choices are in each example.

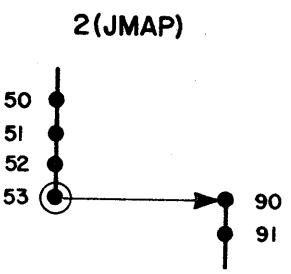
Instruction 0, JZ (JUMP and ZERO, or RESET), unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.



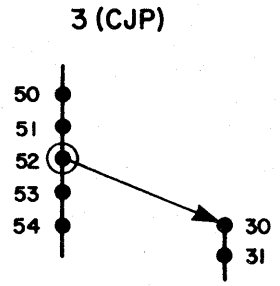
Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. In this example the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.



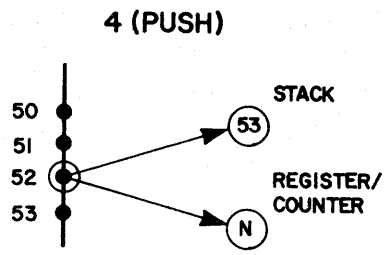
Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.



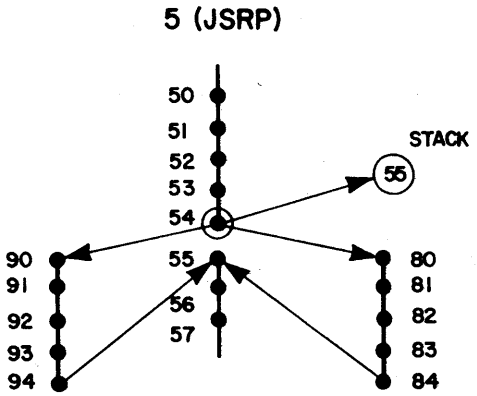
Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value. This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. The conditional jump via the pipeline register address is at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.



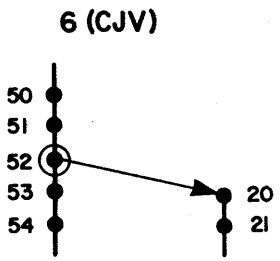
Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In the example, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will describe how to use the pushed value and the register/counter for looping.



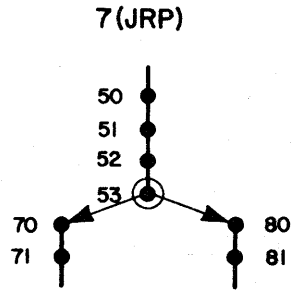
Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number A) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the 2910 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.



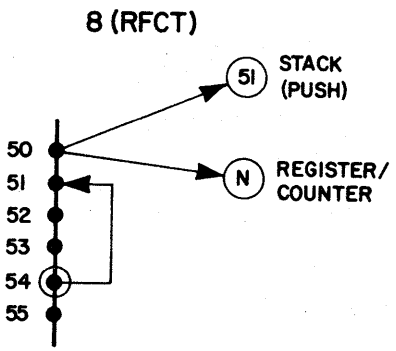
Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the 2910 $\overline{\text{VECT}}$ output is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the TEST input is High and the microinstruction at address 53 will be executed if the TEST input is Low.



Instruction 7 is a CONDITIONAL JUMP via the contents of the 2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to Instruction 5, the conditional jump-to-subroutine via R or PL. The major difference between Instruction 5 and Instruction 7 is that no push onto the stack is performed with 7. The example depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the 2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.



Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POPed by decrementing the stack pointer, but the contents of the top of the stack are thrown away.



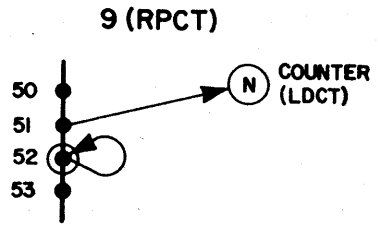
An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

Since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

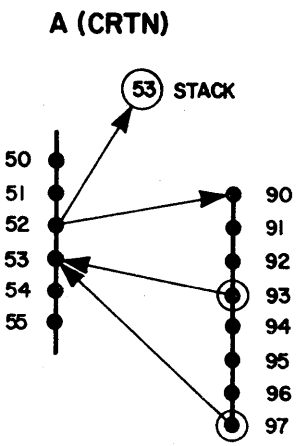
Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to Instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of Instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

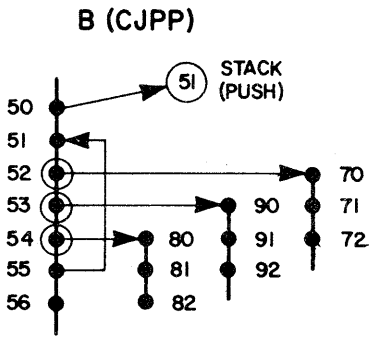
In the example, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number C). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.



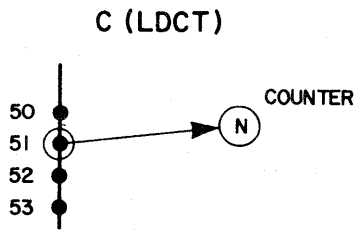
Instruction A is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force $\overline{CCEN}$ High, disabling the test and the forced PASS causes an unconditional return.



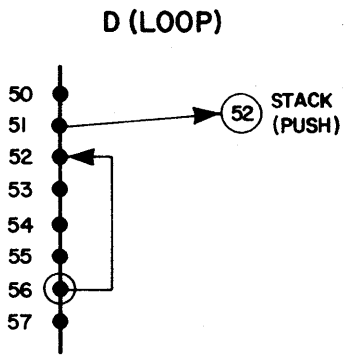
Instruction B is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the TEST input is passed, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.



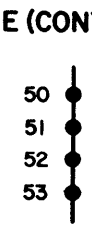
Instruction C is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter - - the explicit load by Instruction C; the conditional load included as part of Instruction 4; and the use of the RLD input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power at the expense of one bit of microinstruction width. Instruction C is exactly equivalent to the combination of instruction E and $\overline{RLD}$ Low. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.



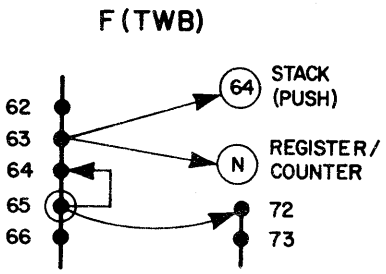
Instruction D is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POPed thus, accomplishing the required stack maintenance.



Instruction E is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.



Instruction F, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like Instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. In struction F performs a decrement-and-branch-until-zero function similar to Instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of Instruction F the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero or by passing the conditional test, the stack is POPed by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.



The application of Instruction F can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

As one example, consider the case of a memory search instruction. The instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POPed once, removing the value 64 from the top of the stack.

DESCRIPTION

Type 3423 is an overvoltage protection (OVP) device that senses transient overvoltages or regulator failures. It is used in conjunction with an external "crowbar" SCR to quickly short circuit the power supply, forcing it into current limiting or opening the fuse or circuit breaker. The device can be connected to operate in either the Instant or the Delayed mode.

In the delayed mode, trip voltage V_T is developed across a voltage divider between Vcc and ground, and is fed to pin 2, where it is compared with the reference voltage, V_{REF}, which is typically 2.6 V. When V_T exceeds V_{REF}, a current flows from pin 4 to charge an external capacitor. If the overvoltage persists long enough, the capacitor will charge to V_T. Because pin 3 is connected to pin 4 in this mode, the delayed trip voltage will activate the device, causing output pin 8 to go high. Pin 8 provides the control for the G (gate) input to the external SCR, which turns on to short the supply.

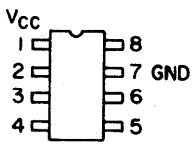
In the instant mode, pin 4 is not used, and pins 2 and 3 are both connected to the trip voltage source. Otherwise, operation is as described above.

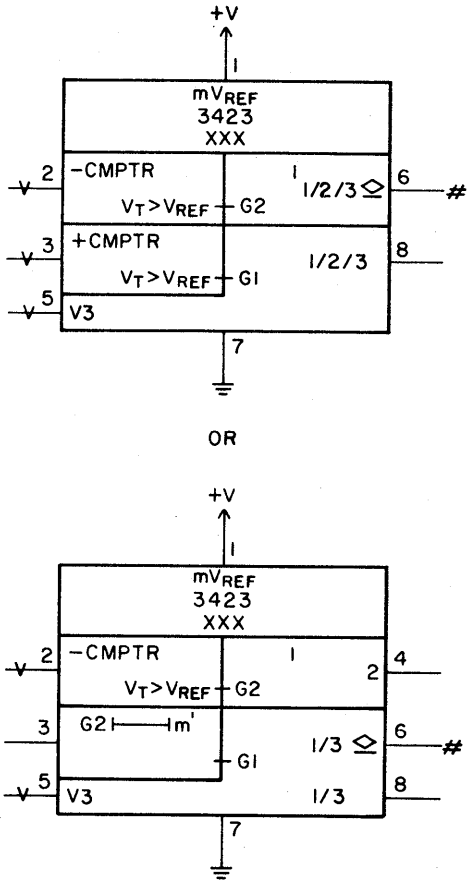
In either mode, if a voltage greater than 2.0 V is applied to pin 5, the device will trip regardless of whether or not an overvoltage condition exists.

Pin 6 provides an open-collector output that goes active along with pin 8. This output may be used to trigger a FF that acts in parallel with the SCR to shut down the power supply. Such an arrangement reduces the heat-sink requirements of the SCR.

NOTES:

1. Element identifier: none
2. Package pin configuration:





1. REPLACE m WITH DESIRED REFERENCE VOLTAGE.
2. REPLACE m' WITH DELAY PERIOD.

LOGIC SYMBOL

3423
Rev K
Sheet 1 of 1

DEXCRIPTION

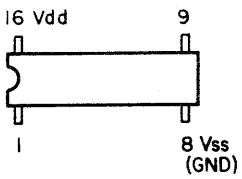
The 4021 is an 8-bit, static CMOS shift register. It is capable of parallel in/serial out, or serial in/serial out operations, depending upon the state of the parallel/serial shift control (pin 9).

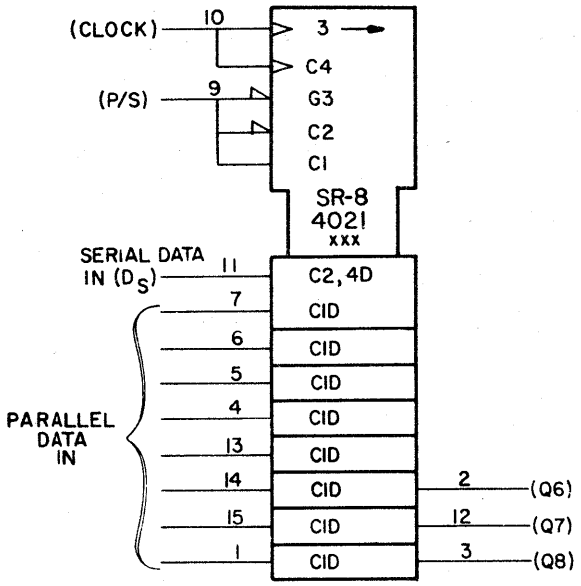
When pin 9 is high, data at the parallel data inputs is asynchronously loaded into the register. In this situation, data received by the last three stages is immediately available at the outputs of those three stages.

When pin 9 is low, data is shifted through the register on the positive-going edge of each clock pulse (pin 10), and at the same time serial data at pin 11 is shifted into the register.

NOTES:

1. Element identification: None
2. Package pin configuration:





LOGIC SYMBOL

TRUTH TABLES

SERIAL OPERATIONS

t	CLOCK	Ds	P/S	Q6 t=n+6	Q7 t=n+7	Q8 t=n+8
n	⌐	0	0	0	?	?
n+1	⌐	1	0	1	0	?
n+2	⌐	0	0	0	1	0
n+3	⌐	1	0	1	0	1
	⌐	X	0	Q6	Q7	Q8

PARALLEL OPERATION

CLOCK	D_s	P/S	D_m	Q_m
⌐	X	1	0	0
⌐	X	1	1	1

X = DON'T CARE

4021
Rev K
Sheet 1 of 1

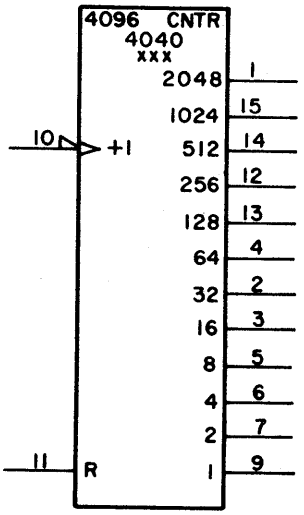
DESCRIPTION

The 4040 is a 12-stage CMOS counter with asynchronous clear. The clock input (pin 10) contains a special pulse-shaping circuit, allowing the counter to be triggered by a sine wave input. The count is advanced on the negative-going edge of the clock.

Maximum clocking frequency is dependent upon the supply voltage (VDD). Typical values are given below

VDD	MHz
5.0V	3.5
10.0V	9.0
15.0V	13.0

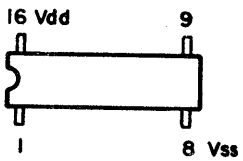
See sheet 2 for functional block diagram and truth table.

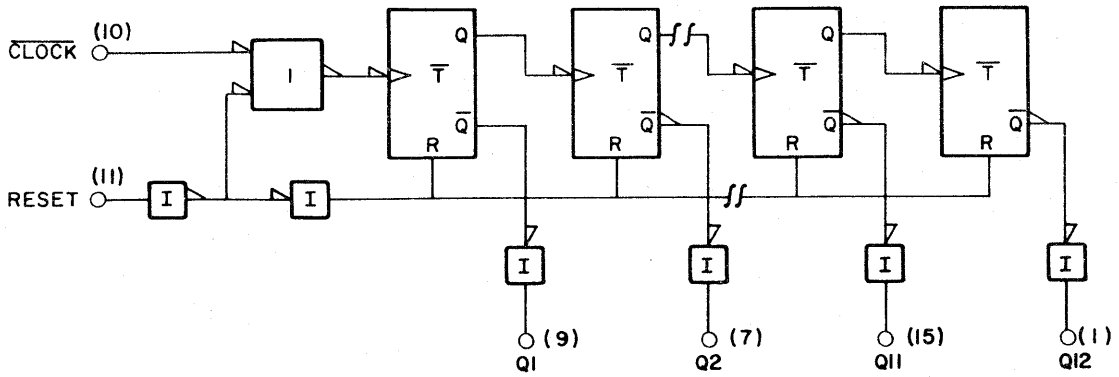


LOGIC SYMBOL

NOTES:

1. Element identifier: None
2. Package pin configuration:





OUTPUTS NOT SHOWN

(6)	Q3	(4)	Q7
(5)	Q4	(13)	Q8
(3)	Q5	(12)	Q9
(2)	Q6	(14)	Q10

FUNCTIONAL BLOCK DIAGRAM

TRUTH TABLE

$\overline{\text{CLOCK}}$	RESET	OUTPUT STATE
⌐‾	L	NO CHANGE
‾⌐	L	ADVANCE TO NEXT STATE
X	H	ALL OUTPUTS ARE LOW

X = DON'T CARE

DESCRIPTION

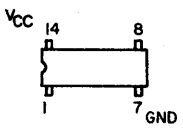
The 5603 circuit is a 1024-bit programmable read-only memory (PROM) organized as 256 words of 4 bits each. Open-collector outputs are provided.

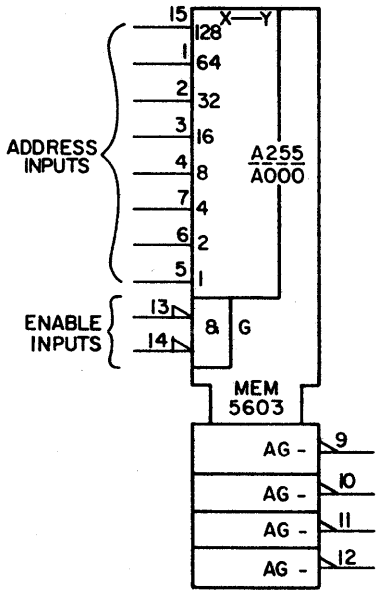
Logical ones are written into the memory using special equipment. Reading is accomplished by bringing the selected address bits high, while bringing both enable inputs (G) low.

With either or both G-inputs high, the outputs are floating. Typical access time is 40 ns.

NOTES:

1. Element identifier: none
2. Package pin configuration.





LOGIC SYMBOL

5603
Rev J
Sheet 1 of 1

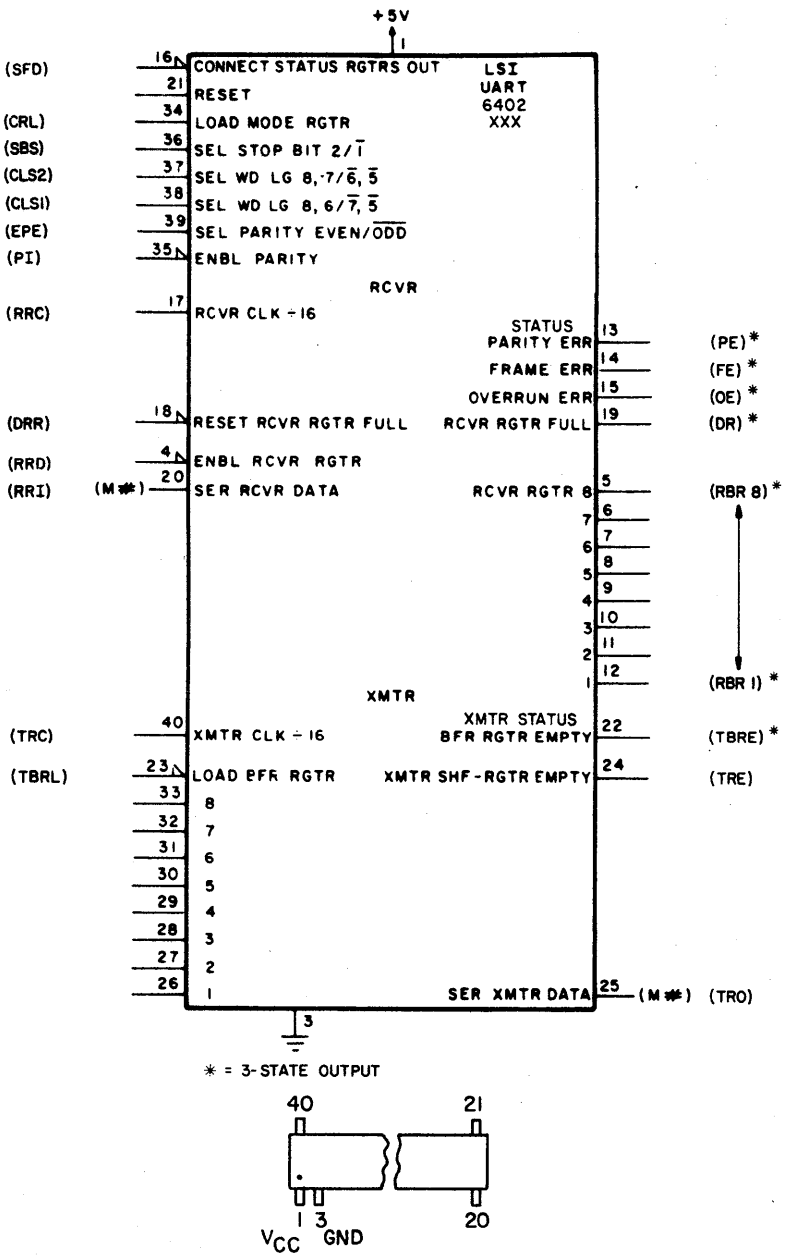
DESCRIPTION

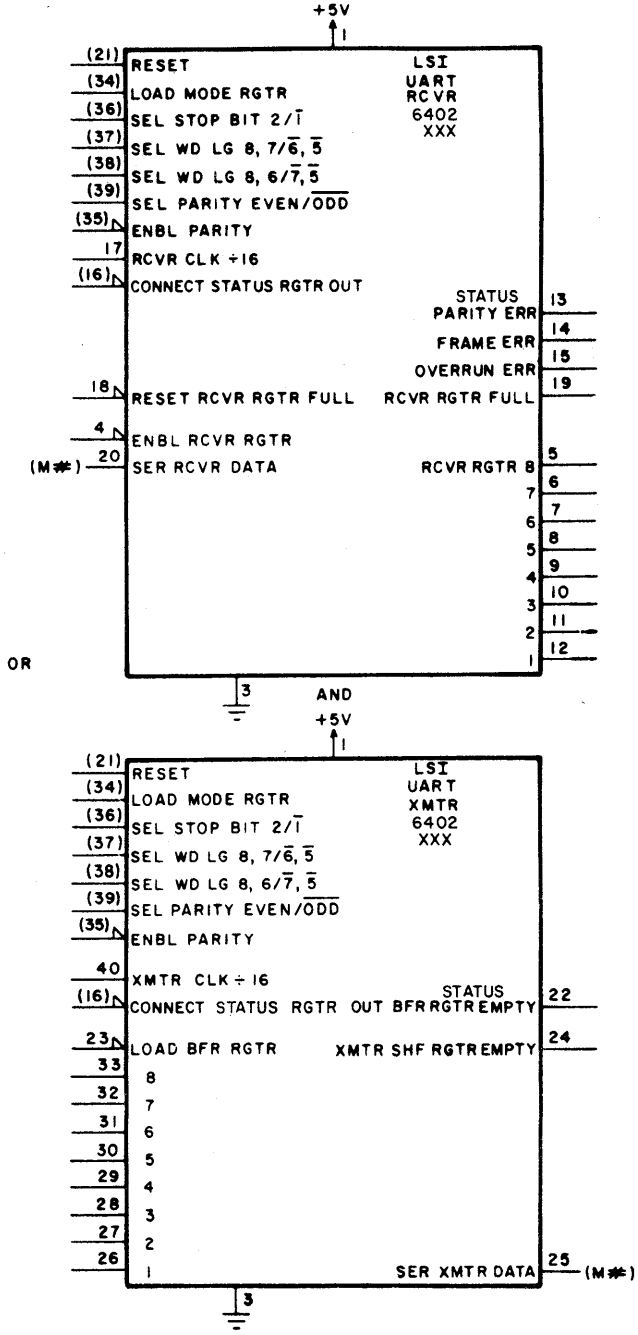
(Logic symbols and pin configuration are on sheet 2.)

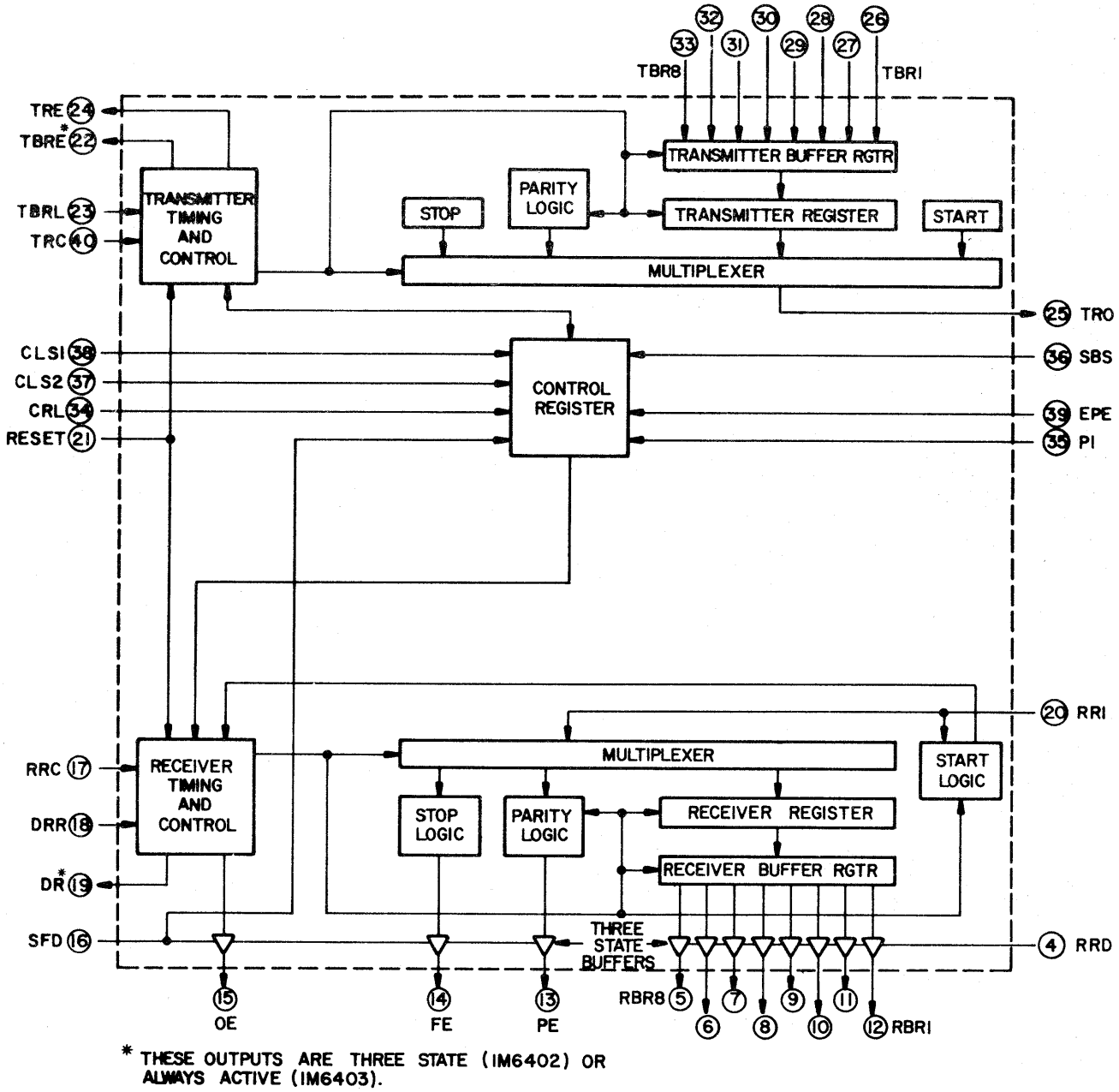
The 6402 is a CMOS Universal Asynchronous Receiver Transmitter (UART) that acts as an interface between a computer or microprocessor and a serial data channel. The Receiver section converts serial start, data, parity, and stop bits into parallel data, at the same time verifying proper code transmission. The Transmitter section converts parallel data to serial form, adding start, parity, and stop bits. Data word length can be 5, 6, 7, or 8 bits. Parity can be odd or even, or the parity check/generate function can be inhibited. Control-word functions are given in table 1 on sheet 6.

Separate inputs are provided for the transmitter and receiver clocks. These inputs will accept frequencies up to 4.0 MHz which, when divided by 16 within the UART, permit data-channel speeds of up to 250,000 band.

Abbreviations have been added to the left-hand symbol on sheet 2; these abbreviations are used in the descriptions of the transmit and receive functions. Note that the received data (RBRx) outputs are three-state, as are all status outputs except TRE (pin 24). Status lines TBRE (pin 22) and DR (pin 19) are always active. Other status lines may be examined by bringing SFD (pin 16) low.


+5V
LSI UART 6402 XXX
(SFD) 16 CONNECT STATUS RGTRS OUT
21 RESET
(CRL) 34 LOAD MODE RGTR
(SBS) 36 SEL STOP BIT 2/1
(CLS2) 37 SEL WD LG 8, 7/6, 5
(CLSI) 38 SEL WD LG 8, 6/7, 5
(EPE) 39 SEL PARITY EVEN/ODD
(PI) 35 ENBL PARITY
RCVR
(RRC) 17 RCVR CLK ÷16
STATUS PARITY ERR 13 (PE)*
FRAME ERR 14 (FE)*
OVERRUN ERR 15 (OE)*
(DRR) 18 RESET RCVR RGTR FULL
RCVR RGTR FULL 19 (DR)*
(RRD) 4 ENBL RCVR RGTR
(RRI) (M*) 20 SER RCVR DATA
RCVR RGTR 8 5 6 7 6 8 5 9 4 10 3 11 2 12 1 (RBR 8)* (RBR 1)*
XMTR
(TRC) 40 XMTR CLK ÷16
XMTR STATUS BFR RGTR EMPTY 22 (TBRE)*
(TBRL) 23 LOAD BFR RGTR
XMTR SHF-RGTR EMPTY 24 (TRE)
33 8 32 7 31 6 30 5 29 4 28 3 27 2 26 1
SER XMTR DATA 25 (M*) (TRO)
3
* = 3-STATE OUTPUT
40 21
1 3 20
VCC GND


+5V
LSI UART RCVR 6402 XXX
(21) RESET
(34) LOAD MODE RGTR
(36) SEL STOP BIT 2/1
(37) SEL WD LG 8, 7/6, 5
(38) SEL WD LG 8, 6/7, 5
(39) SEL PARITY EVEN/ODD
(35) ENBL PARITY
17 RCVR CLK ÷16
(16) CONNECT STATUS RGTR OUT
STATUS PARITY ERR 13
FRAME ERR 14
OVERRUN ERR 15
18 RESET RCVR RGTR FULL
RCVR RGTR FULL 19
4 ENBL RCVR RGTR
(M*) 20 SER RCVR DATA
RCVR RGTR 8 5 6 7 6 8 5 9 4 10 3 11 2 12 1
3
OR
AND
+5V
LSI UART XMTR 6402 XXX
(21) RESET
(34) LOAD MODE RGTR
(36) SEL STOP BIT 2/1
(37) SEL WD LG 8, 7/6, 5
(38) SEL WD LG 8, 6/7, 5
(39) SEL PARITY EVEN/ODD
(35) ENBL PARITY
40 XMTR CLK ÷16
(16) CONNECT STATUS RGTR OUT
STATUS BFR RGTR EMPTY 22
23 LOAD BFR RGTR
XMTR SHF RGTR EMPTY 24
33 8 32 7 31 6 30 5 29 4 28 3 27 2 26 1
SER XMTR DATA 25 (M*)
3



* THESE OUTPUTS ARE THREE STATE (IM6402) OR ALWAYS ACTIVE (IM6403).

Figure 1. Functional Block Diagram

TRANSMIT FUNCTION

The transmitter section accepts parallel data, formats it, and transmits it in serial form on the TRO line. Data is loaded into the transmitter buffer register (refer to block diagram, figure 1) from inputs TRI-TR8 by bringing TBRL low (see A in figure 2). If less than eight bits, the character is right-justified into the least significant bit, TRl. Only the significant bits are transmitted. The rising edge of TBRL clears TBRE (at B) and, zero to one clock cycles later, data is transferred to the transmitter register. At the same time, TRE is cleared, TBRE is set high, and serial data transmission is begun. Output data is clocked by TRC; 16 clock cycles are required to serialize each bit.

A second pulse on TBRL (C) loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the previous character has been completed (at D). Transmission of the second character begins one-half cycle later.

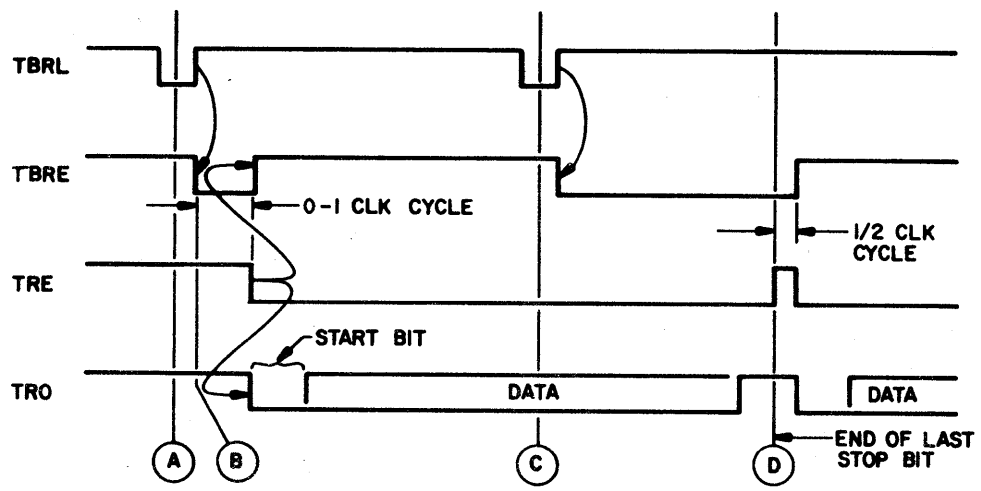


Figure 2. Transmitter Timing

RECEIVE FUNCTION

Serial data is received at the RRI input, pin 20. As shown in figure 3, RRI must remain in the MARK state (logic HI) when no data is being received. Data is clocked by RRC, which pulses at 16 times the data rate.

A low on DRR (A in figure 3) clears the DR line as well as the receiver and receiver buffer registers (see figure 1). Meanwhile, the start logic has been looking for a start bit, signalled by RRI going low. (A valid start bit is signified if RRI is still low after 7 1/2 clock cycles.) After having s sensed the start bit, the UART loads the serial data bits into the receiver register.

Upon sensing the first stop bit (MARK state for 7 1/2 cycles) data is transferred from the receiver register to the receiver buffer register (B), right-justified to the least significant position, RBR1. If DR was not cleared prior to this transfer (DR is cleared by a low on DRR), an overrun error occurs and is indicated by OE going high. One-half clock cycle later (at C), DR is set high and PE and FE are evaluated. A high on PE indicates a parity error; a high on FE indicates a framing error, caused by sensing an invalid stop bit. Data in the receiver buffer register is read by bringing RRD (pin 4) low.

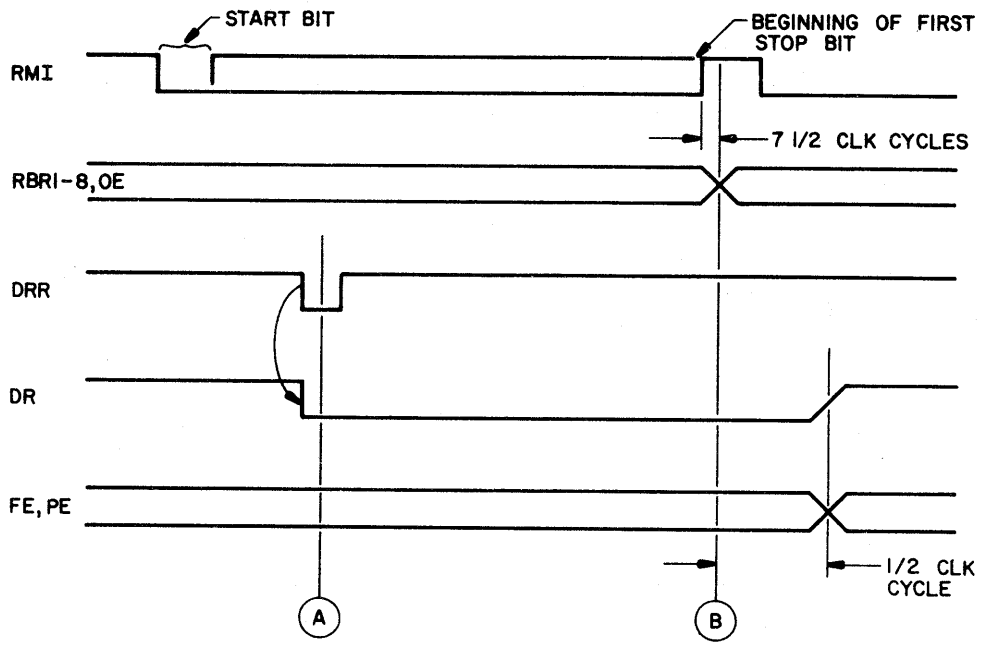


Figure 3. Receiver Timing

Table 1. 6402 Control-Word Definition

CONTROL WORD					CHARACTER FORMAT			
SBS								
EPE								
PI								
CLS 1								
CLS 2								
Pin No→	37	38	35	39	36	START BIT	DATA BITS	PARITY BIT	STOP BITS
	L	L	L	L	L	1	5	Odd	1
	L	L	L	L	H	1	5	Odd	1.5
	L	L	L	H	L	1	5	Even	1
	L	L	L	H	H	1	5	Even	1.5
	L	L	H	X	L	1	5	None	1
	L	L	H	X	H	1	5	None	1.5
	L	H	L	L	L	1	6	Odd	1
	L	H	L	L	H	1	6	Odd	2
	L	H	L	H	L	1	6	Even	1
	L	H	L	H	H	1	6	Even	2
	L	H	H	X	L	1	6	None	1
	L	H	H	X	H	1	6	None	2
	H	L	L	L	L	1	7	Odd	1
	H	L	L	L	H	1	7	Odd	1
	H	L	L	H	L	1	7	Even	1
	H	L	L	H	H	1	7	Even	2
	H	L	H	X	L	1	7	None	1
	H	L	H	X	H	1	7	None	2
	H	H	L	L	L	1	8	Odd	1
	H	H	L	L	H	1	8	Odd	2
	H	H	L	H	L	1	8	Even	1
	H	H	L	H	H	1	8	Even	2
	H	H	L	X	L	1	8	None	1
	H	H	L	X	H	1	8	None	2

L = Low; H = High; X = Don't care

DESCRIPTION

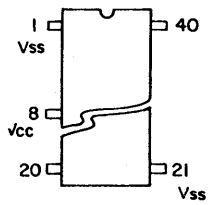
The 6800 is a monolithic 8-bit microprocessor. In all respects save two, it functions in the same manner as the 6802 (which see). The two differences, lack of an internal system clock and lack of 128 bytes of on-board RAM, necessitate differences in five pin functions. These are listed below and described on sheet 3. A block diagram of the 6800 is shown on sheet 2. For all other aspects, please refer to the 6802 data sheets.

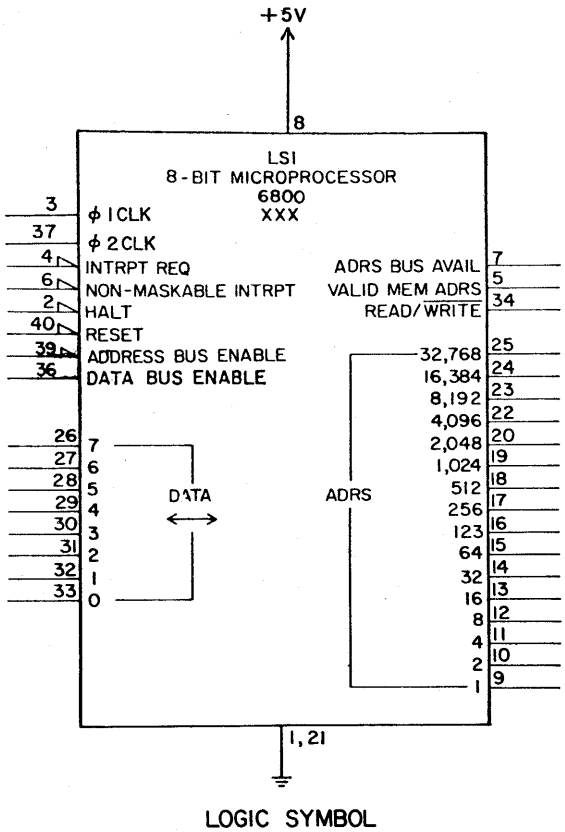
In the pin differences below, the 6802 pin functions are shown in parentheses.

Pin	FUNCTION
3	01 CLK (MEM RDY)
37	02 CLK (ENBL SYSTEM)
39	ADDRESS BUS ENBL (XTAL)
36	DATA BUS ENBL (RAM ENBL)
35	NOT USED (Vcc STANDBY)

NOTES:

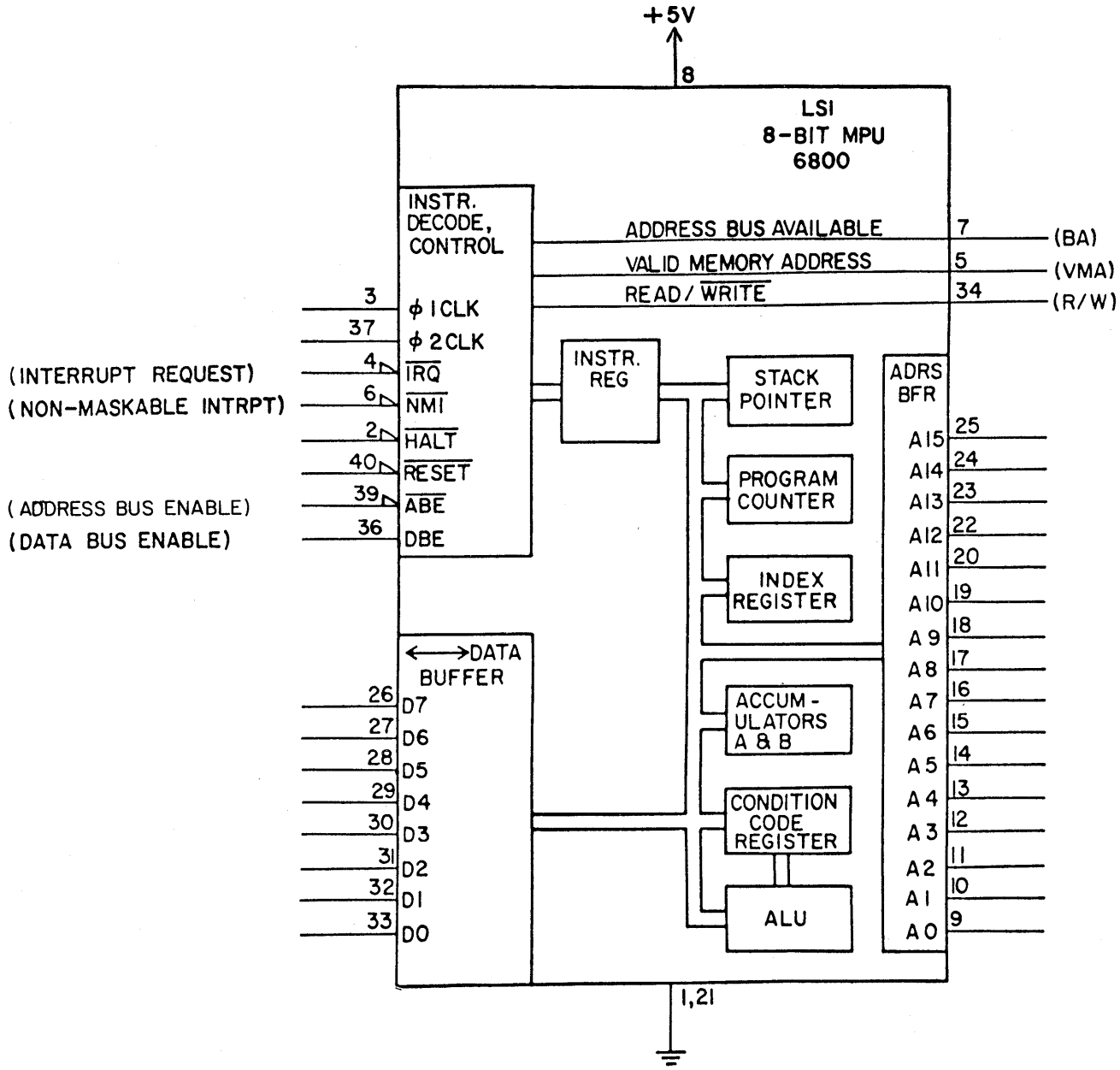
1. Element identifier: None
2. Package pin configuration.





LOGIC SYMBOL

6800
Rev. L
Sheet 1 of 3



MPU Block Diagram

6800
Rev. L
Sheet 2 of 3

pin 3 Ø1 CLK
pin 37 Ø2 CLK

These two input pins are connected to an external clock generator such as the 6875 (which see).

pin 39 ADDRESS BUS ENABLE (ABE)

When this line is high, the Address Bus and the R/W line are placed in a Hi-Z state. In addition, VMA and BA are forced low to prevent false reads or writes on any device enabled by VMA. This condition will occur 700 ns after ABE=2.0 V. The Data Bus is not affected by ABE and has its own enable (DBE). In direct memory access (DMA) applications, TSC should be brought high on the leading edge of the Ø1 clock. The Ø1 clock must be held high and the Ø2 clock held low for this (DMA) application. The Address Bus will then be available for other devices to directly address memory. Because the MPU is a dynamic device, it can be held in this state for only 4.5 µs or destruction of data will occur.

pin 36 DATA BUS ENABLE (DBE)

This input is the 3-state control for the MPU Data Bus, and enables the bus drivers when in the high state. For normal operation, DBE would be driven by the Ø2 clock. During an MPU Read cycle, the Data Bus drivers are disabled internally. When it is desired that another device control the Data Bus, such as in DMA applicatins, DBE should be held low.

pin 35 Not used in the 6800

READER NOTICE

The following data sheets provide basic information on the 6802 microprocessor, including the instruction list, register descriptions, signal definitions, and some timing functions. Information concerning specific applications of the 6802 is contained in the Theory of Operation section of the Hardware Reference manual for the relevant equipment.

These data sheets do not tell how to program the 6802. For such information, the reader is referred to material provided by the vendor (Fairchild) and/or to the various programming manuals available for the 6800/6802 family.

DESCRIPTION

The 6802 is a monolithic 8-bit microprocessor with a repertoire of 72 instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions.

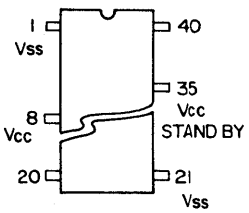
In addition to the registers needed to perform the above operations, the 6802 contains an internal systems-clock oscillator and 128 bytes of on-board RAM. The first 32 bytes in RAM, locations 0000 through 001F, may be retained in a low-power mode (Vcc Standby) that facilitates memory retention during a power-down situation.

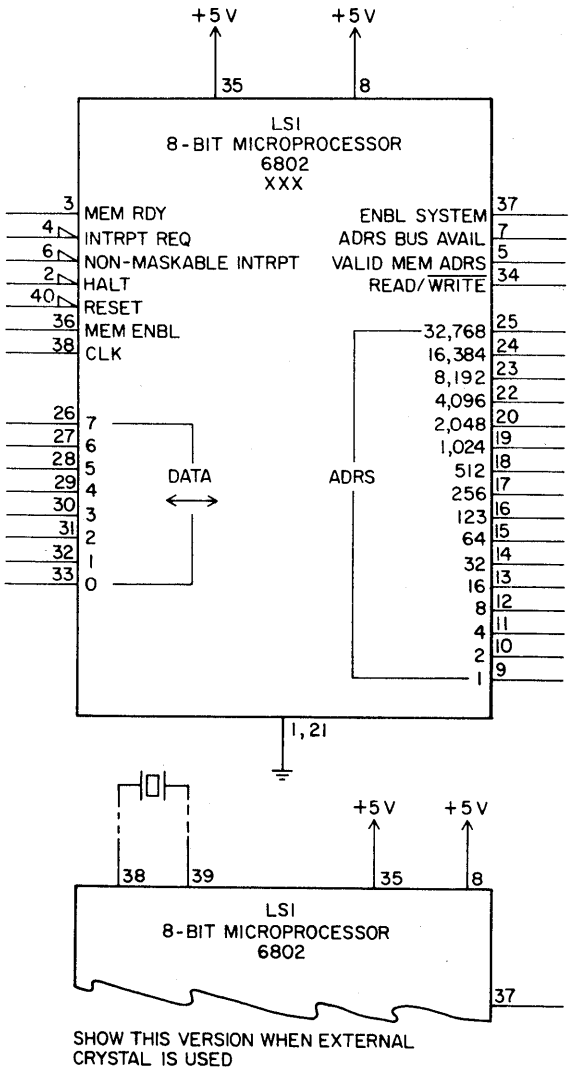
The 6802 is compatible with all other elements in the 6800 family, and is expandable to 64K words. A block diagram of the microprocessing unit (MPU) is shown in figure 1. Table 1 contains the instruction set, given in alphabetic sequence.

NOTES:

1. Element identifier (for reference only): 585

2. Package pin configuration:





LOGIC SYMBOL

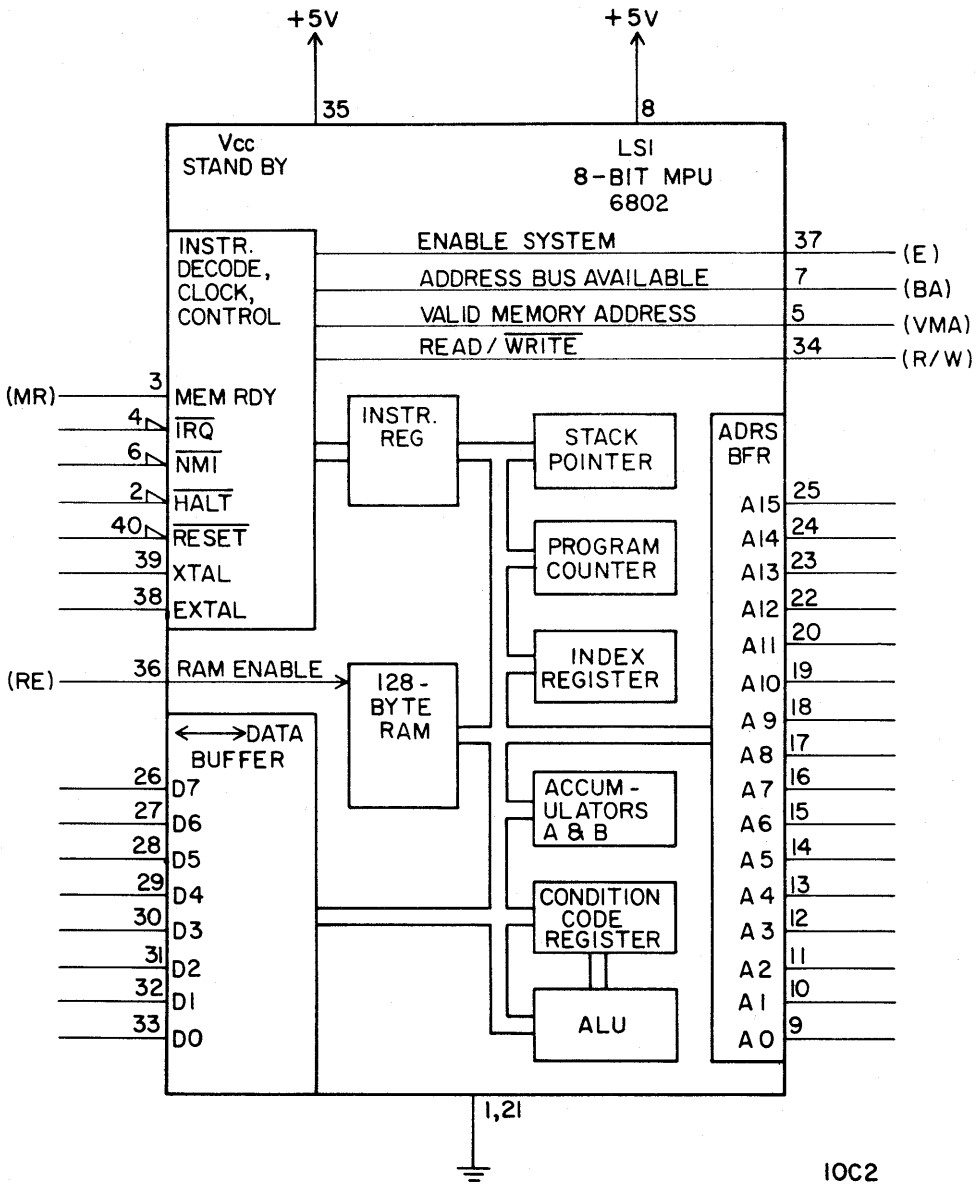


Figure 1. MPU Block Diagram

TABLE 1 - 6802 MICROPROCESSOR INSTRUCTION SET - ALPHABETIC SEQUENCE

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch to Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return form Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

MPU REGISTERS

As shown in figure 1, the number and configuration of the registers are the same as for the 6800. The 128 X 8-bit RAM has been added to the basic MPU. The first 32 bytes may be operated in a low-power mode via a Vcc standby. These 32 bytes can be retained during power-up and power-down conditions via the RE signal.

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (figure 2).

PROGRAM COUNTER

The program counter is a 2- byte (16 bits) register that points to the current program address.

STACK POINTER

The stack pointer is a 2- byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

INDEX REGISTER

The index register is a 2-byte register that is used to store data or a 16-bit memory address for the Indexed mode of memory addressing.

ACCUMULATORS

The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

CONDITION CODE REGISTER

The condition code register (8 bits) holds the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from Bit 7 (C), and half carry from Bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 3 shows the order of saving the microprocessor status within the stack.

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to

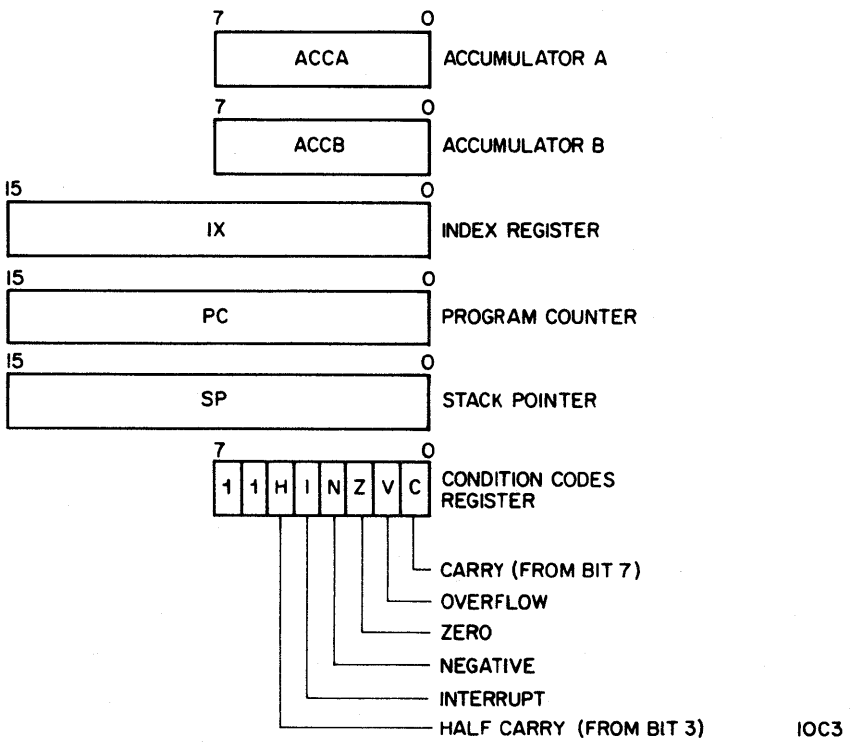


Figure 2. Programming Model of the Microprocessing Unit

determine the state of the processor. These control and timing signals for the 6802 are identical to those of the 6800 except that TSC, DBE, Φ1, Φ2 input, and two unused pins have been eliminated, and the following signal and timing lines have been added:

RAM Enable (RE)
Crystal Connections EXtal and Xtal
Memory Ready (MR)
Vcc Standby
Enable Φ2 Output (E)

A summary of the 6802 MPU signals follows.

ADDRESS BUS (A0—A15)

Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0—D7)

Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has 3-state output buffers capable of driving one standard TTL load and 130 pF.

$\overline{\text{HALT}}$

When this input is in the LOW state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a HIGH state, Valid Memory Address will be at a LOW state, and all other 3-state lines will be in the High-Z mode. The address bus will display the address of the next instruction.

To ensure single instruction operation, transition of the $\overline{\text{HALT}}$ line must not occur during the last 250 ns of E and the $\overline{\text{HALT}}$ line must go HIGH for one Clock cycle.

READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$)

This TTL-compatible output signals the peripherals and memory devices whether the MPU is in a Read (HIGH) or Write (LOW) state. The normal standby state of this signal is Read (HIGH). When the processor is halted, it will be in the logical "1" state. This output is capable of driving one standard TTL load and 90 pF.

SP = STACK POINTER
CC = CONDITION CODES (ALSO CALLED THE PROCESSOR STATUS BYTE)
ACCB = ACCUMULATOR B
ACCA = ACCUMULATOR A
IXH = INDEX REGISTER, HIGHER ORDER 8 BITS
IXL = INDEX REGISTER, LOWER ORDER 8 BITS
PCH = PROGRAM COUNTER, HIGHER ORDER 8 BITS
PCL = PROGRAM COUNTER, LOWER ORDER 8 BITS

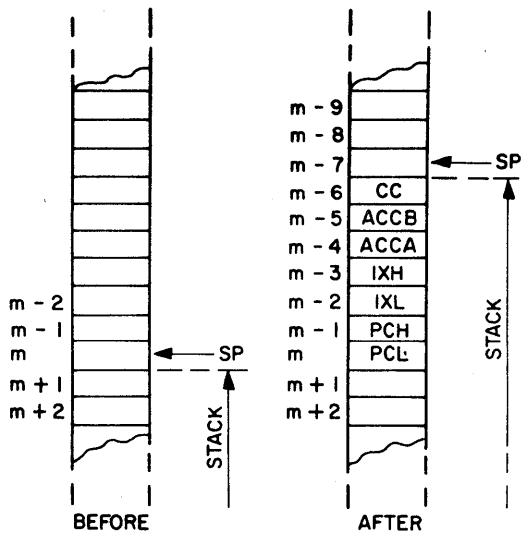


Figure 3. Saving the Status of the Microprocessor in the Stack

VALID MEMORY ADDRESS (VMA)

This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling pheripheral interfaces such as the PIA and ACIA. This signal is not 3-state. One standard TTL load and 90 pF may be directly driven by this active HIGH signal.

ADDRESS BUS AVAILABLE (BA)

The Address Bus Available signal is normally in the LOW state; when activated, it will go to the HIGH state indicating that the microporcessor has stopped and that the address bus is available. This will occur if the $\overline{\text{HALT}}$ line is in the LOW state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all 3-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit 1 = "0") or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

INTERRUPT REQL ($\overline{\text{IRQ}}$)

This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit HIGH so that no further nnterrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{HALT}}$ line must be in the HIGH state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{HALT}}$ is LOW.

The $\overline{\text{IRQ}}$ has a high-impedance pull-up device internal to the chip; however, a 3-kΩ external resistor to Vcc should be used for wired-OR and optimum control of interrupts.

$\overline{\text{RESET}}$

This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. When this line is LOW, the MPU is inactive and the information in the registers will be lost. If a HIGH level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced HIGH. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. Power-up and reset timing and power-down sequences are shown in figures 4 and 5, respectively.

NON—MASKABLE INTERRUPT ($\overline{\text{NMI}}$)

A LOW-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is 1 located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high—impedance pull-up resistor internal to the chip; however, a 3-kΩ external resistor to Vcc should be used for wired-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled when E is HIGH and will start the interrupt routine on a LOW E following the completion of an instruction.

Figure 6 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 2 gives the memory map for interrupt vectors.

RAM ENABLE (RE)

A TTL-compatible RAM Enable input controls the on-chip RAM of the 6802. When placed in the HIGH state, the on-chip memory is enabled to respond to the MPU controls. In the LOW state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during a power-down situation. RAM Enable must be LOW 3μs before Vcc goes below 4.75 V during a power down.

EXTAL AND XTAL

The 6802 has an oscillator that may be crystal controlled. These connections are for a series resonant fundamental crystal. (AT cut.) A divide-by-four circuit has been added to the 6802 so that a 4-MHz crystal may be used in lieu of a 1-MHz crystal for a more cost effective system. Pin 38 of the

6802 may be driven externally by a TTL input signal if a separate clock is required. Pin 39 is to be left open in this mode.

MEMORY READY (MR)

MR is a TTL-compatible input control signal which allows stretching of E. When MR is HIGH, E will be in normal operation. When

AC OPERATING CONDITIONS (Use with figures 4, 5, and 8)

Symbol	Parameter	Min	Typ	Max	Unit
t_{AD}	Address Delay	-	-	270	ns
t_{ACC}	Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{DSR})$	-	-	530	ns
t_{DSR}	Data Setup Time (Read)	100	-	-	ns
t_H	Input Data Hold Time	10	-	-	ns
t_H	Output Data Hold Time	20	-	-	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	20	-	-	ns
t_{DDW}	Data Delay Time (Write)	-	165	225	ns
	Processor Controls				
t_{PCS}	Processor Control Setup Time	200	-	-	ns
t_{PCr}, t_{Pcf}	Processor Control Rise and Fall Time (Measured between 0.8 and 2.0 V)			100	ns

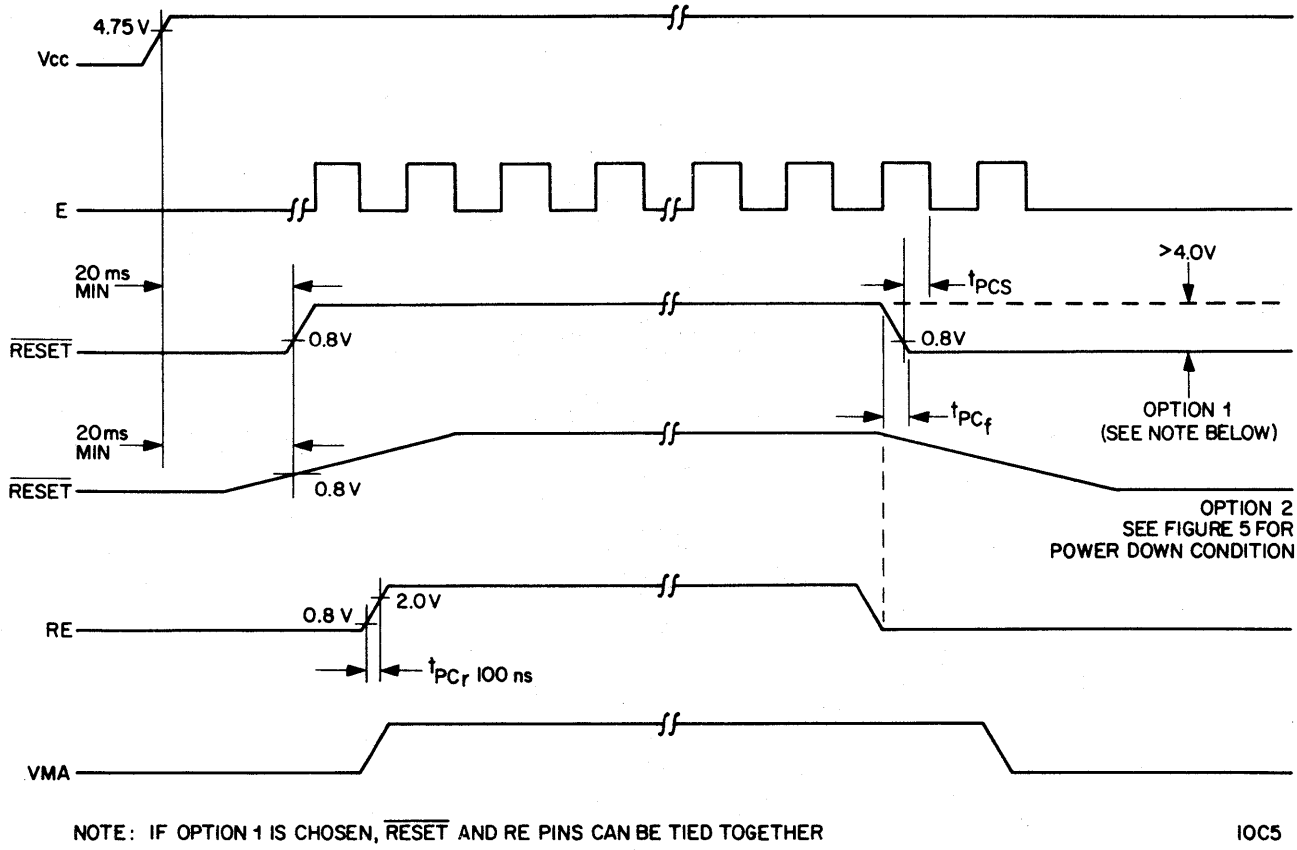


Figure 4. Power-Up and Reset Timing

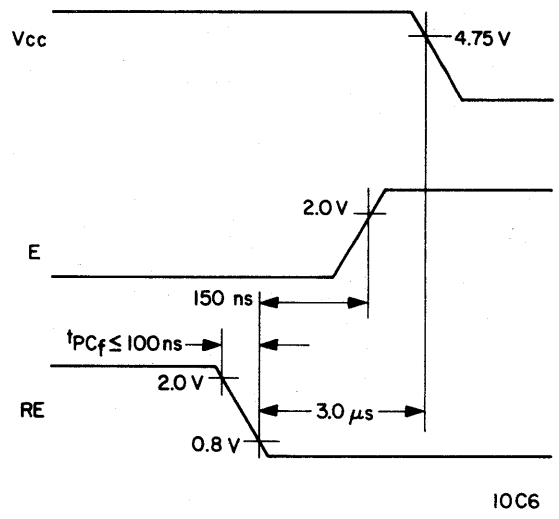


Figure 5. Power-Down Sequence

TABLE 2 - MEMORY MAP FOR INTERRUPT VECTORS

VECTOR MS	VECTOR LS	DESCRIPTION
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

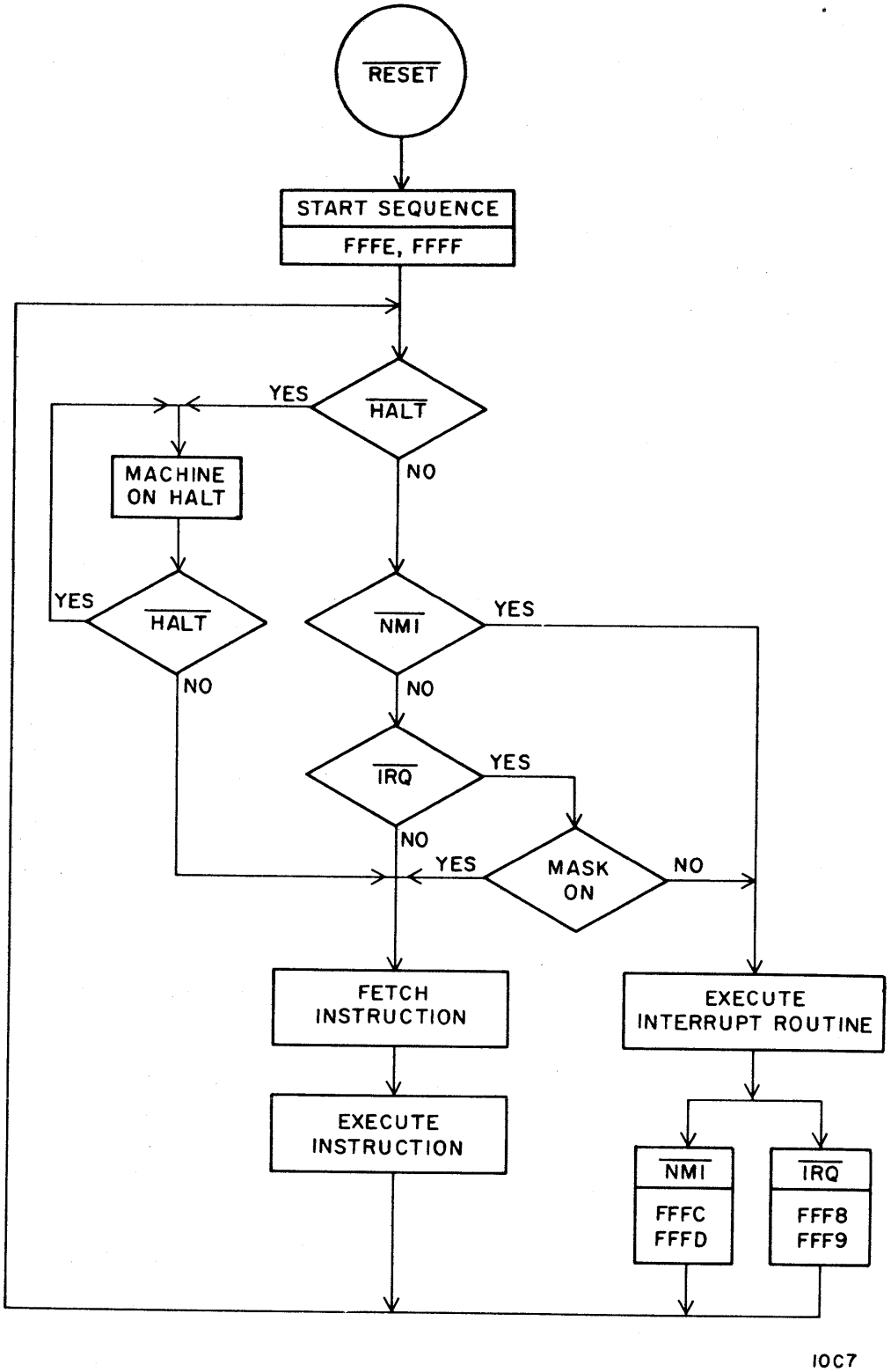


Figure 6. MPU Flowchart

MR is LOW, E may be stretched integral mul multiples of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Figure 7.

ENABLE SYSTEM (E)

This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL-compatible clock. This clock may be conditioned by a Memory Ready signal. This is equivalent to Φ2 on the 6800.

Vcc STANDBY

This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed. Maximum current drain at 5.25 V is 8 mA.

MPU ADDRESSING MODES

The 6802 8-bit microprocessing unit has seven seven address modes that can be used by a programmer, with the addressing mode a fun function of both the type of instruction and the coding within the instruction.

ACCUMULATOR (ACCX) ADDRESSING

In accumulator only addressing, either accumulator A or accumulator B is specified. These are 1-byte instructions.

IMMEDIATE ADDRESSING

In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses this location when it fetches the immediate instruction for execution. These are 2 or 3-byte instructions.

DIRECT ADDRESSING

In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are 2-byte instructions.

EXTENDED ADDRESSING

In extended addressing, the address contained in the second byte of the instruction is used as the higher eight bits of the address of the operand. The third byte of the instruct struction is used as the lower eight bits of the address for theoperand. This is an absolute address in memory. These are 3-byte instructions.

INDEXED ADDRESSING

In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are 2-byte instructions.

IMPLIED ADDRESSING

IN the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are 1-byte instructions.

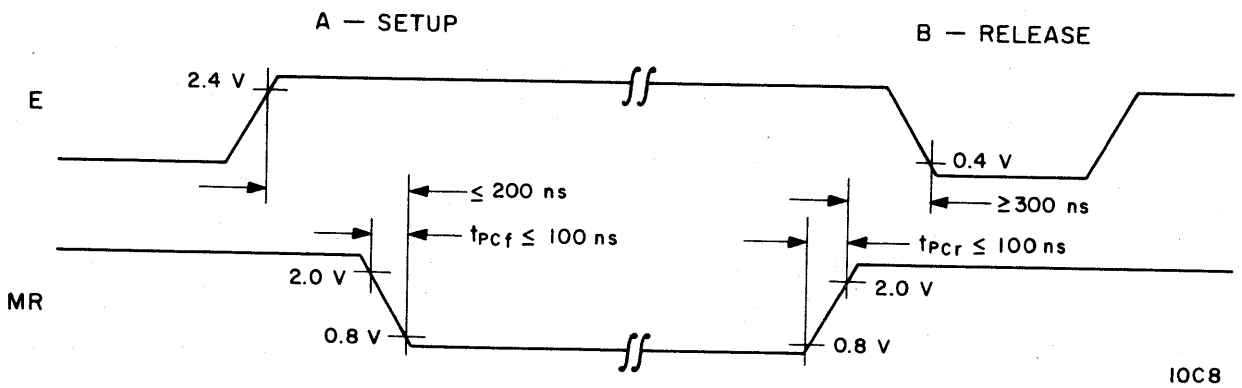


Figure 7. Memory Ready Control Function

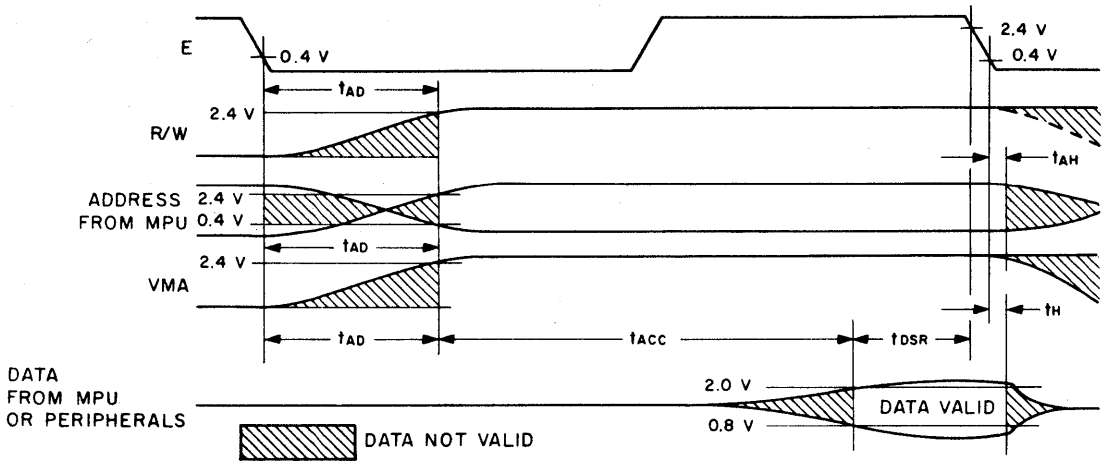
RELATIVE ADDRESSING

In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are 2-byte instructions.

DATA TIMING

Figure 8 shows Read/Write data timing for both the MPU memory and peripheral equipment.

READ DATA FROM MEMORY OR PERIPHERALS



WRITE DATA IN MEMORY OR PERIPHERALS

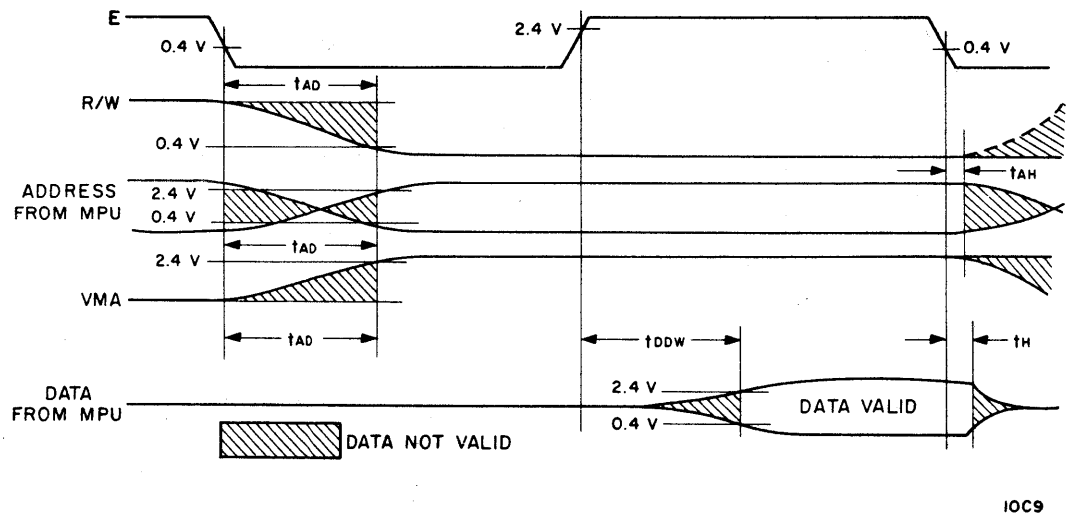


Figure 8. Read/Write Timing

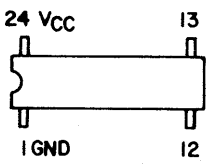
DESCRIPTION

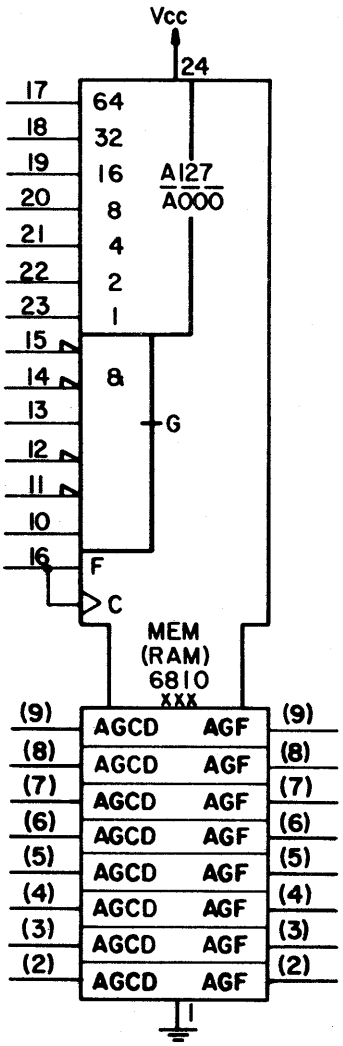
The 6810 is a TTL-compatible, 128 x 8 MOS random-access memory. Six chip select inputs (two active high, four active low) allow for memory expansion in the horizontal (word length) and/or vertical (number of words) direction. The 6810 incorporates data buffering and features three-state outputs. The memory is static and requires no refreshing.

With the 6810 selected (G active) and pin 16 high, memory data is available on the bidirectional bus and is strobed into the microporcessor by the system clock. Data is written into the 6810 on the low-to-high transition of the Write signal at pin 16. To accomplish successive Writes when G remains active, pin 16 must remain high until the address lines have settled.

NOTES:

1. Element identifier: none
2. Package pin configuration.





LOGIC SYMBOL

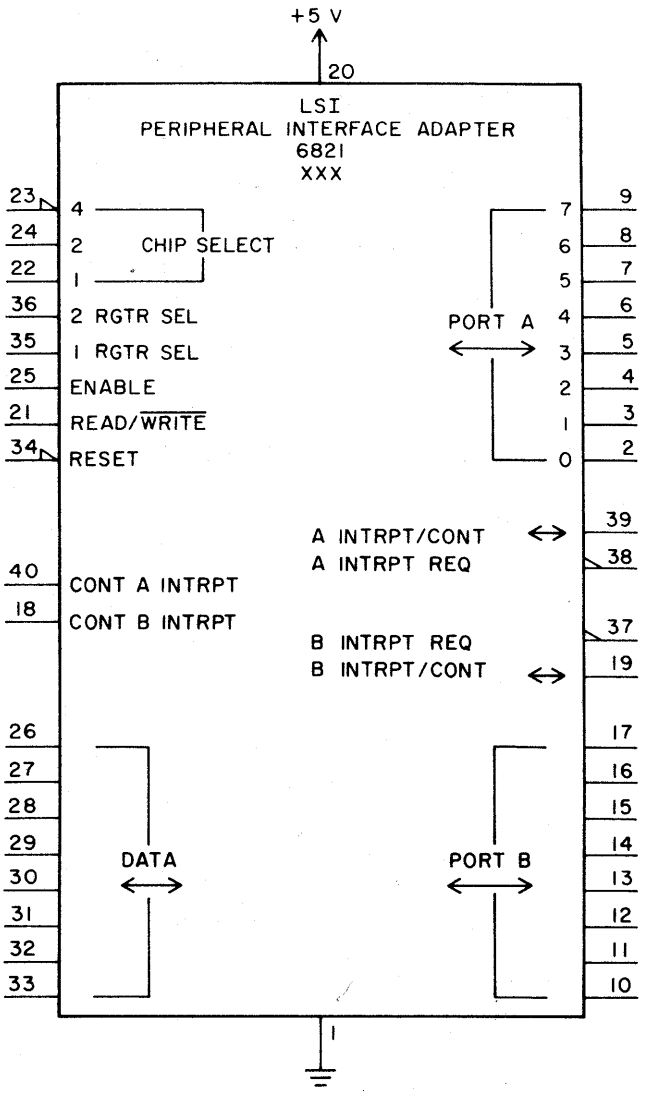
6821 PERIPHERAL INTERFACE ADAPTER (PIA)

The 6821 PIA is a member of the 6802 microprocessor (μP) family of chips. It provides a universal interface between the 6802 and its peripheral equipment. The interface is accomplished through two 8-bit bidirectional data buses and four control lines, permitting independent control over two peripheral units. In most cases, this control is effected without additional external logic.

The functional configuration of the PIA is programmed by the 6802 during system initialization. Each peripheral data line can be programmed to act as an input or an output, and each of the four interrupt/control lines can be programmed for one of several control modes. Features of the 6821 PIA include:

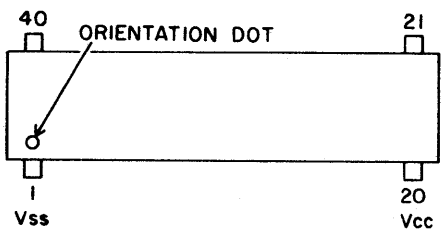
- 8-bit bidirectional data bus to μP
- Two 8-bit bidirectional data buses (Port A, Port B) for communication with separate peripheral devices
- Programmable control registers (2)
- Programmable data direction registers (2)
- Individually controlled interrrupt input lines (4), two usable as peripheral-control outputs
- Three-state and direct transistor drive lines to peripherals
- Program-controlled interrupt/interrupt disable capability
- CMOS drive capability on Port A
- Two-TTL-load capability on all Port A/B buffers

A functional block diagram of the 6821 is shown in figure 1. The abbreviated signal names shown in parentheses in that figure will be used throughout the rest of this discussion.

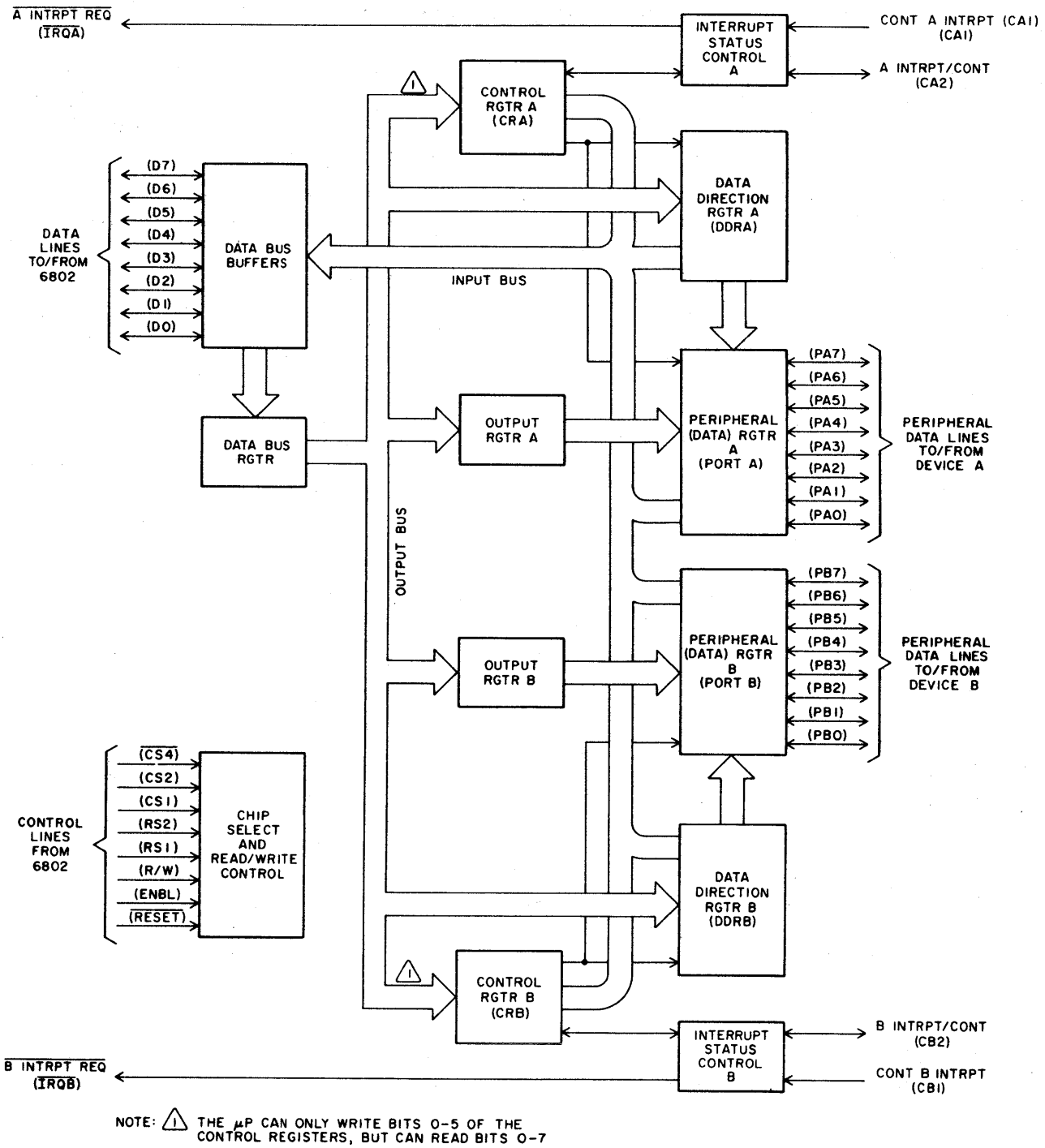


NOTES:

1. Vendor type number: 6821
2. Package pin configuration:



6821
Rev M
Sheet 1 of 8



Block Diagram, 6821 PIA.

PIA INTERFACE LINES FROM/TO MICROPROCESSOR

The PIA interface to the 6802 μP consists of an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, and read/write, enable, and reset lines. These lines, in conjunction with a valid memory address (VMA) signal from the 6802, permit the μP to have complete control over the PIA. *

BIDIRECTIONAL DATA LINES (D0-D7)

The drivers (μP input) on these lines are three-state devices that remain in the high-impedance (off) state except when the μP has programmed a PIA Read operation (Read/write line high).

ENABLE (ENBL)

The ENBL pulse is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading or trailing edges of this pulse. The ENBL pulse is normally a derivative of the 6802 phase 2 (Φ2) clock.

READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$)

This signal controls the direction of data transfers between the 6821 and the 6802. A low on the R/$\overline{\text{W}}$ line enables the PIA input buffers and data is transferred from the μP to the PIA's Data Bus register upon the appearance of the ENBL signal, provided that the PIA has been selected. A high on the R/$\overline{\text{W}}$ line sets up the drivers in the Data Bus buffers, and information is transferred from the PIA to the μP when ENBL comes up.

$\overline{\text{RESET}}$

This low-active signal clears all registers in the PIA. It can be used as a power-on reset or as a master clear during system operation.

CHIP SELECT LINES (CS1, CS2, $\overline{\text{CS4}}$)

To select the PIA, lines CS1 and CS2 must be high, and line CS4 must be low. The numbers (1, 2, 4) indicate the relative binary weighting value of the three select lines. Data transfers are then accomplished by the ENBL and R/$\overline{\text{W}}$ lines. The chip select lines must be stable throughout the duration of the ENBL pulse, for putting any of those three lines in the inactive state will deselect the PIA.

* See NOTE on sheet 8.

REGISTER SELECT LINES (RS1, RS2)

These two lines are used in conjunction with the internal Control registers to select one of the six addressable registers in the PIA. The numbers (1, 2) imply binary weighting. While in a Read or Write cycle, the register select lines must be stable for the duration of the ENBL pulse.

INTERRUPT REQUEST LINES ($\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$)

These low-active lines interrupt the 6802 either directly or through interrupt priority circuitry. Their open-collector outputs permit wired-OR connections.

Each $\overline{\text{IRQ}}$ line has two internal interrupt flag bits that can cause the respective $\overline{\text{IRQ}}$ line to go low. Each flag bit is associated with a particular interrupt line from the peripheral device. The PIA provides four interrupt enable bits that may be used to inhibit a particular interrupt coming from a peripheral device.

Servicing an interrupt may be accomplished by the μP through a software routine that sequentially reads and tests the two Control registers in the PIA for interrupt flag bits that have been set. The interrupt flags are cleared by any Read Peripheral Data operation, initiated by the 6802, for the correstponding data register (that is, Port A or Port B). Once cleared, the flag bit cannot be enabled to be set until the PIA is deselected during an ENBL pulse.

The ENBL pulse is used to condition the four interrupt lines, CA1, CA2, CB1, and CB2. When these lines are used as interrupt inputs, at least one ENBL pulse must occur between the inactive edge and the active edge of the interrupt signal to condition the edge-sensing logic. If the interrupt flag has been enabled and the edge-sensing logic properly conditioned, the flag bit will be set on the next active transition of the interrupt line.

PIA INTERFACE LINES TO/FROM DEVICES

The PIA provides two 8-bit bidirectional data buses (Port A, Port B), and four interrupt/control lines to peripheral devices.

PORT A DATA LINES (PA0-PA7)

These data lines can be individually programmed for input or output by a corresponding bit in Data Direction Register A (DDRA). A "1" bit in DDRA causes the correspondingly

numbered peripheral data line to act as an input; setting the bit to "0" causes the line to act as an output. During a μP Read Peripheral Data operation, the data on the peripheral data lines that have been programmed as inputs will appear directly at the three-state drivers of the Data Bus Buffers. Internal pull-up resistors on these drivers represent a 1.5 standard TTL load (maximum) during a Read operation.

Data in Output Register A will appear on those peripheral data lines programmed as outputs. A "1" bit in the register drives the line high, a "0" bit drives the line low. This data (from Output Register A) is also available during a Read operation. It will be read properly if the voltage on the corresponding peripheral data lines is greater than 2.0 volts for a "1" or less than 0.8 volt for a "0". Loading the output lines such that these lines do not reach full voltage causes the data transferred to the μP during a Read operation to differ from that contained in the respective bits of Output Register A.

PORT B DATA LINES (PB0-PB7)

These data lines may be programmed for input or output (using DDRB) just as for Port A. The output drivers for Port B, however, have a three-state capability, which allows them to assume the high-impedance state when the associated peripheral data lines are programmed for input. During a Read operation, data on those lines programmed as outputs will appear correctly at the Data Bus Buffers even if the voltages are below 2.0 volts for a "1".

As outputs, these lines are TTL compatible. In addition, they may be used as a source of up to 1 mA at 1.5 V to directly drive the base of a transistor switch.

INTERRUPT INPUT LINES (CA1, CB1)

Lines CA1 and CB1 are input lines only and set interrupt bit 7 in the associated Control register. The active transition (↑,↓) for these signals is also programmed by the control registers.

A INTERRUPT/CONTROL (CA2)

This line may be programmed to act as an interrupt input or as a peripheral control output. As an output, the line is TTL compatible. As an input, the internal pull-up resistor represents a 1.5 standard TTL load. The function of CA2 is programmed by Control Register A.

B INTERRUPT/CONTROL (CB2)

Like CA2, this line may also be programmed as an input or output. As either an interrupt input or peripheral control output, the line is TTL compatible. In addition, it may be used during an output to source up to 1 mA at 1.5 V to directly drive the base of a transistor switch. In this respect, it matches the output capabilities of the Port B data lines. This line is programmed by Control Register B.

INTERNAL CONTROLS

The PIA contains six addressable registers -- those accessible to the 6802 data bus: two peripheral (data) registers, two control registers, and two data direction registers. Selection of these registers is controlled by register select lines RS1 and RS2, together with bit 2 in the corresponding Control register, as shown in table 1.

TABLE 1. INTERNAL ADDRESSING

RS2	RS1	Control Register Bit		Location Selected
		CRA-2	CRB-2	
0	0	1	X	Peripheral (Data) Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral (Data) Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't care

INITIALIZATION

A low on the $\overline{\text{RESET}}$ line clears all PIA registers. This sets PA0-PA7, PB0-PB7, CA2, and CB2 as inputs, and disables all interrupts. The PIA must be configured during the restart program that follows the reset pulse.

Possible configurations for the Data Direction and Control registers follow.

DATA DIRECTION REGISTERS (DDRA, DDRB)

These registers allow the 6802 μp to control the direction of data on each peripheral data line. Any DDR bit set to "0" makes the corresponding data line act as an input; a "0" results in the line acting as an output.

CONTROL REGISTERS (CRA, CRB)

These two registers allow the 6802 μP to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition, these registers allow the μP to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of these registers may be written or read by the μP when the proper chip select and register select signals are activated. Bits 6 and 7 are for reading only, and are modified by the peripheral interrupt signals that appear on control lines CA1, CA2, CB1, and CB2. The format of the control word stored in these registers is shown in table 2.

Data Direction Access Control Bits (CRA-2, CRB-2)

Bit 2 in each control register allows the selection of either the peripheral interface register (hereafter called the Data register), or the Data Direction register when the proper register select lines are activated (see table 1).

Interrupt Flag Bits (CRA-7, CRA-6, CRB-7, CRB-6)

These four interrupt flag bits are set by active transitions on interrupt lines CA1 or CB1, or on interrupt/control lines CA2 or CB2 when those two lines are programmed as inputs. Line CA1 (CB1) sets control register bit CRA-7 (CRB-7), while line CA2 (CB2) sets bit CRA-6 (CRB-6).

How bits 7 and 6 of the control registers are set by interrupt inputs is shown in tables 3 and 4, respectively. As implied earlier, these bits cannot be set from the 6802 data bus; they will be cleared, however, by a Read Peripheral (Data) Register operation for the appropriate port.

Control of CA1 and CB1 Interrupt Input Lines --

The two low-order bits of the control registers (CRA-0, CRA-1, CRB-0, CRB-1) control the effect that an active transition on interrupt lines CA1 or CB1 will have on the respective Interrupt Request to the μP. As seen in table 3, CRA-0 (CRB-0) enables the IRQ and CRA-1 (CRB-1) determines whether a positive-going or negative-going transition on the interrupt line will set the interrupt flag (bit 7 of the control register).

Control of CA2 and CB2 Interrupt/Control Lines --

Bits 3, 4, and 5 of the control registers are used to control CA2 and CB2. Bit 5 (CRA-5, CRB-5), if low, makes the line an interrupt input. In this situation, as shown in table 4, bit 3 enables the IRQ and bit 4 determines the active transition of the interrupt line.

TABLE 2. CONTROL WORD FORMAT

CR Bits	7	6	5	4	3	2	1	0
CRA	IRQA-1	IRQA-2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB-1	IRQB-2	CB2 Control			DDRB Access	CB1 Control	

TABLE 3. CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	µP Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled -- $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the Interrupt Flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled -- $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the Interrupt Flag bit CRA-7 (CRB-7) goes high

NOTES:

1. ↓ = High-to-low transition
2. ↑ = Low-to-high transition
3. Interrupt Flag bits CRA-7 and CRB-7 are cleared by a Read Peripheral Data operation for the corresponding port.
4. If an interrupt occurs when IRQ is disabled (Control register bit 0 is low), IRQA (IRQB) occurs after CRA-0 (CRB-0) is brought high.

TABLE 4. CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA-5 (CRB-5) IS LOW

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	µP Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled -- $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the Interrupt Flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled -- $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the Interrupt Flag bit CRA-6 (CRB-6) goes high.

NOTES:

1. ↓ = High-to-low transition
2. ↑ = Low-to-high transition
3. Interrupt Flag bits CRA-6 and CRB-6 are cleared by a Read Peripheral Data operation for the corresponding port.
4. If an interrupt occurs when IRQ is disabled (control register bit 3 is low), IRQA (IRQB) occurs after CRA-3 (CRB-3) is brought high.

When bit 5 is high, CA2 (CB2) becomes an output that can be used to control the peripheral device. In the output mode, CB2 and CA2 have slightly different characteristics, as seen in tables 5 and 6:

TABLE 5. CONTROL OF CB2 AS AN OUTPUT
CRB-5 IS HIGH

CRB-5	CRB-4	CRB-3	CB2	
			Cleared	Set
1	0	0	Low on ↑ of first ENBL pulse following a µP Write Data Register B operation.	High when Interrupt Flag bit CRB-7 is set by an active transition of CB1.
1	0	1	Low on ↑ of first ENBL pulse following a µP Write Data Register B operation.	High on ↑ of first ENBL pulse following an ENBL pulse that occurred while the port was deselected.
1	1	0	Low when CRB-3 goes low as a result of a µP Write Control Register B operation.	Always low as long as CRB-3 is low. Will go high on a µP Write Control Register B operation that changes CRB-3 to a "1" (high).
1	1	1	Always high as long as CRB-3 is high. Will go low when a µP Write Control Register B operation results in setting CRB-3 to a "0" (low).	High when CRB-3 goes high as a result of a µP Write Control Register B operation.

NOTES: ↑ = Low-to-high transition

TABLE 6. CONTROL OF CA2 AS AN OUTPUT
CRA-5 IS HIGH

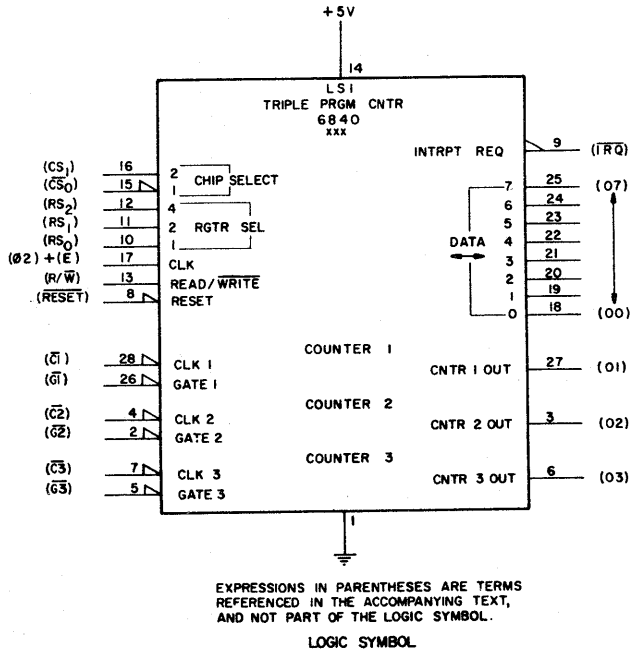
CRA-5	CRA-4	CRA-3	CA2	
			Cleared	Set
1	0	0	Low on ↓ of ENBL pulse following a µP Read Data Register A operation	High when Interrupt Flag bit CRA-7 is set by an active transition of CA1 signal.
1	0	1	Low on ↓ of ENBL pulse following a µP Read Data Register A operation.	High on the negative edge of an ENBL pulse that occurs during a deselect.
1	1	0	Low when CRA-3 goes low as the result of a µP Write Control Register A operation.	Always low as long as CRA-3 is low. Will go high on a µP Write Control Register A operation that sets CRA-3 to a "1" (high)
1	1	1	Always high as long as CRA-3 is high. Will go low on a µP Write Control Register A operation that sets CRA-3 to a "0" (low).	High when CRA-3 goes high as the result of a µP Write Control Register A operation.

NOTES: ↓ = High-to-low transition

NOTE: The three chip select inputs are normally tied to the 6802 address lines in accordance with the peripheral addressing configuration used by the μP. It is customary to AND one of the address lines with the VMA signal (also from the 6802), and to feed the result into one of the chip select inputs.

DESCRIPTION

The 6840 is a programmable timing module (PTM) that is controlled by Load and Store instructions from the 6800/6802 MPU. It contains three independent timers, each 16 bits wide and capable of holding a maximum count of 65,535 (decimal). The PTM has a variety of applications, but all involve either pulse generations or time-interval comparisons, both of which depend upon decrementing a count that has been preset in the timer. To provide the widest possible latitude in these functions, each timer can select as its clocking (decrementing) input either the Enable System clock (E, or Φ2) from the MPU or any signal that is connected to its External Clock ($\overline{C}$) input pin. For accurate clocking, the $\overline{C}$ frequency should not exceed one-half that of E (Φ2), since E is used to resync $\overline{C}$ with the system. More about that later.



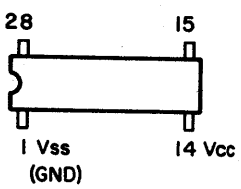
As shown in the block diagram, figure 1, each timer consists of four elements.

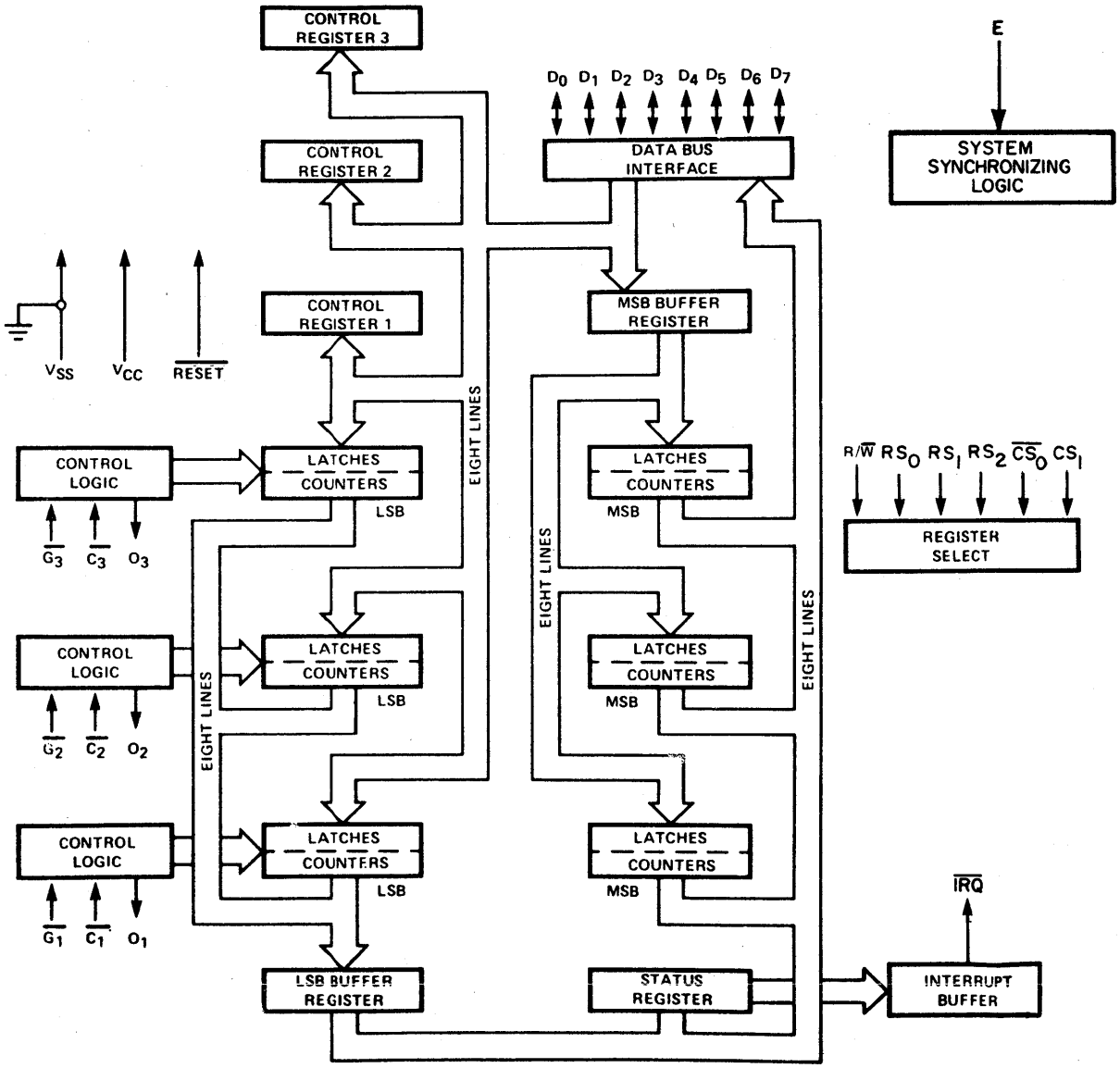
- a control register that determines its counting mode
- a set of 16 bit latches (Timer Latches)
- a 16-bit counter (Timer Counter)
- gating and clocking logic

Information is written into the timer latches by the MPU and transferred to the timer counter by a counter initialization (CI) cycle. Contents of the counters can be read by the MPU at any time, and interrupts may be set if certain conditions occur during the count down.

NOTES:

1. Element identifier (for reference only: 587
2. Package pin configuration:




CONTROL REGISTER 3
CONTROL REGISTER 2
CONTROL REGISTER 1
DATA BUS INTERFACE
MSB BUFFER REGISTER
SYSTEM SYNCHRONIZING LOGIC
E
D0 D1 D2 D3 D4 D5 D6 D7
VSS
VCC
RESET
CONTROL LOGIC
LATCHES COUNTERS
LSB
MSB
G3 C3 O3
G2 C2 O2
G1 C1 O1
EIGHT LINES
R/W RS0 RS1 RS2 CS0 CS1
REGISTER SELECT
LSB BUFFER REGISTER
STATUS REGISTER
INTERRUPT BUFFER
IRQ

REGISTER SELECTION

Register selections, as well as the various PTM Read/Write functions, are defined in table 1. There are nine register selections to be made for Write, but only three Register Select lines available for the task. To solve this situation, the RS_0=RS_1=RS_2=0 condition selects either of two registers, depending upon the state of Bit 0 in Control Register 2 ($CR2_0$).

REGISTER LOADING

With respect to the MPU, the Control Registers and Timer Latches are write-only, although both are affected by a Reset command from the MPU. Because the timer latches are 16 bits wide, two-byte write instructions (e.g. STX, STS) are required to load them. (Refer to table 1.) First, a Write MSB Buffer Register command stores the Most Significant Byte in the MSB buffer. Then, as the Least Significent Byte is loaded directly into the lower eight latches by a Write Timer X Latches command, data from the MSB buffer is simultaneously transferred to the upper eight latches.

REGISTER READING

With respect to the MPU, the Status Register and the Timer Counters are read-only, although both can be cleared by a Reset command from the MPU. Again, two-byte data instructions (e.g., LDX, LDS) are required to transfer the 16-bit contents of a timer counter to the Data Bus Interface. First, the upper bits of the counter are transmitted to the MPU by a Read Timer X Counter command; then the relevant Read LSB Buffer Register command (one of three) transfers the lower eight bits via the LSB Buffer.

The Status Register contains an Interrupt flag bit for each timer, plus an Interrupt Request bit ($\overline{IRQ}$) that is a composite of the individual timer flags. When the Status Register is read, the four unused bits at the top of the register are transferred as ls. (The interrupt flags are discussed below under Operating Modes.)

CONTROL REGISTERS

The three control registers define the operating mode, and control the operation,

TABLE 1. REGISTER SELECTIONS

Register Select Bits			Operations	
RS_2	RS_1	RS_0	$R/\overline{W}$ = 0	$R/\overline{W}$ = 1
0	0	0	$CR2_0$=0 Write Control Register 3	No Operation
			$CR2_0$=1 Write Control Register 1	
0	0	1	Write Control Register 2	Read Status Register
0	1	0	Write MSB Buffer Register	Read Timer 1 Counter
0	1	1	Write Timer 1 Latches	Read LSB Buffer Register
1	0	0	Write MSB Buffer Register	Read Timer 2 Counter
1	0	1	Write Timer 2 Latches	Read LSB Buffer Counter
1	1	0	Write MSB Buffer Register	Read Timer 3 Counter
1	1	1	Write Timer 3 Latches	Read LSB Buffer Register

of the timers. The bit functions are defined in table 2. Note that for each control register, Bit 0 has a unique function. Other bits, 1 through 7, have common functions for each timer.

Bit 0 of Control Register 1 ($CR1_0$) is the Internal Reset bit. It is the only bit in all of the control registers that is not cleared out by a Reset command from the MPU. It is cleared (or set) only when the MPU writes into that control register.

TABLE 2. CONTROL REGISTER BITS

Bit Designation & Value	Name/Function
$CR1_0$	Internal Reset
0	All timers allowed to operate
1	All timers held in preset state
$CR2_0$	Control Register Address
0	CR#3 may be written
1	CR#1 may be written
$CR3_0$	Timer 3 Clock Control
0	Timer 3 clock is not prescaled
1	Timer 3 clock is prescaled by ÷8
CRX_1	Timer X Clock Source
0	Timer X uses Cx input as clock source
1	Timer X uses Enable System (E) as clock source
CRX_2	Timer X counting Mode Control
0	Timer X configured for 16-bit mode
1	Timer X configured for dual 8-bit mode
CRX_3 CRX_4 CRX_5	Timer X Operating Mode and Interrupt Control (see table 3)
CRX_6	Timer X Interrupt Enable
0	Timer X Interrupt Flag masked on $\overline{IRQ}$
1	Timer X Interrupt Flag enabled to $\overline{IRQ}$
CRX_7 (1)	Timer X Counter Output Enable
0	Timer X Output masked on output Ox.
1	Timer X Output enabled to output Ox.

NOTE (1) Operation of the timer Counter, and read-out to the Data Bus Interface, is not affected by the state of CRX_7.

Bit 0 of Control register 2 ($CR2_0$) selects one of two other control registers, as mentioned earlier.

Bit 0 of Control Register 3 ($CR3_0$) controls the Prescaler function unique to Timer 3. If $CR3_0$=1, a divide-by-8 counter is interposed between the timer clock input (either E or $\overline{C3}$) and the timer counter. As a result, the counter decrements once for every eight clock pulses.

INPUT/OUTPUT LINES

BUS INTERFACE

The bus interface comprises those I/O lines that connect to the MPU bus. They are shown in the top half of the logic symbol. Output drivers on the Data Bus interface are 3-state, while the $\overline{IRQ}$ output is an "open drain" FET. Both allow wired-OR connections to similar lines from other devices in the 6800 family. As indicated in table 2, the $\overline{IRQ}$ line will not reflect the presence of a timer's Interrupt flag unless Bit 6 in the associated control register is set (CRX_6=1).

A high-to low-level transition on the Reset line has the following effects:

1. All timer latches are preset to maximum (65,535).
2. All counters are preset to the value in their latches.
3. All counter outputs are cleared and all counter clocks disabled (Counter Enable FF--CE--reset).
4. All Status Register bits (Interrupt flags) are cleared.
5. All Control Register bits cleared except the Internal Reset bit ($CR1_0$), which is set.

EXTERNAL I/O LINES

The external I/O lines are shown in the lower half of the logic symbol. The Clock and Gate inputs ($\overline{C_x}$, $\overline{G_x}$), which come from a source other than the MPU, must be synchronized with the Enable System (E) clock in order to be recognized by the PTM. This takes three to four E periods, depending upon system jitter. In the case of a $\overline{C}$ input, the E pulse following the synchronization decrements the counter.

A high-to low-level transition on the Gate input is one method of initializing a counter; that is, transferring the contents of the timer latches to the timer counter and starting the "countdown".

OPERATING MODES

Control Register bits 3, 4, and 5 set the four operating modes of each timer, as seen in table 3. Unused bits in the table are used to modify counter initialization and interrupt enable conditions, as defined in subsequent tables under the various mode descriptions.

PULSE-GENERATING MODES

The continuous and single-shot modes are both used to generate pulses. Of the four timer modes, it is only for these two that the timer outputs ($O1$—$O3$) are functional.

Continuous Mode

Control Register bit settings for the continuous mode are given in table 4, and the output waveforms in figure 2. Note that CRX_2 determines the counting mode, either 16-bit or dual 8-bit. In the 16-bit counting mode (CRX_2=0), a square wave is produced, the duration of which is determined by the value (N) set in the timer. If N=0, the output is zero.

In the dual 8-bit counting mode, provided that both the MSB and LSB values preset in the latches are non-zero, a pulse train is produced wherein the duration of each pulse is governed by the value of L (LSB, see figure 2), and the space between each pulse is determined by M(L+1)+1. If either M or L (or both) are zero, square waves are produced.

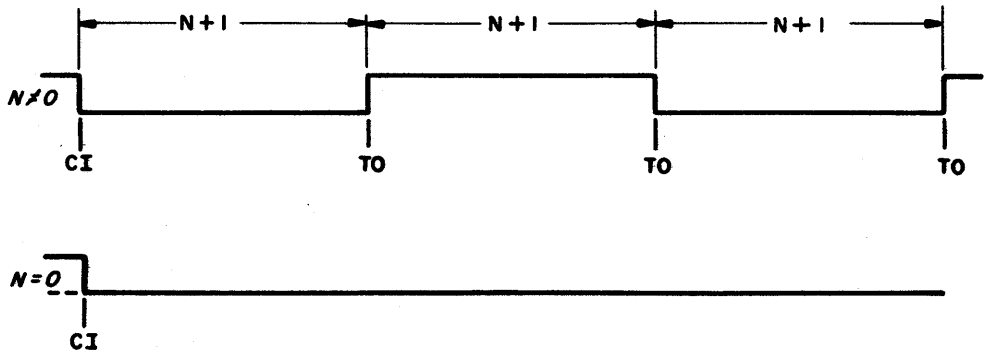
Single-Shot Mode

The Single-Shot mode is the same as the continuous mode except for three differences:

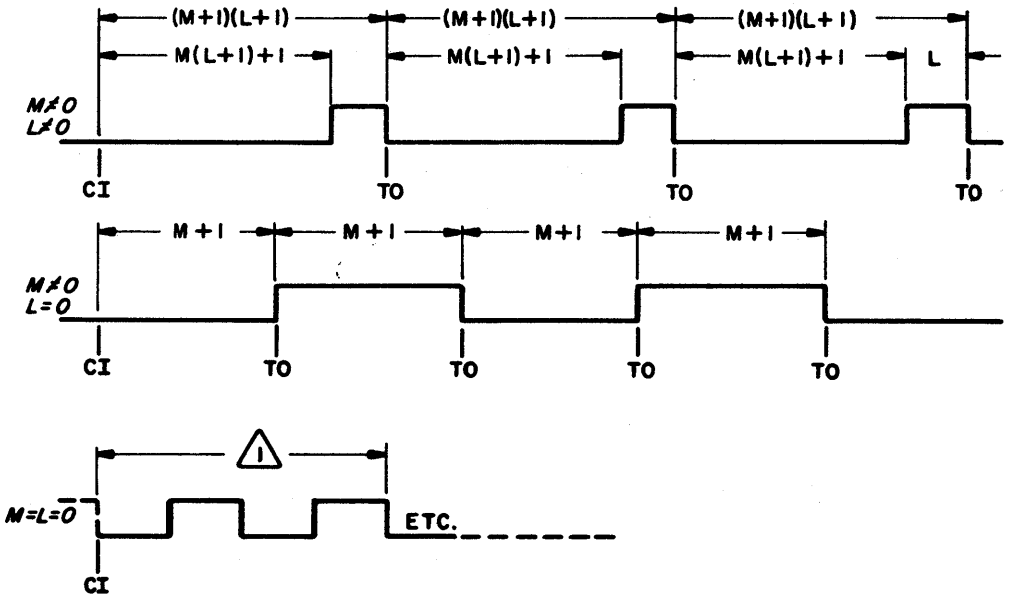
1. After one output pulse, Ox remains LOW until the next counter initialization.

TABLE 3. OPERATING MODES

Control Register			
CRX_3	CRX_4	CRX_5	Operating Mode
0	-	0	Continuous
0	-	1	Single-Shot
1	0	-	Frequency Comparison
1	1	-	Pulse-Width Comparison



16—BIT COUNTING MODE



DUAL 8—BIT COUNTING MODE

NOTES:

N = 16—BIT CONTENTS OF COUNTER

M = 8—BIT NUMBER IN MSB

L = 8—BIT NUMBER IN LSB

CI = COUNTER INITTALIZATION

TO = COUNTER TIMEOUT

1 OUTPUT TOGGLES AT 1/2 THE CLOCK FREQUENCY

Figure 2. Output Waveforms, Continuous Mode

TABLE 4. CONTINUOUS MODE

Preconditions: CRX_3=0, CRX_5=0, CRX_7=1		NOTE: After initialization (or reinitialization), G must be LOW for the counter to decrement.	
CR Bits		Counter Initialization	Counter Mode
CRX_2	CRX_4		
0	0	$\overline{G}\downarrow$ + W + R	16-bit
0	1	$\overline{G}\downarrow$ + R	
1	0	$\overline{G}\downarrow$ + W + R	Dual 8-bit
1	1	$\overline{G}\downarrow$ + R	

NOTES: $\overline{G}\downarrow$ = Negative transition of Gate Pulse

W = Write Timer X Latches command

R = Timer Reset (CRl_0=1 or Reset on pin 8)

2. Counter action (counter enable) is not dependent upon G remaining LOW.

3. If M=L=O (or N=0), counter output is disabled.

The Control Register bit settings for the Single-Shot mode are given in table 5. Output waveforms are shown in figure 3.

TIME-INTERVAL MODES

The two time-interval modes differ from the two pulse-generating modes in that interrupts can be generated not only by a counter time-out, but also by transitions of the Gate input. Moreover, these transitions can be negative-going or positive-going, depending upon the specific time-interval mode.

Aside from minor variations in counter initialization, there is one basic difference between the two time-interval modes. Stated simply, that difference is this:

- In the Frequency Measurement mode, frequency is determined by the interval between successive negative-going transitions on the $\overline{G}$ input.
- In the Pulse-Width Comparison mode, the width of the pulse is determined by the time that the $\overline{G}$ input, having gone LOW, remains LOW.

As stated previously, output pulses (O_X) are not defined for these modes.

Frequency Measurement Mode

The Control Register bits for setting up the Frequency Measurement mode are shown in table 6. Note that CRX_5 determines whether the Interrupt flag is set on a counter time-out (TO) or a Gate transition. When CRX_5=O, a counter time-out occurring prior to the negative-going Gate signal will recycle the counter, starting another count down. In any event, the count stops when Gate goes LOW, and the Interrupt flag is set. Another counter initialization cannot occur until the Interrupt has been reset.

If CRX_5=1, the counter will be recycled if Gate goes LOW before the counter times out. If TO occurs before $\overline{G}$, the Interrupt flag is set and the counter halts.

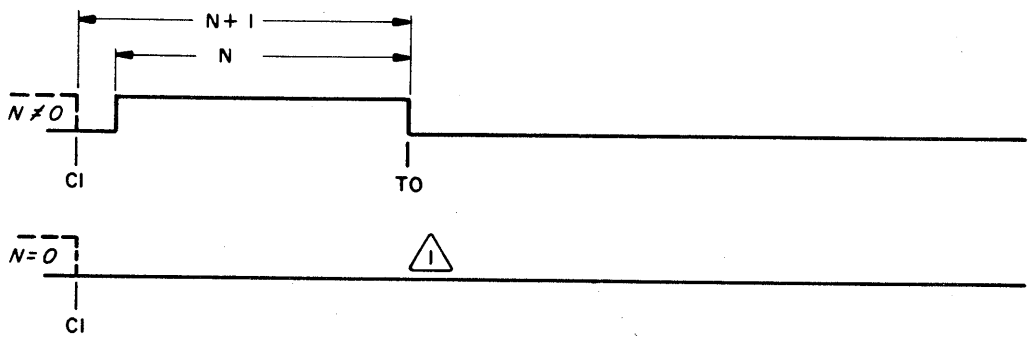
In either case, a Reset pulse (CRl_0=1 or External Reset at pin 8) must first be issued to clear the Interrupt flag and initialize the counter. At this point the next $\overline{G}\downarrow$ signal will set the Counter Enable FF, thereby allowing the timer to decrement with each Clock input.

Pulse-Width Comparison Mode

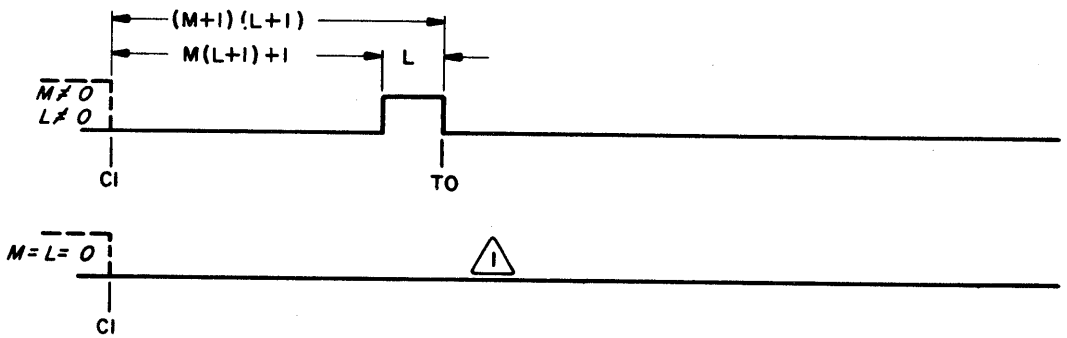
Table 7 depicts the set-up for this mode. Again, CRX_5 determines whether an Interrupt will be caused by a counter time-out or a positive-going transition at the Gate input. In other respects, this mode is similar to Frequency Measurement.

TABLE 5. SINGLE-SHOT MODE

Preconditions: CRX_3=0, CRX_5=1, CRX_7=1		NOTE: After initialization, counter operation is not dependent upon $\overline{G}$ remaining LOW.	
CR Bits		Counter Initialization	Counting Mode
CRX_2	CRX_4		
0	0	$\overline{G}\downarrow$ + W + R	16-bit
0	1	$\overline{G}\downarrow$ + R	
1	0	$\overline{G}\downarrow$ + W + R	Dual 8-bit
1	11	$\overline{G}\downarrow$ + R	



16-BIT COUNTING MODE



DUAL 8-BIT COUNTING MODE

NOTES

1. TIME OUTS OCCUR AT END OF EVERY CLOCK PERIOD.
2. FOR INTERPRETATION OF EXPRESSIONS, SEE FIGURE 2.

Figure 3. Output Waveforms, Single-Shot Mode

TABLE 6. FREQUENCY MEASUREMENT MODE

Preconditions:
CRX_3=1
CRX_4=0

CRX_5	Counter Initialization	CE FF Set	CE FF Reset	Interrupt Flag Set (I)
0	$\overline{G}\downarrow \cdot \overline{I} \cdot (\overline{CE}+TO \cdot CE) + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	W + R + I	$\overline{G}\downarrow$ before TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	W + R + I	TO before $\overline{G}\downarrow$

CE = Counter Enable (flip-flop)
TO = Timeout
for other symbols, see Table 4

TABLE 7. PULSE-WIDTH COMPARISON MODE

Preconditions:
CRX_3=1
CRX_4=1

CRX_5	Counter Initialization	CE FF Set	CE FF Reset	Interrupt Flag Set (I)
0	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	W + I + R + G	$\overline{G}\uparrow$ before TO
1	$\overline{G}\downarrow \cdot \overline{I} + R$	$\overline{G}\downarrow \cdot \overline{W} \cdot \overline{R} \cdot \overline{I}$	W + I + R + G	TO before $\overline{G}\uparrow$

DESCRIPTION

The 6875 is a clock generator/driver that provides non-overlapping Φ1 and Φ2 clock signals for the 6800 microporcessor. The 6875 is compatible with 1.0, 1.5, or 2.0 MHz versions of the 6800.

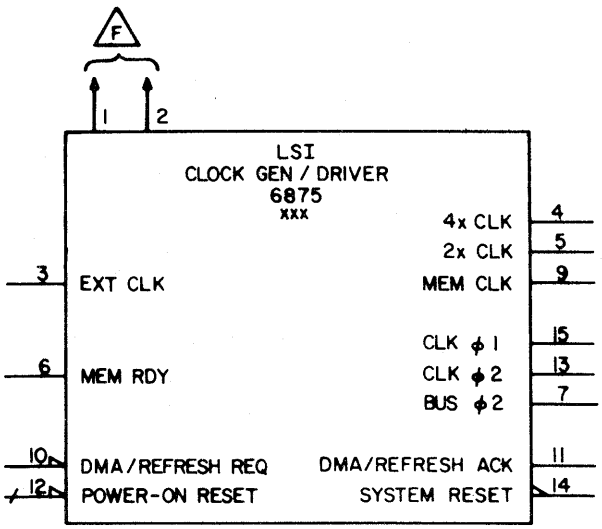
For crystal operation, a tank circuit tuned to the desired crystal frequency, 4 x CLK, is connected between pins 1 and 2; pin 3 is grounded. For operation as an R-C oscillator, the resistor is connected between pins 1 and 2, and the capacitor between pin 2 and ground. Again, pin 3 is grounded. T The 6875 may also be excited by an external pulse generator, the output of which is connected to pin 3. In this mode, pin 1 is left open and pin 2 is grounded. Figure 1 is a simplified logic diagram of the 6875.

Figures 2 and 3 show the 6875 timing when only static memories are used in conjunction with the 6800 microprocessor. (Static memories require no refreshing.) In figure 2, the memory speed is compatible with that of the microprocessor, and so there is no need to extend (stretch) the 6800's machine cycle during memory references. Figure 3 shows how the cycle is stretched when slow memories are used. Memory Ready goes low to extend all clock output pulses during these slow-memory references.

Note that in figure 3 the DMA/Refresh Request signal is shown going low at the same time as Memory Ready. It is during these dynamic memory access (DMA) extensions that the row-addressed cells of all dynamic memories are refreshed. As will be seen in figure 4, however, these refresh cycles do not affect the Memory Clock. The extension of Memory Clock in figure 3 is entirely the result of bringing Memory Ready low.

Figure 4 shows how the DMA/Refresh Request signal is used by the 6875 to stretch dynamic-memory cycles. During the DMA or refresh period, the microprocessor's Φ1 and Φ2 clocks must stay in sync with the memory cycle, as referenced to Memory Clock. Maintaining the integrity of Memory Clock provides this reference to the 6800.

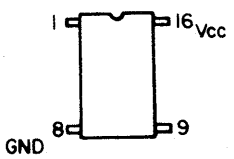
Figure 5 shows how a System Reset pulse is generated when power is first applied. Reference levels are given for positive logic voltage levels, although the Reset pulse itself is low-going.



LOGIC SYMBOL

NOTES:

1. Element identifier: none
2. Package pin configuration.



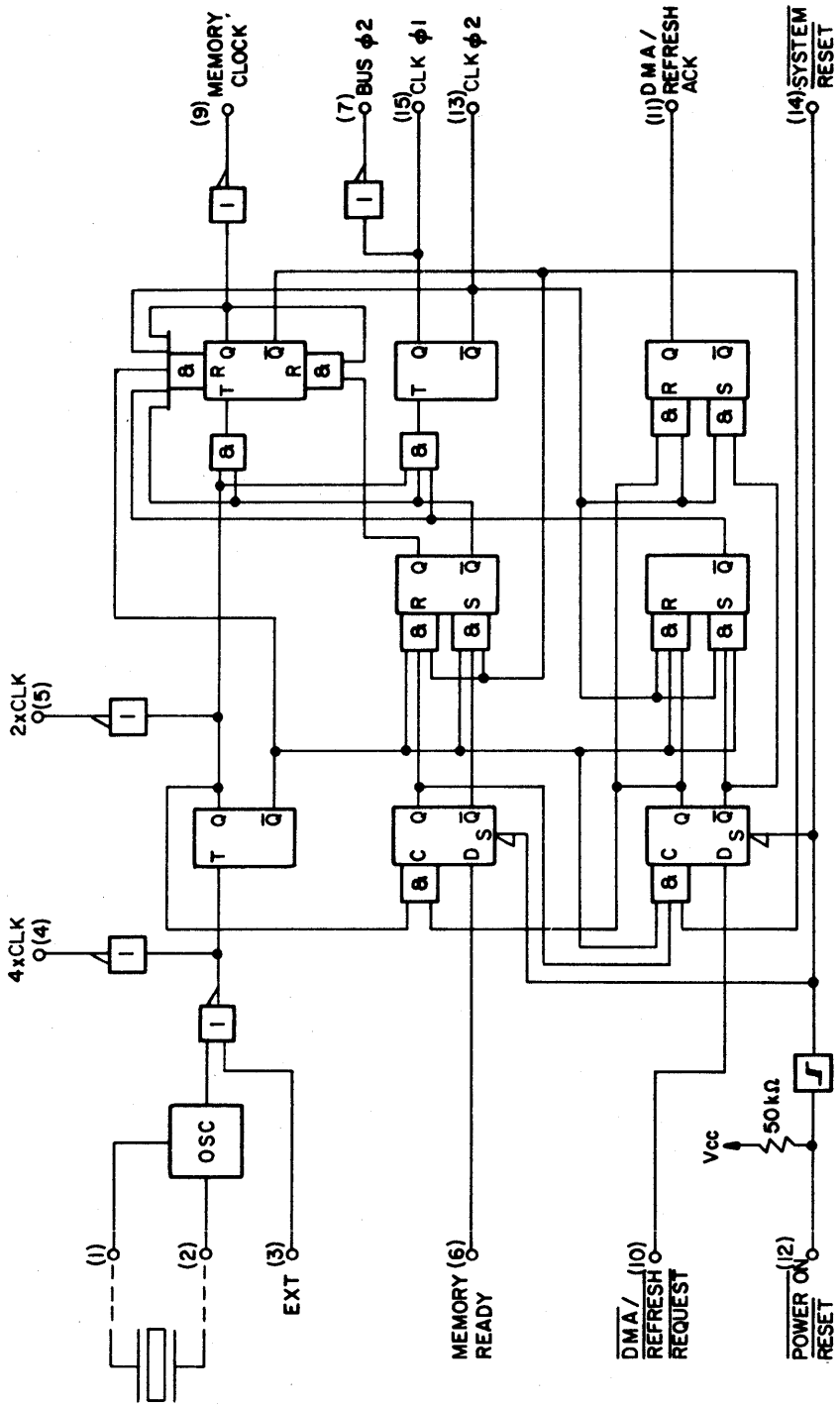
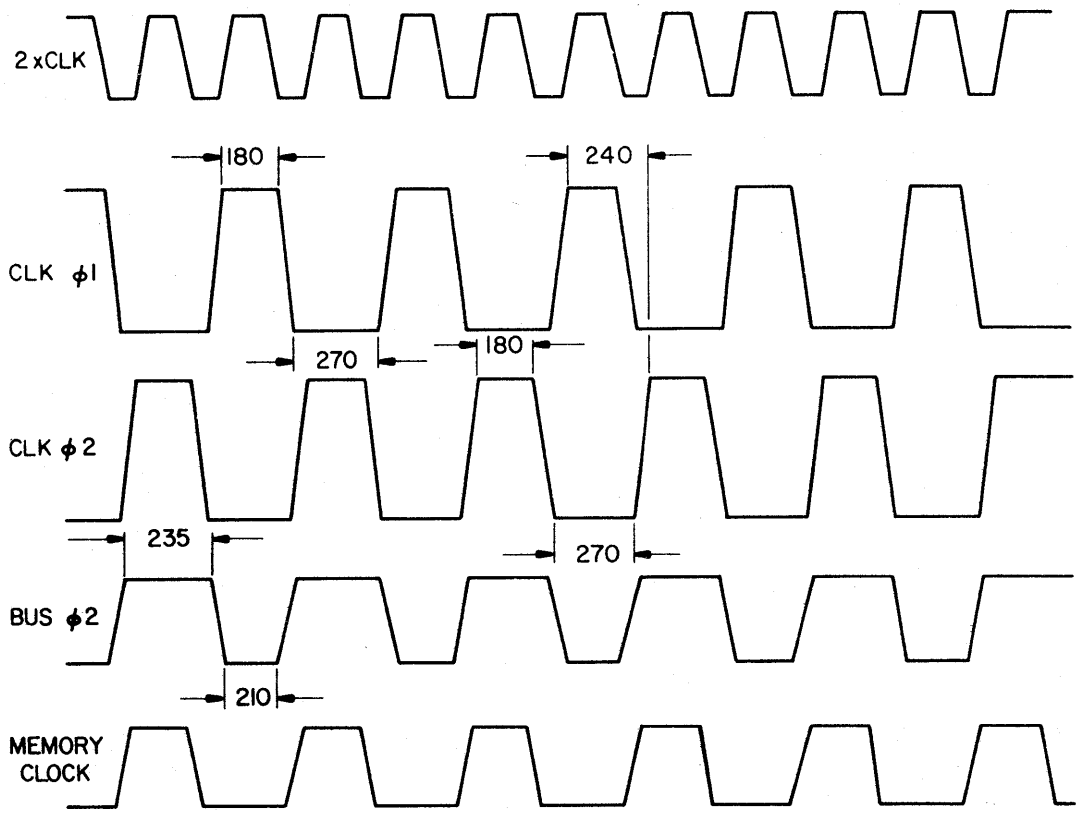


Figure 1. 6875 Logic Diagram



NOTE:
1. TIMES ARE IN NANOSECONDS FOR fo=2MHz

Figure 2. Non-Stretched Operation
(Memory Ready and DMA/Refresh Request held high)

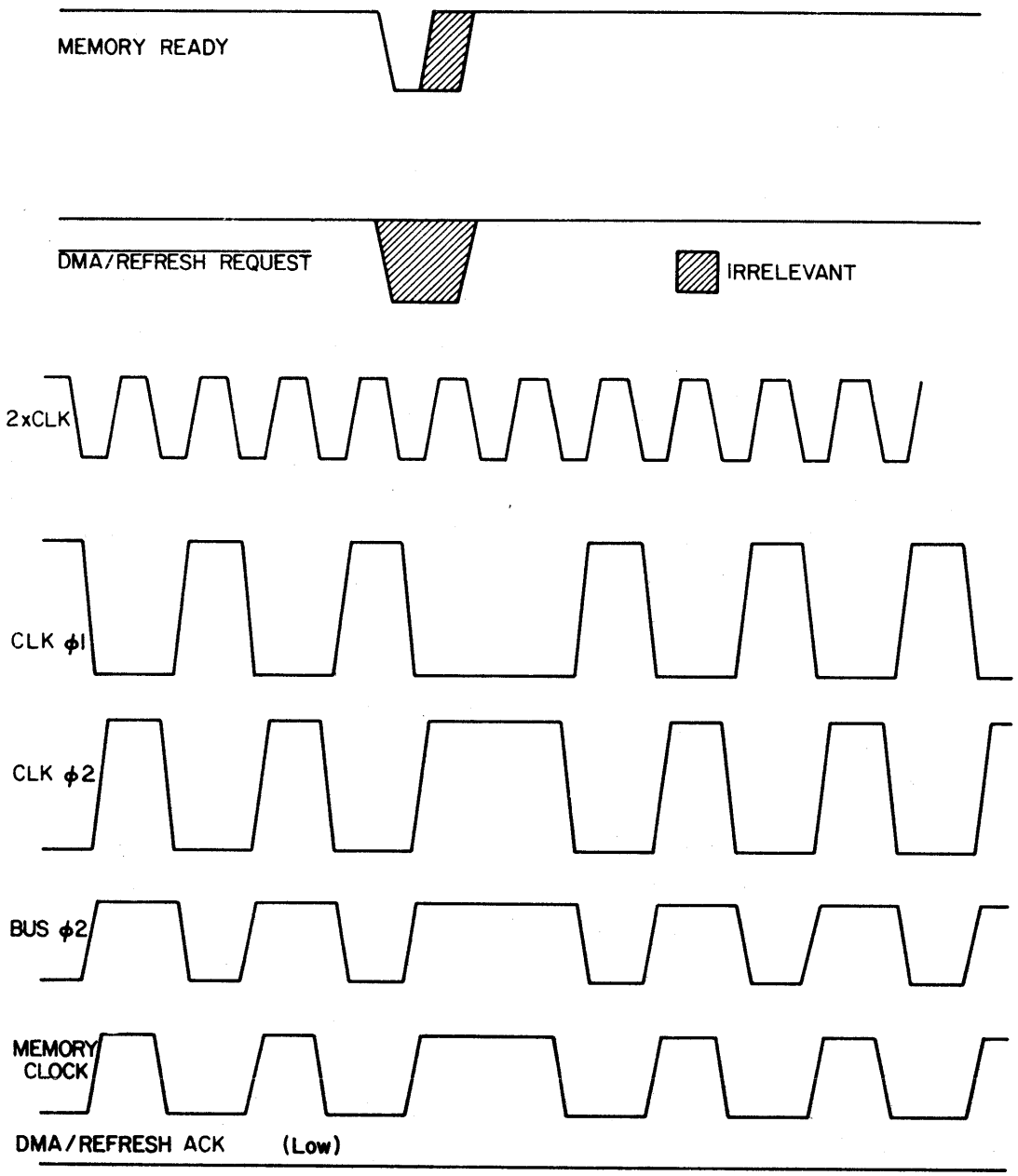


Figure 3. Memory Ready Stretch Operation (minimum stretch shown)

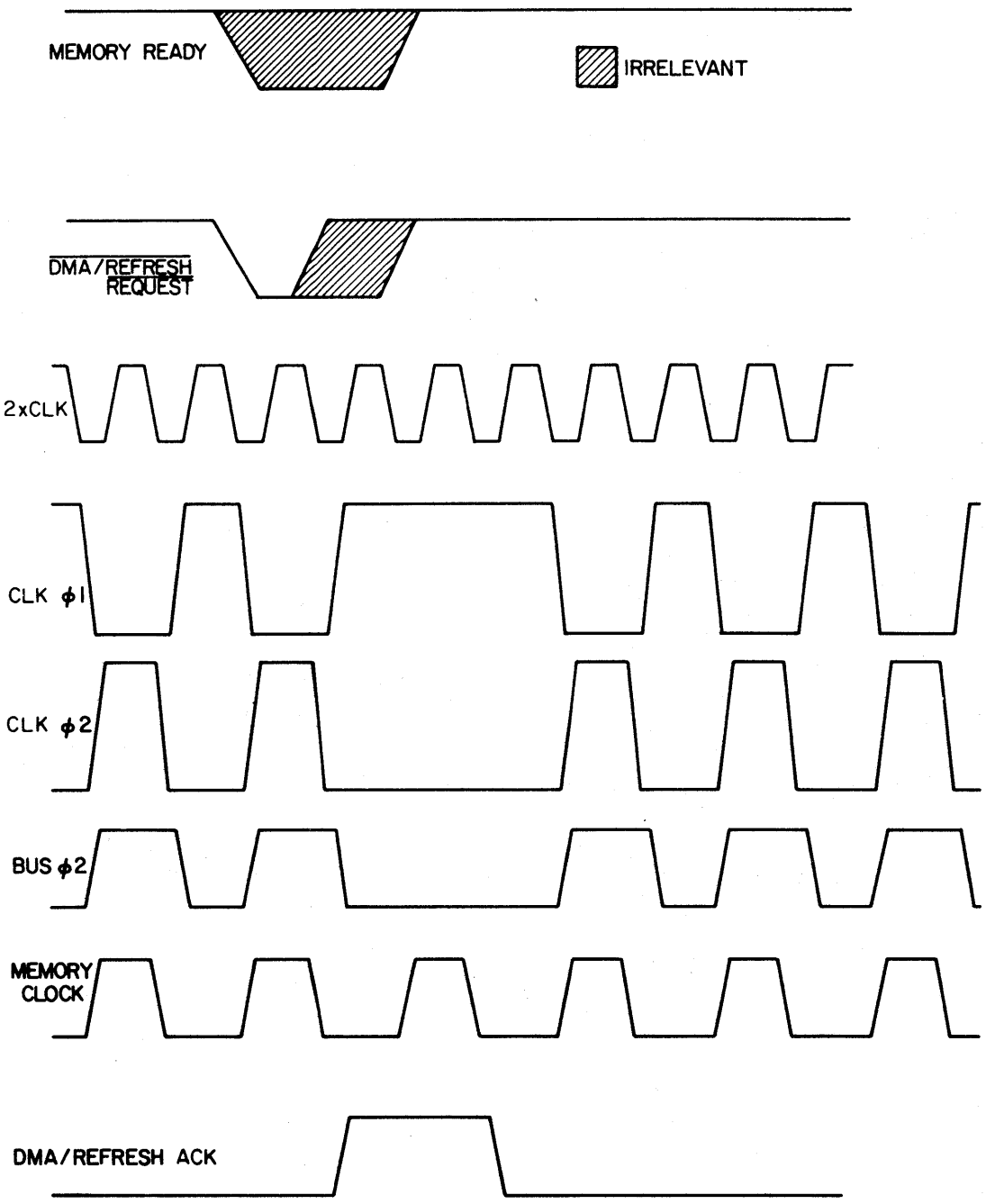


Figure 4. DMA/Refresh Request Stretch Operation
(minimum stretch shown)

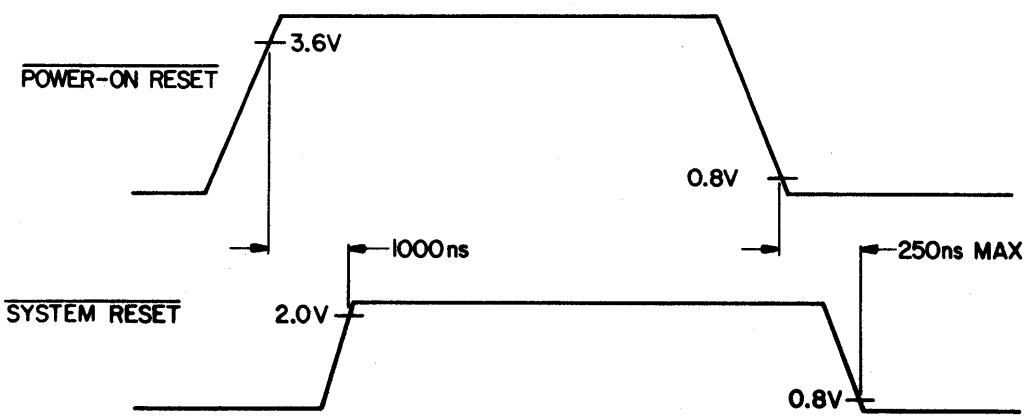


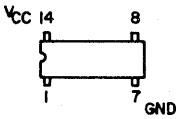
Figure 5. Power On Reset

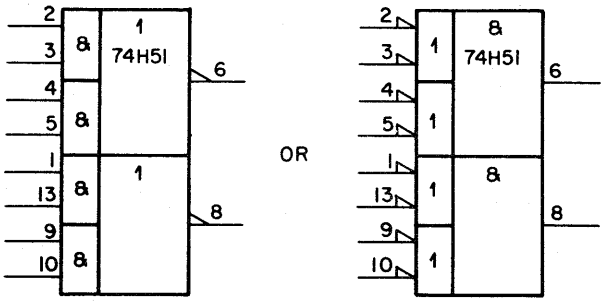
DESCRIPTION

The 74H51 circuit consists of two 2-wide, 2-input, positive AND-OR-INVERT gates in one package.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74H51
3. Package pin configuration:





LOGIC SYMBOL

INPUT PINS				OUT-PUT PIN
2 (1)	3 (13)	4 (9)	5 (10)	6 (8)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

AND-OR-INVERT

INPUT PINS				OUT-PUT PIN
2 (1)	3 (13)	4 (9)	5 (10)	6 (8)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

OR-AND-INVERT

TRUTH TABLES

74H51
Rev J
Sheet 1 of 1

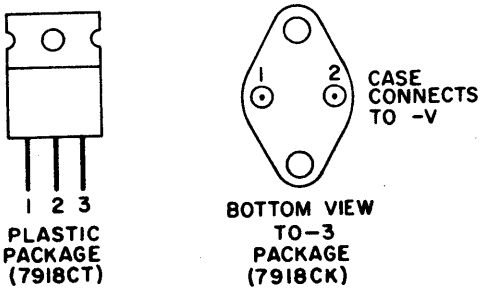
DESCRIPTION

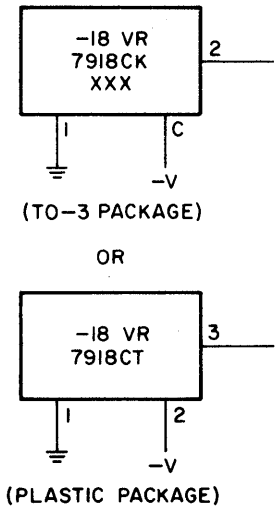
Type 7918C is a negative-voltage regulator employing current limiting, thermal shutdown, and safe-area compensation. The device has a fixed output voltage and with adequate heat-sinking can deliver currents in excess of 1.0 ampere.

The input voltage (-V) should remain 2.0 volts more negative than the output. An input capacitor (typically 0.33 µF) is required if the regulator is placed an appreciable distance from the power supply filter, and a 1.0 µF output capacitor improves stability.

NOTES:

1. Element identifier: none
2. Package pin configuration:





LOGIC SYMBOL

7918C
Rev. J
Sheet 1 of 1

DESCRIPTION

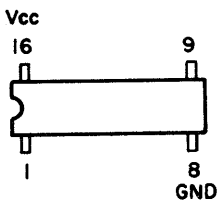
The 9368 is a TTL 7-segment decoder/driver incorporating input latches and providing outputs that can directly drive common-cathode LED displays requiring up to 20 mA (at 1.7V) per segment. The hexadecimal decode network provides outputs for numerics 0-9 and alpha characters A-F. A ripple-blanking feature permits suppression of leading and/or trailing zeros.

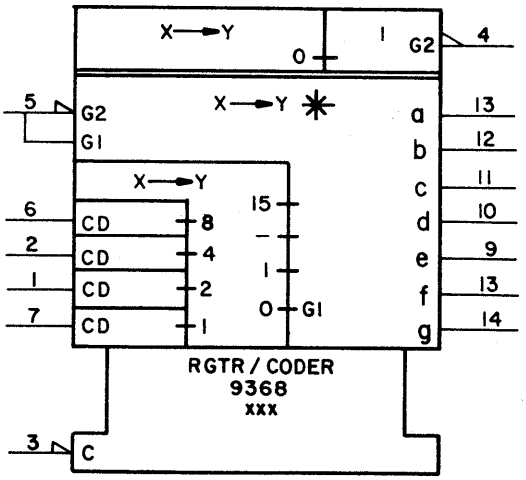
When pin 3 goes low, the input latches are enabled and the outputs present a decode of the input data. When pin 3 goes high, the latch inputs are disabled and the outputs reflect the information retained in the latches.

Zero suppression is effected by connecting the low-active Ripple Blanking Output (pin 4) of one stage to the low-active Ripple Blanking Input (pin 5) of the next lower stage. Pin 5 of the MSB stage is grounded and pin 4 of LSB is left open. This allows a number such as 0060.0300 to be displayed as 60.03.

NOTES:

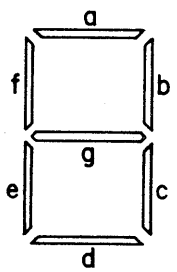
1. Element identifier: None
2. Package pin configuration:



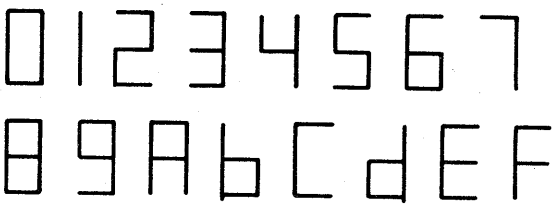


THE ASTERISK INDICATES AN INCOMPLETE PORTRAYAL OF COMPLEX LOGIC.

LOGIC SYMBOL



SEGMENT IDENTIFICATION



CHARACTER REPRESENTATIONS

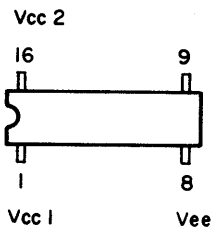
9368
REV L
Sheet 1 of 1

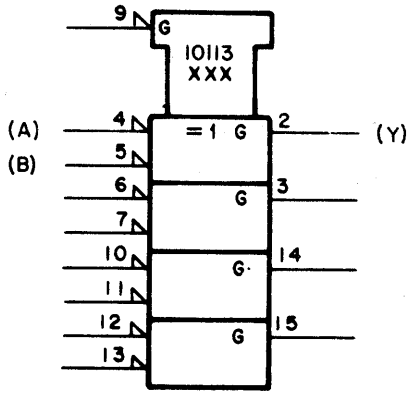
DESCRIPTION

ECL element 10113 comprises four 2-input, dual-purpose gates having a common control (pin 9). When pin 9 is low, the high-active Exclusive OR function Y=AB + AB, or the low-active equivalence (identity) function Y=AB + AB, is performed. When pin 9 is high, all four outputs are forced low, regardless of the state of the other inputs.

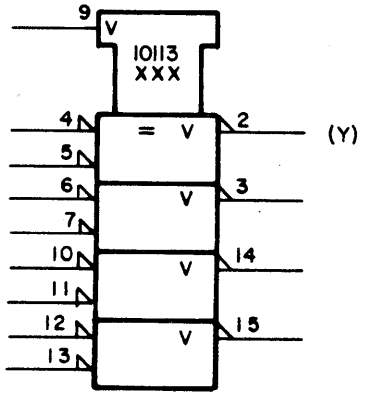
NOTES:

1. Element identifier: none
2. Package pin configuration.





OR



LOGIC SYMBOL

TRUTH TABLE

G/V	A	B	Y
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	X	X	L

X=Don't care

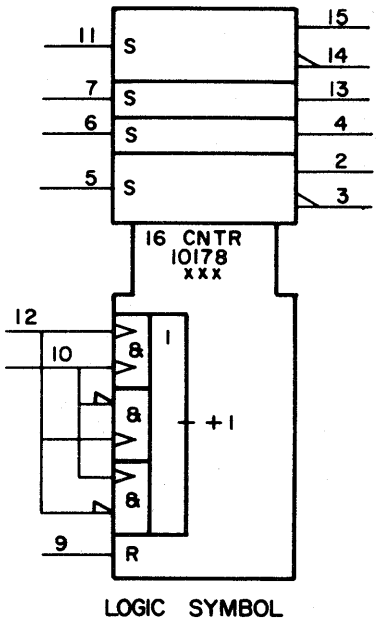
10113
Rev. M
Sheet 1 of 1

DESCRIPTION

The 10178 is a 4-bit ECL binary counter with separate Set inputs for each stage and a common Reset. Complementary outputs are provided for the first and fourth stages.

Pins 10 and 12 provide two positive-edge-triggered clock inputs. The positive-going clock pulse can be applied to both pins simultaneously, or to either pin, provided the other pin is held LOW. That is to say, a static HIGH on either clock input pin inhibits the clocking function, as evidenced by the truth table on sheet 2.

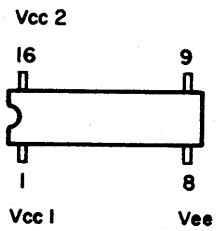
The asynchronous Set and Reset inputs override the clock.

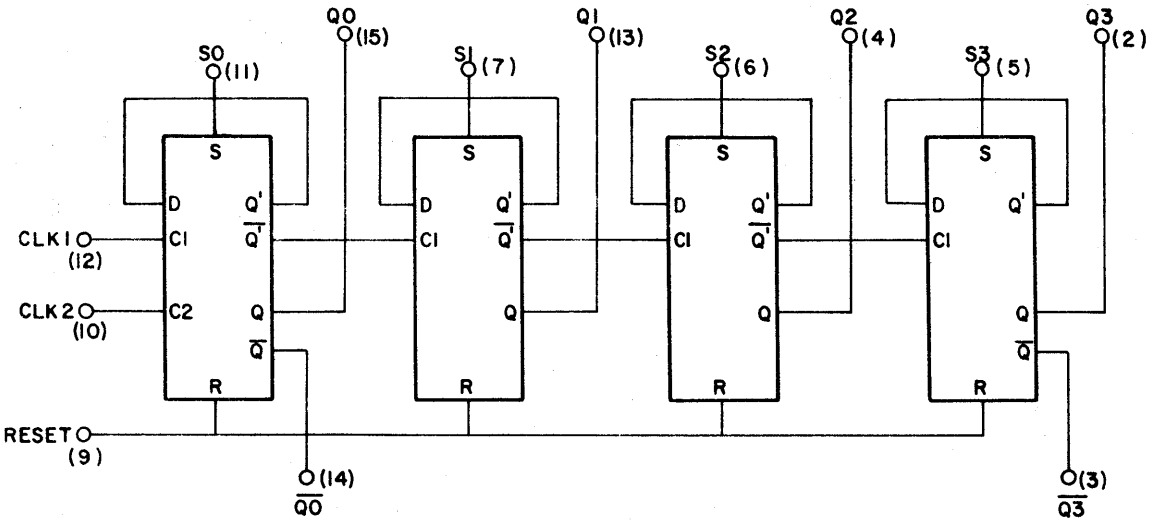


LOGIC SYMBOL

NOTES:

1. Element identifier: None
2. Package pin configuration:





FUNCTIONAL BLOCK DIAGRAM

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	CLK 1	CLK 2	Q0	Q1	Q2	Q3
H	L	L	L	L	X	X	L	L	L	L
L	H	H	H	H	X	X	H	H	H	H
L	L	L	L	L	H	X	NO COUNT			
L	L	L	L	L	X	H	NO COUNT			
L	L	L	L	L	**		L	L	L	L
↑	↑	↑	↑	↑	**		H	L	L	L
					**		L	H	L	L
					**		H	H	L	L
					**		L	L	H	L
					**		H	L	H	L
					**		L	H	H	L
					**		H	H	H	L
					**		L	L	L	H
					**		H	L	L	H
					**		L	H	L	H
					**		H	H	L	H
					**		L	L	H	H
					**		H	L	H	H
↓	↓	↓	↓	↓	**		L	H	H	H
L	L	L	L	L	**		H	H	H	H

KEY

X = DON'T CARE

** = ⎍ ON BOTH CLOCK INPUTS, OR ON EITHER CLOCK INPUT WITH THE OTHER INPUT LOW

DESCRIPTION

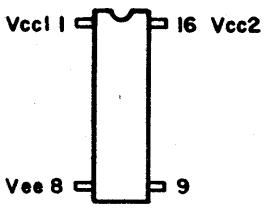
ECL element 10195 is a hex, 2-input inverter/buffer. The pin 9 input is common to all sections.

Each section acts as an inverter for its second input when pin 9 is low, and as a noninverting buffer for its second input when pin 9 is high.

As shown by the truth table, the 10195 therefore performs the Exclusive OR function for low-active signals, and acts as an Equivalence (identity) gate for high-active signals.

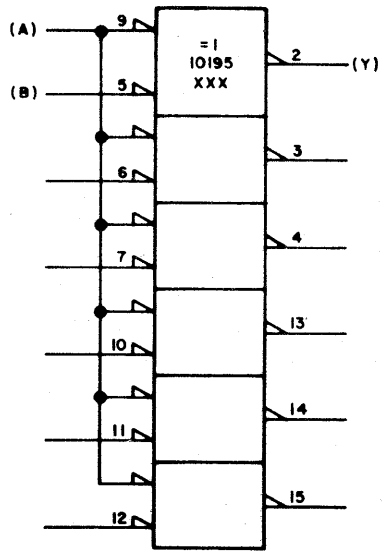
NOTES

1. Element identification: none
2. Package pin configuration.

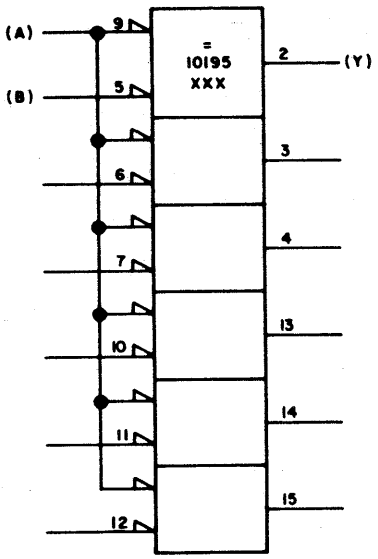


TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H



OR



LOGIC SYMBOL

10195
Rev. M
Sheet 1 of 1

DESCRIPTION

CMOS type 14411 is a bit-rate generator that uses a crystal-controlled oscillator and a frequency-divider network to produce a wide range of output frequencies.

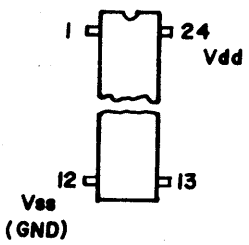
When pin 10 is high, the bit-rate outputs on pins 1 through 11, and on pins 13 through 17, are determined by the state of the two mode select inputs, pins 22 and 23. (Refer to table on sheet 2.)

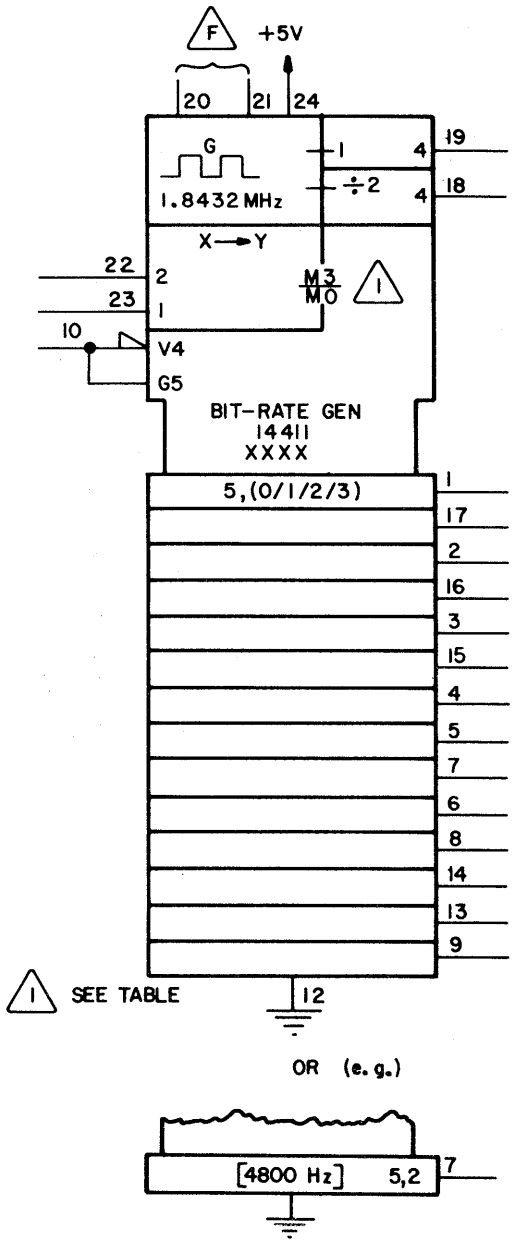
When pin 10 is low, the basic oscillator frequency (1.8432 MHz) appears at pin 19, one-half that basic frequency appears at pin 18, and the other output pins are disabled.

For specific applications, the logic symbol is often abbreviated as shown, with the table reference omitted from the control block.

NOTES:

1. Element identification: none
2. Package pin configuration





LOGIC SYMBOL

MODE SEL 2	MODE SEL 1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

(1)

OUTPUT PIN #	OUTPUT RATES (Hz) 0	1	2	3
9	75	600	1200	4800
13	109.9	879.4	1758.8	7035.5
14	134.5	1076.6	2153.3	8613.2
8	150	1200	2400	9600
6	200	1600	3200	12.8K
7	300	2400	4800	19.2K
5	600	4800	9600	38.4K
4	1200	9600	19.2K	76.8K
15	1800	14.4K	28.8K	115.2K
3	2400	19.2K	38.4K	153.6K
16	3600	28.8K	57.6K	230.4K
2	4800	38.4K	76.8K	307.2K
17	7200	57.6K	115.2K	460.8K
1	9600	76.8K	153.6K	614.4K
18	921.6K			
19	1.8432M			

DESCRIPTION

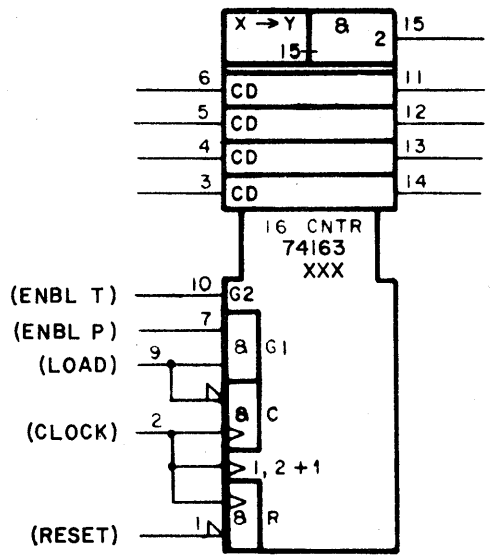
The 74163 is a 4-bit synchronous binary counter. Preset, reset, count, and ripple-carry functions are all synchronized with the rising edge of the clock (pin 2).

The 74163 may be preset to any value appearing at the CD inputs by bringing the Load input (pin 9) low. At the next rising edge of the clock, the output data will agree with the CD input data, regardless of the condition of the Enable P and Enable T inputs.

For counting, Enable P and Enable T (pins 7 and 10) must both be high. Bringing pin 1 (Reset) low clears the counter at the next clock pulse, regardless of the state of the two Enable inputs.

The ripple-carry output is used when cascading counters for n-bit synchronous operations.

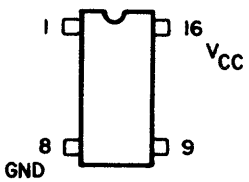
High-to-low transitions on the Enable inputs should occur only when the clock is high.



LOGIC SYMBOL

NOTES:

1. Element identification: 540
2. Package pin configuration



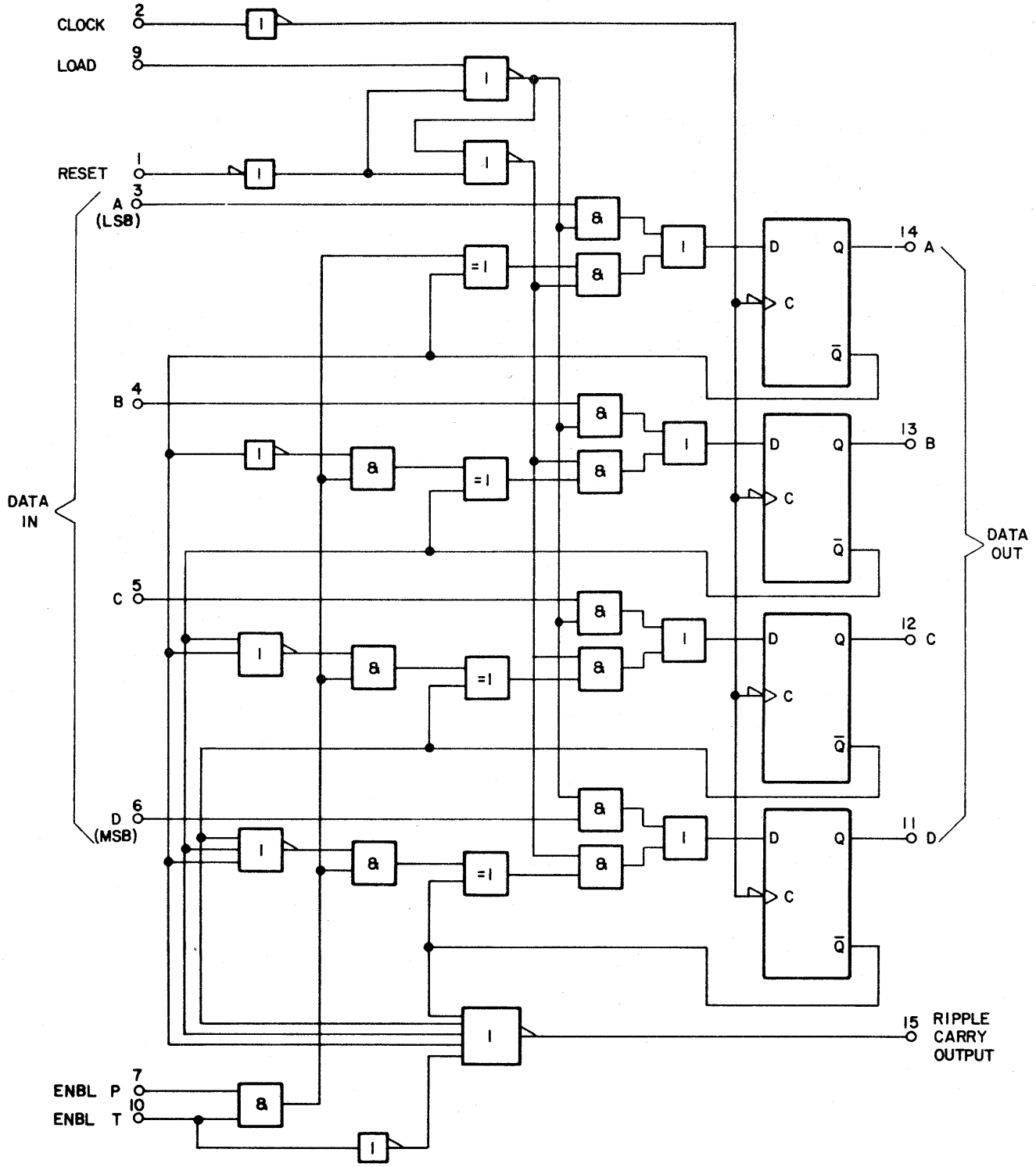


Figure 1. Logic Diagram

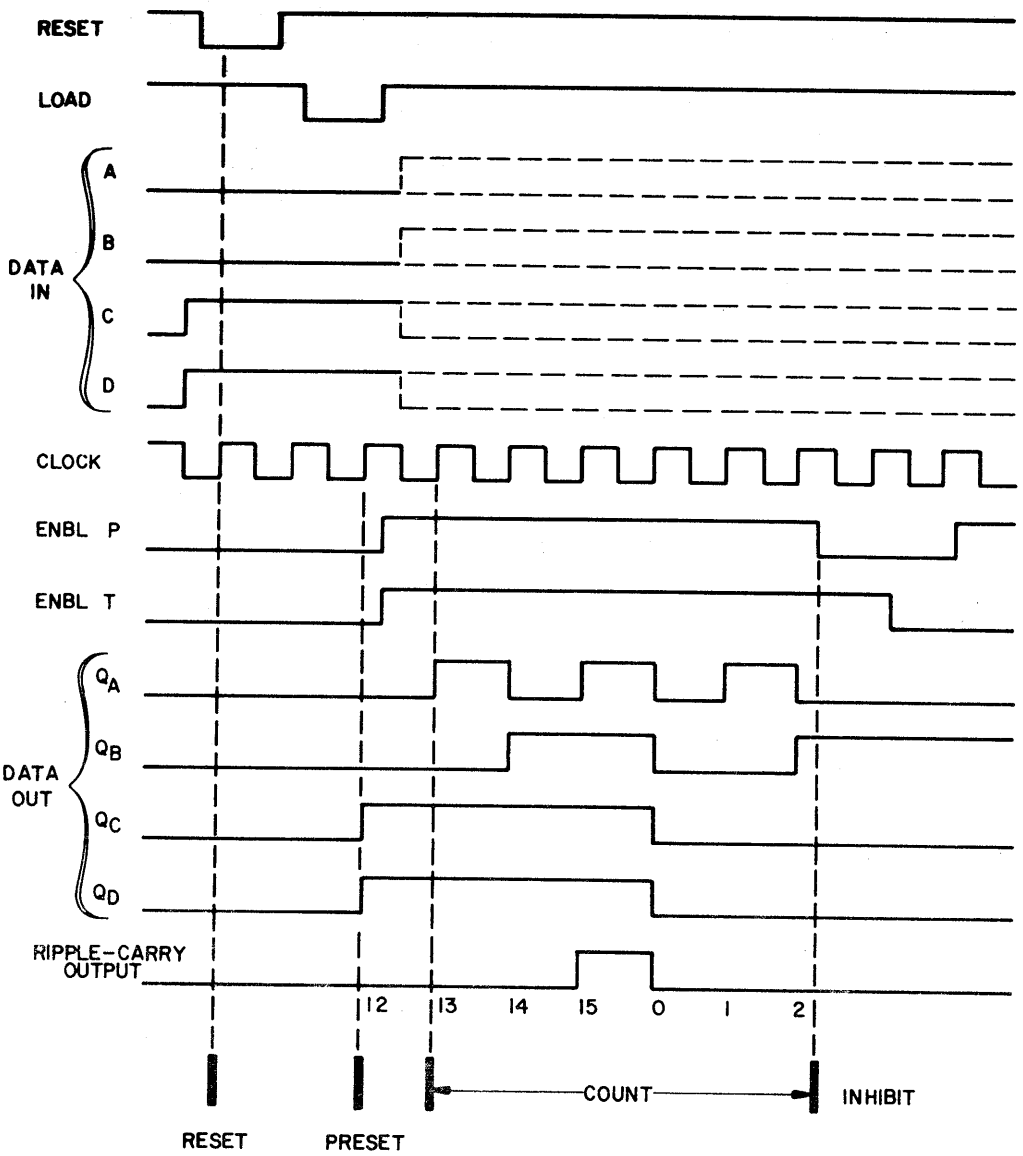


Figure 2. Timing Diagram

DESCRIPTION

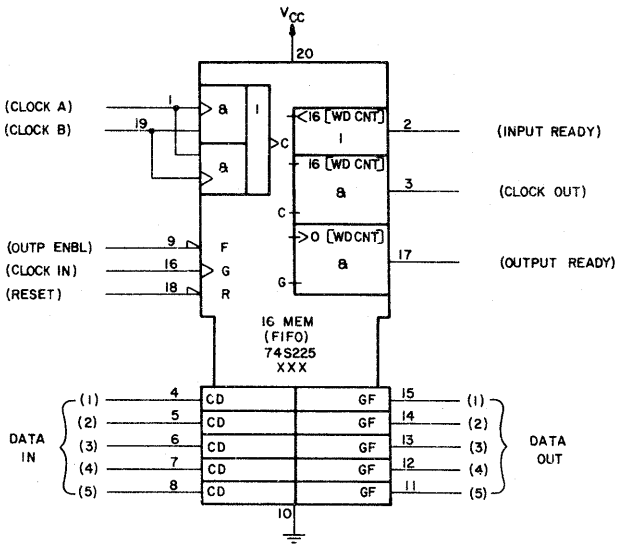
The 74S225 is a first-in-first-out (FIFO) memory, organized as sixteen 5-bit words. Data outputs are three-state. Word lengths can be increased in multiples of 5 bits by paralleling the circuits; the number of words can be increased in multiples of 16 by cascading the circuits. Memory expansion is possible using either or both of these options.

Data is gated into the Last Word position (word 16) of FIFO on the rising edge of Clock A (pin 1) or Clock B (pin 19), provided that the other clock (A or B) is held high. Data will be accepted whenever Input Ready (pin 2) is high, indicating that Word 16 is vacant. Once entered in Word 16, the data ripples through FIFO until it reaches the First Word position (Word 1), or until it can't go any farther without bumping into a word that is already present.

Data is read from the First Word position by bringing Clock In (pin 16) high. If, when pin 16 goes high, the First Word position contains data (Wd Cnt > 0), Output Ready (pin 17) will go high and will remain high until FIFO is completely empty. Output Ready, therefore, indicates the presence of valid data.

The Clock Out signal (pin 3) rises with each gating input, and will stay high if the input data so gated remains in the Last Word position. This indicates that FIFO is full and cannot accept more data. As soon as a word is read from the First Word position, any remaining words ripple down to fill that just-vacated position. This frees the Last Word position (assuming that FIFO had previously been full), and Clock Out returns to a low level.

Data can be read from FIFO only when Output Enable (pin 9) is low. Bringing pin 9 high forces all five data outputs to the Hi-Z state, regardless of other considerations.

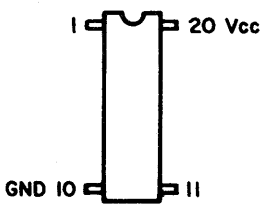


LOGIC SYMBOL

The Reset input (pin 18) invalidates all data stored in FIFO by clearing the control logic and setting Output Ready to a low level on the negative-going edge of the Reset pulse. The data outputs do not change as a result of the Reset; however, Output Ready being at a low level signifies invalid data.

NOTES:

1. Element identification: none
2. Package pin configuration.



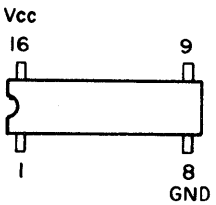
74S225
Rev. M
Sheet 1 of 1

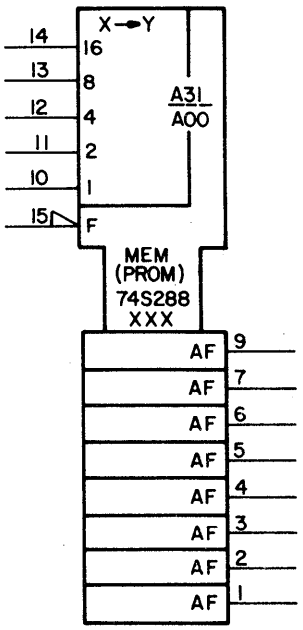
DESCRIPTION

The 74S288 is a 256-bit (32 x 8) PROM with three-state outputs. Typical access time is 25 nanoseconds. Unprogrammed outputs are at a low logic level and are programmed high by burning out the titanium-tungsten fuse link provided for each bit. Once programmed high, the bit cannot be reprogrammed low. When the chip select input (pin 15) is high, all outputs are in the Hi-Z state.

NOTES:

1. Element identifier: none
2. Package pin configuration.





LOGIC SYMBOL

74S288
Rev. M
Sheet 1 of 1

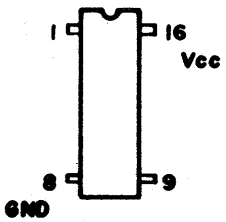
DESCRIPTION

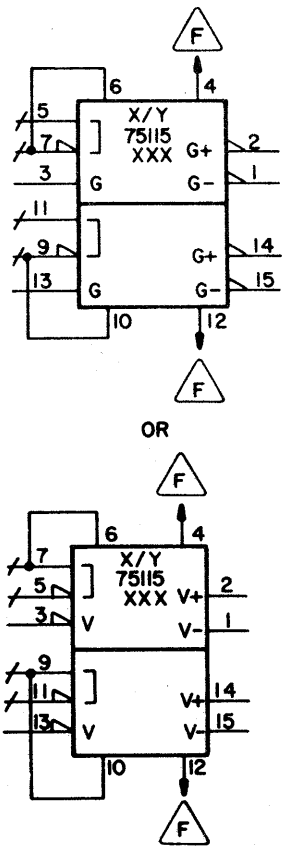
The 75115 is a dual differential line receiver with open-collector outputs. Each section has its own strobe input which, when low, forces the output to a high level. Frequency response for each section is controlled by the external capacitor (connected to pin 4 or 12) to provide immunity to noise spikes.

The outputs are similar to TTL totem-pole outputs, but with the sink output and corresponding active pull-up terminal for each section (see electrical schematic) available on adjacent pins.

NOTES:

1. Element identification: none
2. Package pin configuration





LOGIC SYMBOL

POSITIVE-LOGIC FUNCTION TABLE

Strobe 3 (13)	Diff Input 5,7 (9,11)	Output *
L	X	H
H	L	H
H	H	L

*Measured with respect to circuit ground.

H = $V_I > V_{IH}$ min or V_{ID} more positive than V_{TH} max.

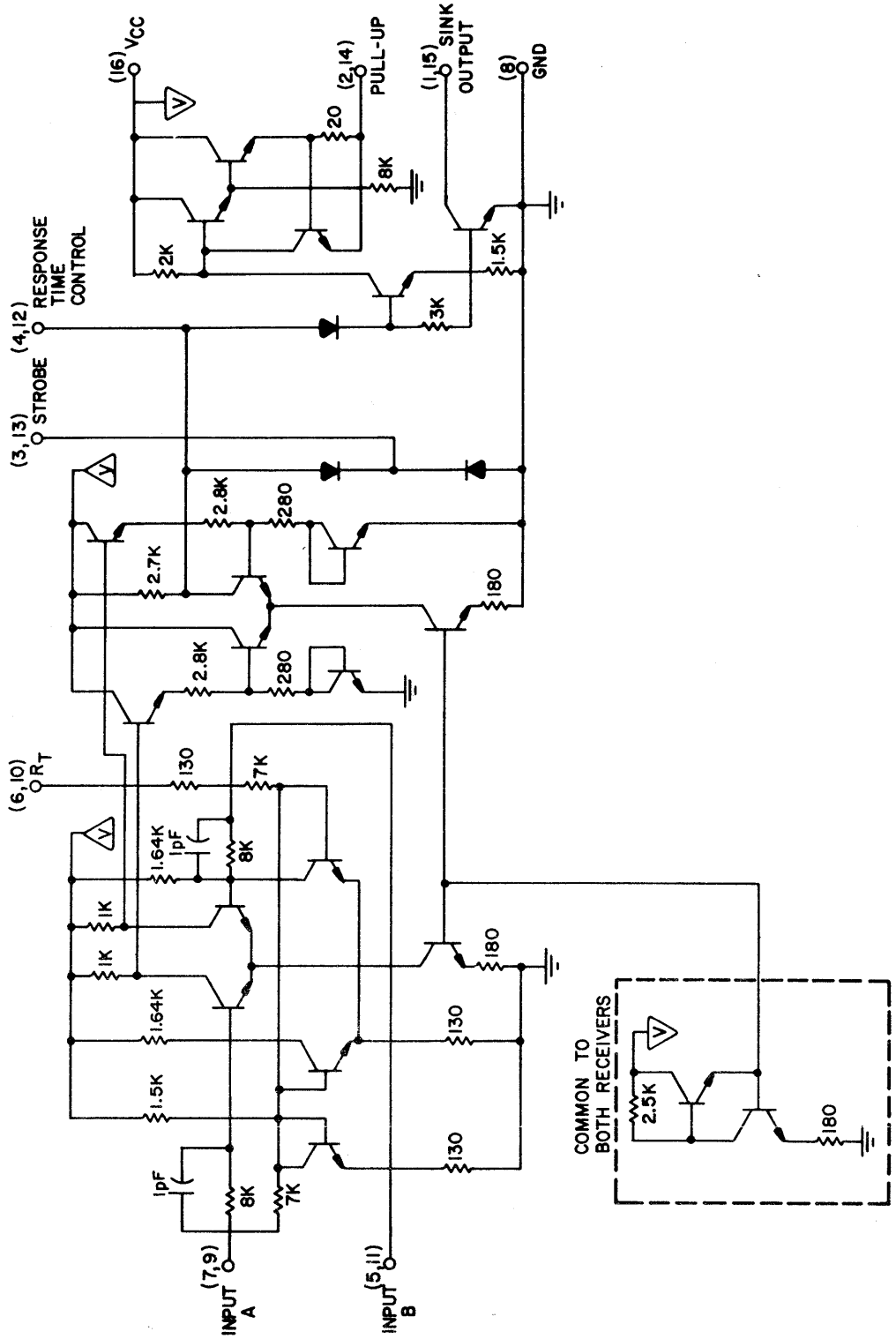
L = $V_I < V_{IL}$ may or V_{ID} more negative than V_{TL} max.

X = Don't care

FUNCTION TABLE KEY

V_I = Strobe voltage
V_{IH} = High-level strobe = 2.4 V min.
V_{IL} = Low=level strobe = 0.4 V max.
V_{ID} = Differential input voltage
V_{TH} = Diff. input, high threshold (+500 mV)
V_{TL} = Diff. input, low threshold (-500 mV)

75115
Rev. M
Sheet 1 of 2



75115
Rev. M
Sheet 2 of 2

DESCRIPTION

The 82S100 and 82S101 are 16 x 48 x 8 Field-Programmable Logic Arrays (FPLA) that are TTL-compatible. The 82S100 has eight three-state outputs; the 82S101 provides eight open-collector outputs. In both arrays, the outputs are enabled when pin 19 goes LO.

These FPLAs have 48 input-AND gates, each of which responds to the true or false states of up to 16 inputs, depending upon how the input matrix is programmed. Likewise, programming the output matrix allows each of the eight OR (output) gates to be activated by one or more of the 48 AND (input) conditions.

Matrix programming consists of burning out (blowing) the links, represented by each pair of crossed lines in Figure 1, for unused inputs to the AND/OR gates. If a "programmed" gate does not use all of its inputs (AND=32 True, 32 False; OR=48), all of the unused links must be blown. If a gate is not used, however, all of its links are left intact. This permits unused gates to be programmed at some future time.

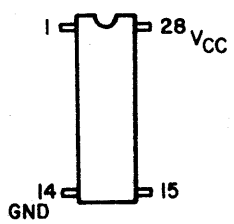
Figure 1 is a representative FPLA configuration utilizing three input lines to provide outputs for the binary numbers 0 through 4. To simplify the presentation, the Output Enable (pin 19) has been omitted. Gate numbers are for illustration only. A truth table (such as that shown) normally appears on the logic diagram. In place of the table, the INPUT PRODUCT/SUM TERMS information or equivalent signal name is displayed on the appropriate output line. Note that the outputs can be programmed active HI or active LO. Here, output 6 is active LO, while outputs 0 through 5 are active HI. Output 7, of course, is unused in this particular example.

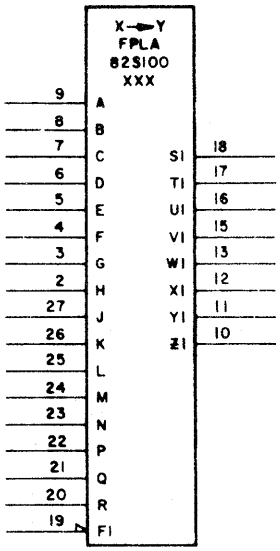
NOTES:

1. Vendor identification:

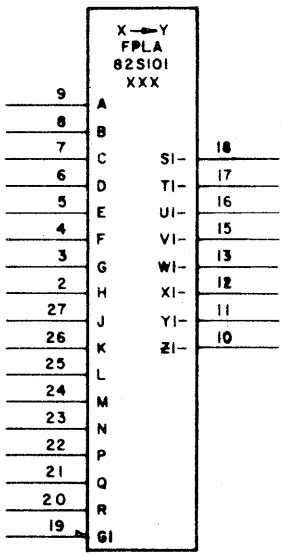
   82S100 (3-state)
   82S101 (open-collector)

2. Element identification: none
3. Package pin configuration





82S100
(THREE-STATE OUTPUTS)

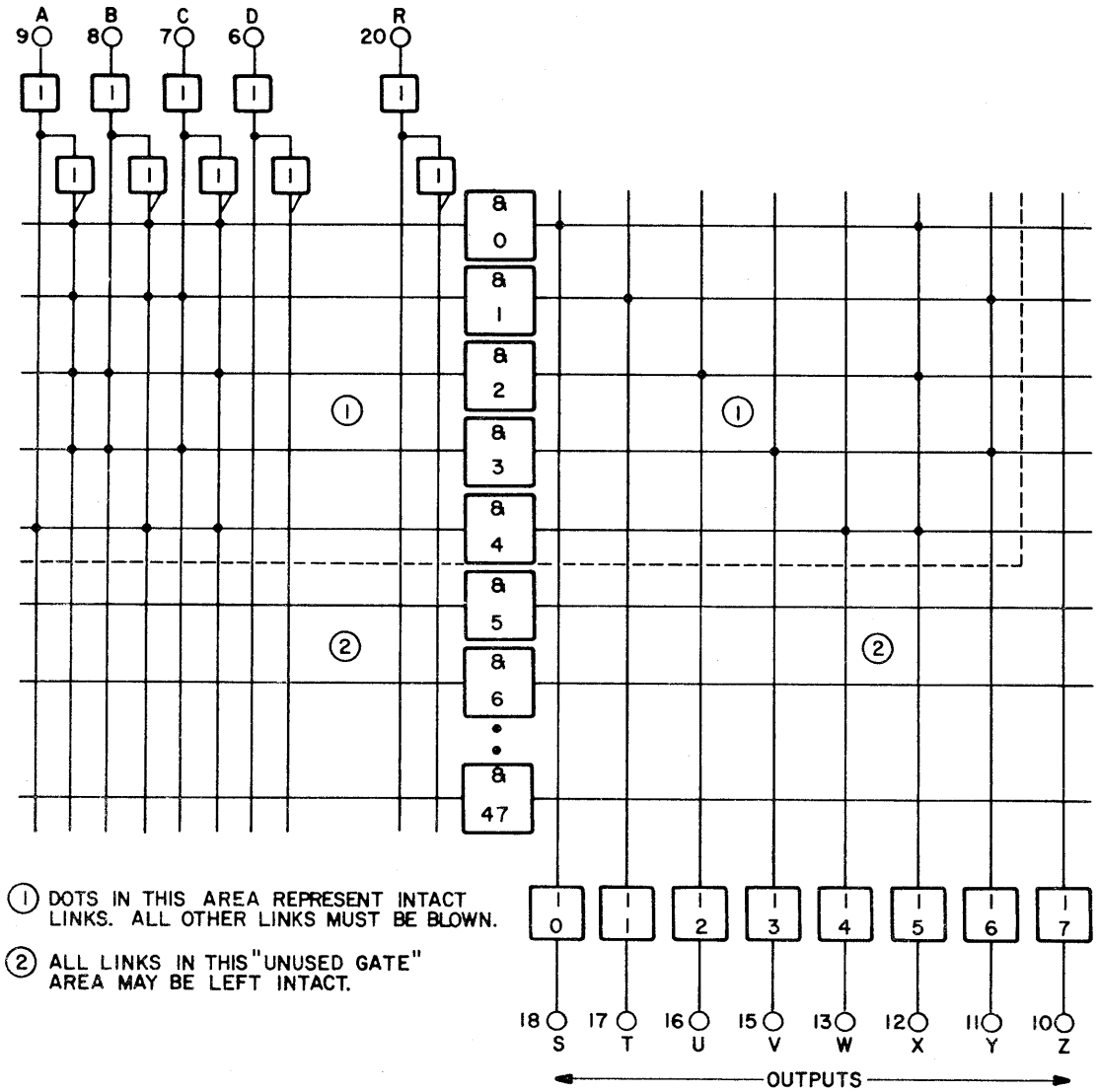


82S101
(OPEN-COLLECTOR OUTPUTS)

NOTE

OUTPUTS PROGRAMMED ACTIVE-LOW MUST BE FLAGGED

LOGIC SYMBOLS



TRUTH TABLE

INPUT PRODUCT/SUM TERMS	OUTPUT/STATE
$\overline{A}\overline{B}\overline{C}$	S = HI
$\overline{A}\overline{B}C$	T = HI
$\overline{A}B\overline{C}$	U = HI
$\overline{A}BC$	V = HI
$A\overline{B}\overline{C}$	W = HI
$\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C}$	X = HI
$\overline{A}\overline{B}C + \overline{A}BC$	Y = LO
(UNUSED)	Z = —

Figure 1. Sample FPLA Configuration

DESCRIPTION

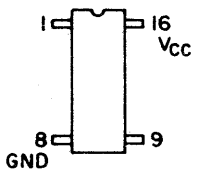
Type 82S131 is a bipolar, 2048-bit, programmable read only memory (PROM) arranged in a 512 x 4 array. When the low-active Enable (pin 13) is high, the three-state outputs are forced to a high-impedance state.

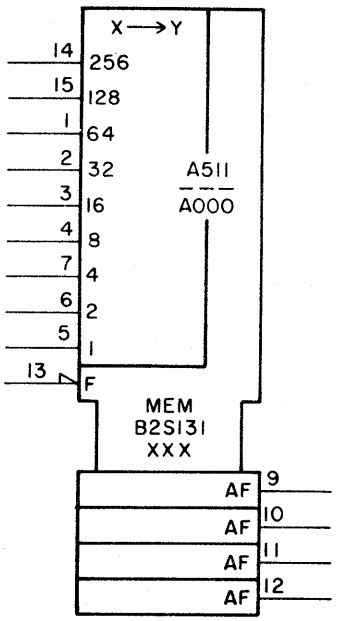
When shipped by the vendor, the device is completely unprogrammed -- that is, all 2048 bits produce a low output when selected. Programming the bits high is a relatively simple procedure that involves selecting an address and raising each output pin to a higher-than-normal Vcc while the Enable pin is held high. This eliminates the need for special programming equipment required by other ROMs or PROMs.

The programming procedure is not reversible. That is, once a bit is programmed high, it cannot be returned to the low-output state.

NOTES:

1. Element identifier: none
2. Package pin configuration:





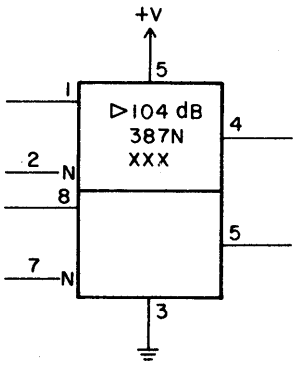
LOGIC SYMBOL

82S131
Rev. J
Sheet 1 of 1

DESCRIPTION:

Element LM387N consists of two low-noise preamplifiers in one package. The 387 will operate satisfactorily over a wide range of power supply voltages from 9 V to 20 V.

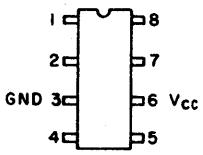
- Output voltage swing: Vcc -2 V (p-p)
- Channel separation: 60 dB



LOGIC SYMBOL

NOTES:

1. Element identifier: none
2. Package pin configuration



LM387N
Rev. J
Sheet 1 of 1

DESCRIPTION

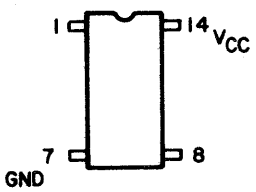
The TIL311 is a single-character hexadecimal display with internal logic for storing and decoding 4-bit binary data, and for displaying same on a 4 x 7 LED matrix. An internal constant-current source ensures uniform intensity of the display (see functional block diagram). This intensity can then be varied, if desired, by pulse=modulating the blanking input (pin 8), which performs its blanking function when high.

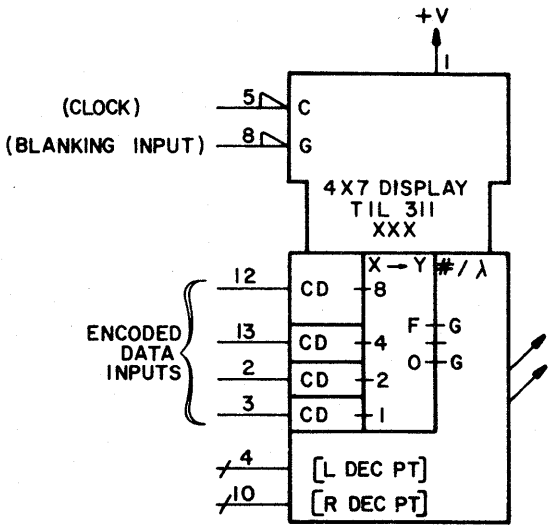
Curent for the two externally driven decimal point LEDs is not affected by TIL311 logic, and must be regulated by the off-chip drivers.

A separate connection for the LED supply (pin 1) permits using a smaller regulated (Vcc) supply. Or, pin 1 may be connected directly to Vcc pin 14.

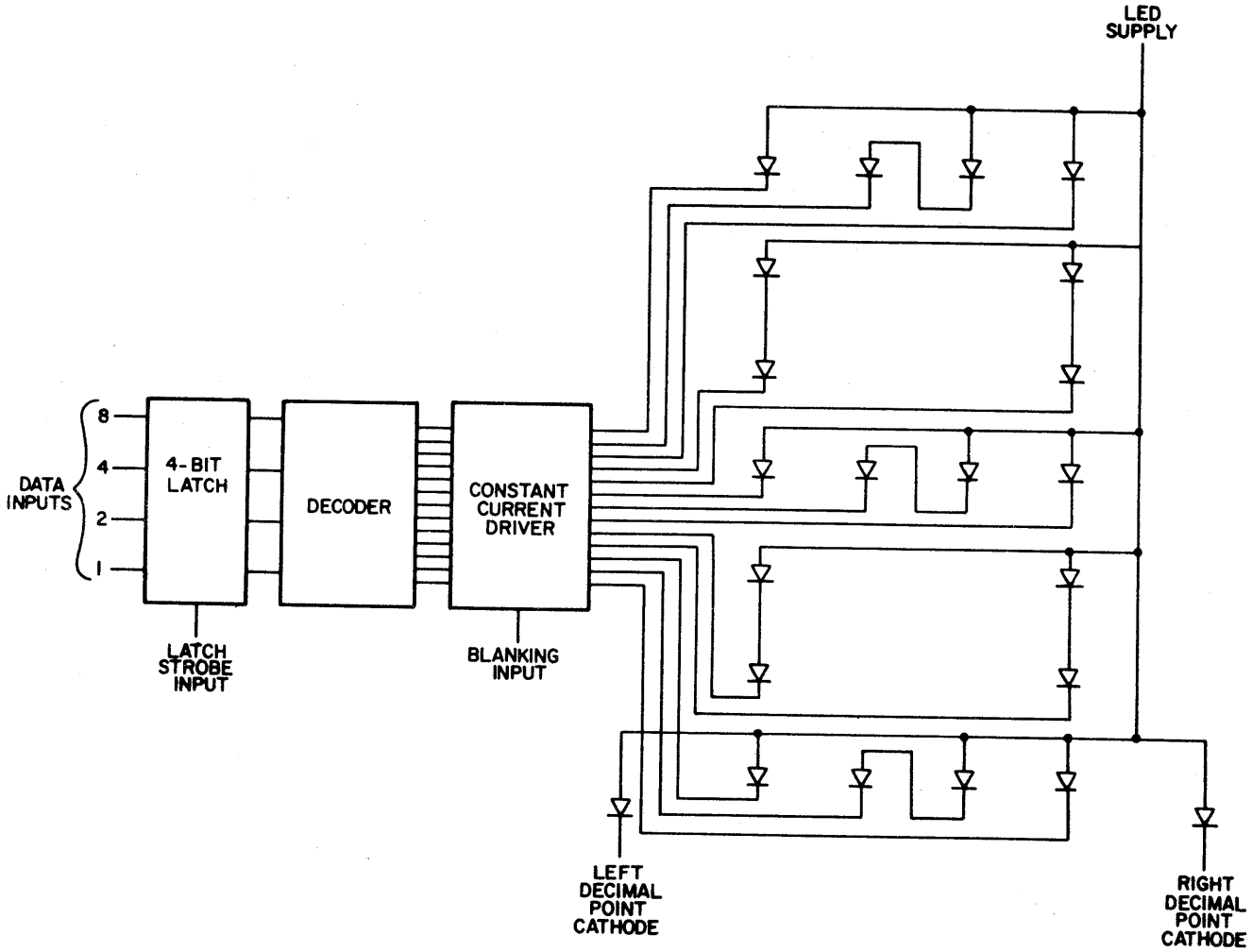
NOTES:

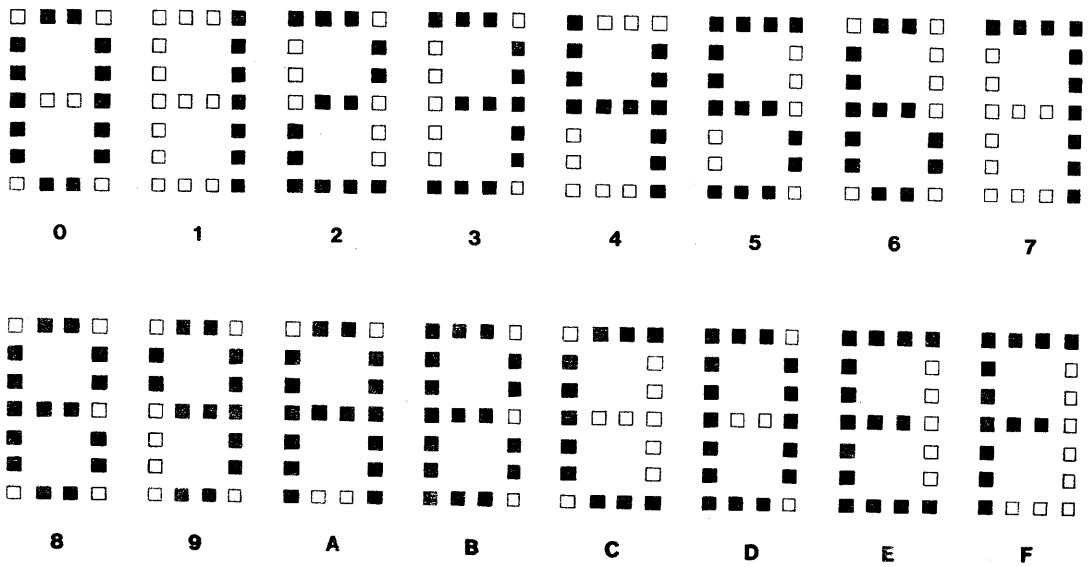
1. Element identifier: none
2. Package pin configuration.





LOGIC SYMBOL





TIL311
Rev. M
Sheet 2 of 2

APPENDIX A

GLOSSARY OF MICROCIRCUIT TERMINOLOGY

APPENDIX A

GLOSSARY OF MICROCIRCUIT TERMINOLOGY

The following terminology is used in this manual to describe microcircuit function and design.

base - (symbol B) The region that lies between an emitter and a collector of a transistor, and into which minority carriers are injected. It corresponds to the grid of an electron tube.

chip - The shaped and processed semiconductor die that is mounted on a substrate to form a transistor, diode, or other semiconductor device.

clock - A source of accurately timed pulses, used for synchronization in a digital computer or as a time base in a transmission system.

clocked flip-flop - A flip-flop circuit (which see) that is triggered only if the data input and clock pulse are present at the same time.

clock frequency - The master frequency of the periodic pulses that schedule the operation of a digital computer.

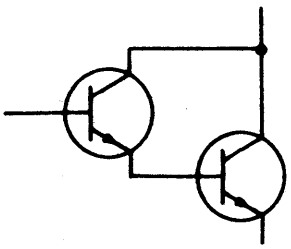
clock rate - The rate at which bits or words are transferred from one internal element of a computer to another.

collector - (symbol C) A semiconductor region through which a primary flow of charge carriers leaves the base of a transistor. The electrode or terminal connected to this region is also called the collector, and corresponds to the anode of an electron tube.

counter - A complete instrument for detecting, totalizing and indicating a sequence of events.

counter circuit - A circuit that receives uniform pulses representing units to be counted and produces a voltage proportional to the total count.

Darlington amplifier - A current amplifier consisting essentially of two separate transistors, often mounted in a single transistor housing. A Darlington amplifier has the same terminations as a single transistor.



decoder - A matrix network in which a combination of inputs produces a single output.

delay multivibrator - A monostable multivibrator that generates an output pulse a predetermined time after it is triggered by an input pulse.

demultiplexer - A device used to separate two or more signals that were previously combined by a compatible multiplexer and transmitted over a single channel.

emitter - (symbol E) A transistor region from which charge carries that are minority carriers in the base are injected into the base. The emitter roughly corresponds to the cathode of an electron tube.

emitter follower - A grounded-collector transistor amplifier whose operation is similar to a cathode follower using a vacuum tube.

flip-flop (FF) - A bistable (two-state) multivibrator, sometimes called an Eccles-Jordan circuit. There are four basic types:

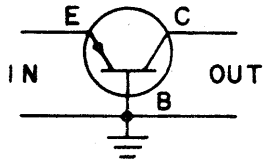
RS (Reset, Set)	- asynchronous (unclocked inputs)
D - type	- synchronous (one clocked input)
J-K type	- synchronous (two clocked inputs)
master/slave	- synchronous (usually two clocked inputs)

In all but the master/slave, outputs change as soon as a change is seen at the inputs. The master/slave has two sets of circuits. The state of the master circuit will track that of the data inputs as long as the clock is active. At the moment the clock goes inactive (trailing edge of the clock signal), data from the master (input) circuit is transferred to the stave (output) circuit.

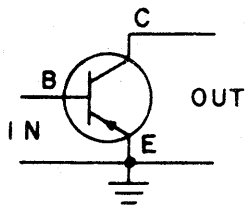
Synchronous FFs may be triggered (set/reset) by either the leading edge of the clock pulse, or by its static level. In addition, asynchronous inputs may be added that will override the trigger action of the clock.

When the output of a FF changes state, the action is called toggling. J-K FFs are unique in that, if both the J and K inputs are active, the outputs will toggle with each clock pulse.

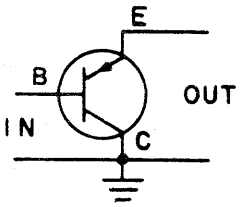
grounded-base connection - A transistor circuit in which the base base electrode is common to both the input and output circuits. The base need not be directly connected to circuit ground. Also called common-base connection.



GROUNDED BASE



GROUNDED EMITTER



GROUNDED COLLECTOR

grounded-collector connection - A transistor circuit in which the collector electrode is common to both the input and output circuits. The collector need not be directly connected to circuit ground. Also called common-collector connection.

grounded-emitter connection - A transistor circuit in which the emitter electrode is common to both the input and output circuits. The emitter need not be directly connected to circuit ground. Also called common-emitter connection.

integrated circuit - An interconnected array of active and passive elements integrated with a single semiconductor substrate or deposited on the substrate by a continuous series of compatible processes, and capable of performing at least one complete electronic circuit function. Normally, only the input, output, and supply terminations are accessible. Also called monolithic circuit and monolithic integrated circuit. When transistors or other discrete components are separately mounted and connected, it is a hybrid integrated circuit.

microcircuit - Generic term for all types of microminiature or microelectronic circuits, including hybrid microcircuits, integrated circuits, thin-film circuits, and monolithic circuits.

microcircuitry - The complete assembly of microcircuits used in a piece of electronic equipment. Also called microelectronic circuitry and microminiature circuitry.

microcircuit wafer - A microwafer containing one or more complete operating microcircuits or stages.

monostable multivibrator - A multivibrator with one stable and one unstable state. A trigger signal is required to drive the unit into the unstable state, where it remains for a predetermined time before returning to the stable state. Also called one-shot multivibrator, single-shot multivibrator, and start-stop multivibrator.

multiplexer - A device for combining two or more signals.

multivibrator - A relaxation oscillator using two tubes, transistors, or other electron devices, with the output of each coupled to the input of the other through resistance-capacitance elements or other elements to obtain in-phase feedback voltage. The fundamental frequency is determined by the time constants of the coupling elements and may be further controlled by an external voltage. When such circuits are normally in a nonoscillating state and a trigger signal is required to start a single cycle of operation, the circuit is commonly called a one-shot multivibrator, a flip-flop circuit, or a start-stop multivibrator.

reference voltage - Reference voltages are typically specified with respect to ground. Unfortunately, there is no industry standard for the various symbols that denote these voltages. Meanwhile, the explanations below hold for this manual, and are generally applicable.

V_{BB} - (Bias) The bias voltage may be produced by an external bias supply or generated internally on each card (or within each IC package). In the latter case, V_{BB} is usually brought out to a connecting pin so as to provide a uniform bias to all applicable circuits.

V_{CC} - (In bipolar (TTL,DTL)and ECL circuits, this term indicates the most-positive supply voltage. In ECL circuits, V_{CC} is typically ground.

V_{DD} - (Drain) In CMOS circuits, this term is generally used in place of V_{CC} to indicate the most-positive supply voltage. When CMOS is used in combination with ECL, V_{DD} is typically ground.

V_{EE} - In ECL circuits, this term indicates the most-negative supply voltage.

V_{SS} - (Source) In CMOS circuits, this term indicates the most-negative supply voltage. When CMOS is used in conjunction with ECL, both V_{SS} and V_{EE} may be used to identify the same (-5.2 V) supply voltage. Often, however, the -5.2 V ECL supply (V_{EE}) may not offer sufficient potential to gain the required speed from the CMOS circuits, and a higher-potential supply (V_{SS}) is necessary. In such cases, V_{SS} and V_{EE} specify different voltages.

reset - Clear.

reset pulse - 1. A drive pulse that tends to reset a magnetic cell in the storage section of a digital computer. 2. A pulse used to reset an electronic counter to zero or to some predetermined position.

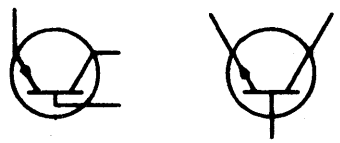
Schmitt trigger - A bistable trigger circuit that converts an a-c input signal into a square-wave output signal by switching action, triggered at a predetermined point in each positive and negative swing of the input signal.

shift - Displacement of an ordered set of characters one or more places to the left or right in a digital computer. If the characters are the digits of a numerical expression, a shift may be equivalent to multiplying by a power of the base.

shift pulse - A drive pulse that initiates shifting of characters in the register of a digital computer.

shift register - A computer circuit that converts a sequence of input signals into a parallel binary number or vice versa, by moving stored characters to the right or left.

transistor - (TRANSfer resISTOR) An active semiconductor device having three or more electrodes. The three main electrodes used are the emitter, collector, and base.



Conduction is by means of electrons and carriers or holes. Germanium and silicon are the materials most often used as the semiconductor material. Transistors can perform practically all the functions of tubes, including amplification and rectification.

transistor-transistor logic - A logic circuit containing two transistors, for driving large output capacitances at high speed.

triggering - Initiation of an action in a circuit, which then functions for a predetermined time.

trigger circuit - 1. A circuit or network in which the output changes abruptly with an infinitesimal change in input at a predetermined operating point. Also called trigger. 2. A circuit in which an action is initiated by an input pulse, as in a radar modulator. 3. Flip-flop circuit.

truth table - A table that describes a function by listing all possible combinations of input values and indications for the output.

AND

B	A	C
L	L	L
L	H	L
H	L	L
H	H	H

OR

B	A	C
L	L	L
L	H	H
H	L	H
H	H	H

NAND

B	A	C
L	L	H
L	H	H
H	L	H
H	H	L

Truth tables for three gating functions.

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